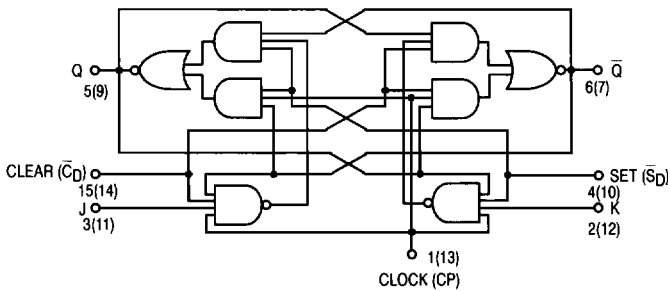




DUAL JK NEGATIVE EDGE-TRIGGERED FLIP-FLOP

The SN54/74LS112A dual JK flip-flop features individual J, K, clock, and asynchronous set and clear inputs to each flip-flop. When the clock goes HIGH, the inputs are enabled and data will be accepted. The logic level of the J and K inputs may be allowed to change when the clock pulse is HIGH and the bistable will perform according to the truth table as long as minimum set-up and hold time are observed. Input data is transferred to the outputs on the negative-going edge of the clock pulse.

LOGIC DIAGRAM (Each Flip-Flop)



MODE SELECT — TRUTH TABLE

OPERATING MODE	INPUTS				OUTPUTS	
	\bar{S}_D	\bar{C}_D	J	K	Q	\bar{Q}
Set	L	H	X	X	H	L
Reset (Clear)	H	L	X	X	L	H
*Undetermined	L	L	X	X	H	H
Toggle	H	H	h	h	q	q
Load "0" (Reset)	H	H	l	h	L	H
Load "1" (Set)	H	H	h	l	H	L
Hold	H	H	l	l	q	q

* Both outputs will be HIGH while both \bar{S}_D and \bar{C}_D are LOW, but the output states are unpredictable if \bar{S}_D and \bar{C}_D go HIGH simultaneously.

H, h = HIGH Voltage Level

L, l = LOW Voltage Level

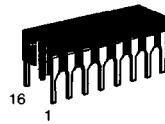
X = Don't Care

l, h (q) = Lower case letters indicate the state of the referenced input (or output) one set-up time prior to the HIGH to LOW clock transition.

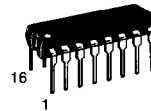
SN54/74LS112A

DUAL JK NEGATIVE EDGE-TRIGGERED FLIP-FLOP

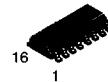
LOW POWER SCHOTTKY



J SUFFIX
CERAMIC
CASE 620-09



N SUFFIX
PLASTIC
CASE 648-08

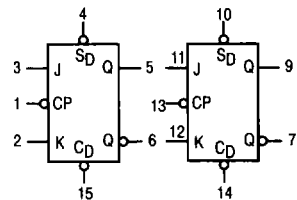


D SUFFIX
SOIC
CASE 751B-03

ORDERING INFORMATION

SN54LSXXXJ Ceramic
SN74LSXXXN Plastic
SN74LSXXXD SOIC

LOGIC SYMBOL



V_{CC} = PIN 16
GND = PIN 8

5

SN54/74LS112A

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V _{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T _A	Operating Ambient Temperature Range	54 74	-55 0	25 25	125 70	°C
I _{OH}	Output Current — High	54, 74			-0.4	mA
I _{OL}	Output Current — Low	54 74			4.0 8.0	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter		Limits			Unit	Test Conditions
			Min	Typ	Max		
V _{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V _{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs
		74			0.8		
V _{IK}	Input Clamp Diode Voltage			-0.65	-1.5	V	V _{CC} = MIN, I _{IN} = -18 mA
V _{OH}	Output HIGH Voltage	54	2.5	3.5		V	V _{CC} = MIN, I _{OH} = MAX, V _{IN} = V _{IH} or V _{IL} per Truth Table
		74	2.7	3.5		V	
V _{OL}	Output LOW Voltage	54, 74		0.25	0.4	V	I _{OL} = 4.0 mA
		74		0.35	0.5	V	I _{OL} = 8.0 mA
I _{IH}	Input HIGH Current	J, K Set, Clear Clock			20 60 80	μA	V _{CC} = MAX, V _{IN} = 2.7 V
		J, K Set, Clear Clock			0.1 0.3 0.4	mA	V _{CC} = MAX, V _{IN} = 7.0 V
I _{IL}	Input LOW Current	J, K Clear, Set, Clk			-0.4 -0.8	mA	V _{CC} = MAX, V _{IN} = 0.4 V
I _{OS}	Short Circuit Current (Note 1)		-20		-100	mA	V _{CC} = MAX
I _{CC}	Power Supply Current				6.0	mA	V _{CC} = MAX

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

AC CHARACTERISTICS (T_A = 25°C, V_{CC} = 5.0 V)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
f _{MAX}	Maximum Clock Frequency	30	45		MHz	V _{CC} = 5.0 V C _L = 15 pF
t _{PLH}	Propagation Delay, Clock Clear, Set to Output		15	20	ns	
t _{PHL}			15	20	ns	

AC SETUP REQUIREMENTS (T_A = 25°C, V_{CC} = 5.0 V)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
t _W	Clock Pulse Width High	20			ns	V _{CC} = 5.0 V
t _W	Clear, Set Pulse Width	25			ns	
t _s	Setup Time	20			ns	
t _h	Hold Time	0			ns	