National Semiconductor

ADVANCE INFORMATION

74LVT543
3.3V ABT Octal Registered Transceiver with TRI-STATE® Outputs

General Description

The 'LVT543 octal transceiver contains two sets of D-type latches for temporary storage of data flowing in either direction. Separate Latch Enable and Output Enable inputs are provided for each register to permit independent control of inputting and outputting in either direction of data flow.

These octal registered transceivers is/are designed for low-voltage (3.3V) V_{CC} applications, but with the capability to provide a TTL interface to a 5V environment. The LVT543 is fabricated with an advanced BiCMOS technology to achieve high speed operation similar to 5V ABT while maintaining a low power dissipation.

Features

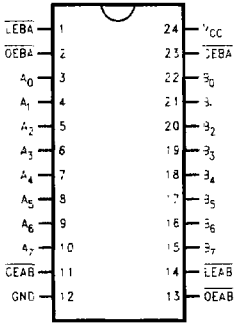
- Input and output interface capability to systems at 5V V_{CC}
- Bus-Hold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Live insertion/extraction permitted
- Power Up/Down high impedance provides glitch-free bus loading
- Outputs source/sink −32 mA/ +64 mA
- Available in SOIC JEDEC and TSSOP
- Functionally compatible with the 74 series 543
- Latch-up performance exceeds 500 mA

Pin Descriptions

Pin Names	Description
$\overline{OEAB}$, $\overline{OEBA}$	Output Enable Inputs
$\overline{LEAB}$, $\overline{LEBA}$	Latch Enable Inputs
$\overline{CEAB}$, $\overline{CEBA}$	Chip Enable Inputs
A_0–A_7	Side A Inputs or TRI-STATE Outputs
B_0–B_7	Side B Inputs or TRI-STATE Outputs

Connection Diagram

Pin Assignment for SOIC, SSOP II and TSSOP



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	SOIC JEDEC	TSSOP	SSOP II
Order Number	74LVT543WM 74LVT543WMX	74LVT543MTC 74LVT543MTCX	74LTV543MSA 74LTV543MSAX
See NS Package Number	M24B	MTC24	MSA24

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Functional Description

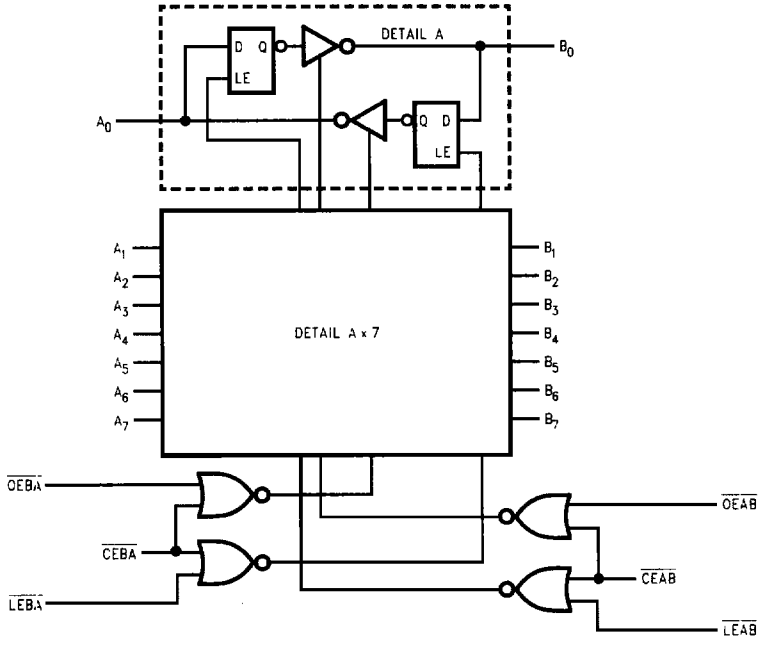
The 'LVT543 contains two sets of D-type latches, with separate input and output controls for each. For data flow from A to B, for example, the A to B Enable ($\overline{CEAB}$) input must be low in order to enter data from the A port or take data from the B port as indicated in the Data I/O Control Table. With $\overline{CEAB}$ low, a low signal on ($\overline{LEAB}$) input makes the A to B latches transparent; a subsequent low to high transition of the $\overline{LEAB}$ line puts the A latches in the storage mode and their outputs no longer change with the A inputs. With $\overline{CEAB}$ and $\overline{OEAB}$ both low, the B output buffers are active and reflect the data present on the output of the A latches. Control of data flow from B to A is similar, but using the $\overline{CEBA}$, $\overline{LEBA}$ and $\overline{OEBA}$.

Data I/O Control Table

Inputs			Latch Status	Output Buffers
$\overline{CEAB}$	$\overline{LEAB}$	$\overline{OEAB}$		
H	X	X	Latched	High Z
X	H	X	Latched	—
L	L	X	Transparent	—
X	X	H	—	High Z
L	X	L	—	Driving

H = High Voltage Level
L = Low Voltage Level
X = Immaterial

Logic Diagram



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