

January 1996

## Radiation Hardened Octal Non-Inverting Three-State Buffer

### Features

- Devices QML Qualified in Accordance with MIL-PRF-38535
- Detailed Electrical and Screening Requirements are Contained in SMD# 5962-96718 and Harris' QM Plan
- 1.25 Micron Radiation Hardened SOS CMOS
- Total Dose ..... >300K RAD (Si)
- Single Event Upset (SEU) Immunity:  $<1 \times 10^{-10}$  Errors/Bit/Day (Typ)
- SEU LET Threshold ..... >100 MEV-cm<sup>2</sup>/mg
- Dose Rate Upset ..... >10<sup>11</sup> RAD (Si)/s, 20ns Pulse
- Dose Rate Survivability ..... >10<sup>12</sup> RAD (Si)/s, 20ns Pulse
- Latch-Up Free Under Any Conditions
- Military Temperature Range ..... -55°C to +125°C
- Significant Power Reduction Compared to ALSTTL Logic
- DC Operating Voltage Range ..... 4.5V to 5.5V
- Input Logic Levels
  - VIL = 0.8V Max
  - VIH = VCC/2 Min
- Input Current  $\leq 1\mu A$  at VOL, VOH
- Fast Propagation Delay ..... 14.5ns (Max), 10ns (Typ)

### Description

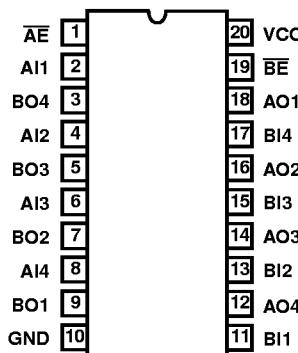
The Harris ACTS244MS is a Radiation Hardened Octal Non-Inverting Three-State Buffer having two active low enable inputs.

The ACTS244MS utilizes advanced CMOS/SOS technology to achieve high-speed operation. This device is a member of radiation hardened, high-speed, CMOS/SOS Logic Family.

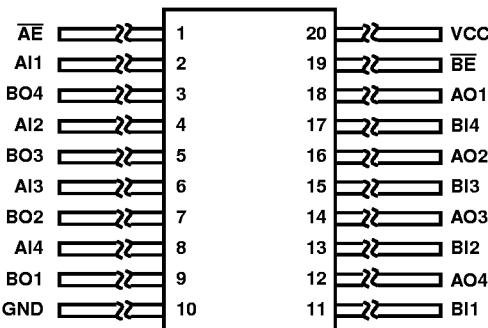
The ACTS244MS is supplied in a 20 lead Ceramic Flatpack (K suffix) or a Dual-In-Line Ceramic Package (D suffix).

### Pinouts

20 PIN CERAMIC DUAL-IN-LINE  
MIL-STD-1835 DESIGNATOR CDIP2-T20,  
LEAD FINISH C  
TOP VIEW



20 PIN CERAMIC FLATPACK  
MIL-STD-1835 DESIGNATOR CDFP4-F20,  
LEAD FINISH C  
TOP VIEW



### Ordering Information

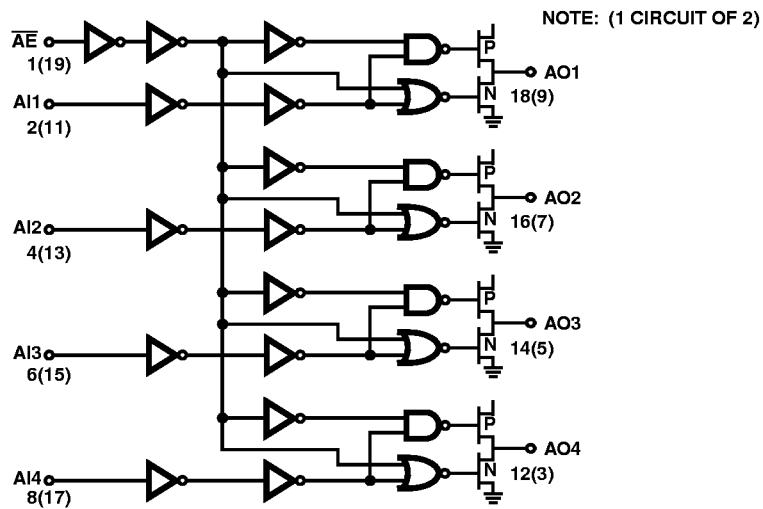
PART NUMBER	TEMPERATURE RANGE	SCREENING LEVEL	PACKAGE
5962F9671801VRC	-55°C to +125°C	MIL-PRF-38535 Class V	20 Lead SBDIP
5962F9671801VXC	-55°C to +125°C	MIL-PRF-38535 Class V	20 Lead Ceramic Flatpack
ACTS244D/Sample	25°C	Sample	20 Lead SBDIP
ACTS244K/Sample	25°C	Sample	20 Lead Ceramic Flatpack
ACTS244HMSR	25°C	Die	Die

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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Spec Number **518784**

File Number **3187.1**

***Functional Diagram*****TRUTH TABLE**

INPUTS		OUTPUT
$\overline{AE}$ , $\overline{BE}$	$AIn$ , $BIn$	$AOn$ , $BOn$
L	L	L
L	H	H
H	X	Z

NOTE: H = High Voltage Level, L = Low Voltage Level,  
X = Immaterial, Z = High Impedance

**Die Characteristics****DIE DIMENSIONS:**

100 x 100 (mils)  
2.54 x 2.54 (mm)

**METALLIZATION:**

Type: AlSi  
Metal 1 Thickness:  $7.125\text{ k}\text{\AA} \pm 1.125\text{ k}\text{\AA}$   
Metal 2 Thickness:  $9\text{ k}\text{\AA} \pm 1\text{ k}\text{\AA}$

**GLASSIVATION:**

Type:  $\text{SiO}_2$   
Thickness:  $8\text{ k}\text{\AA} \pm 1\text{ k}\text{\AA}$

**WORST CASE CURRENT DENSITY:**

$< 2.0 \times 10^5 \text{ A/cm}^2$

**BOND PAD SIZE:**

110 x 110 ( $\mu\text{m}$ )  
4.4 x 4.4 (mils)

***Metallization Mask Layout***

ACTS244MS

