ISI IDEAL SEMICONDUCTOR INC.
"Your Best Defense Against Obsolescence"

OBJECTIVE SPECIFICATIONS

3-Line to 8-Line Decoders/Multiplexers

Features

- Designed specifically for high-speed memory decoders and data transmission systems
- Incorporates 3 enable inputs to simplify cascading and/or data reception
- Function, pin-out, speed and drive compatability with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs: I_{OL} = 8 mA @ V_{OL} = 0.5V
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industial and military temperature ranges:

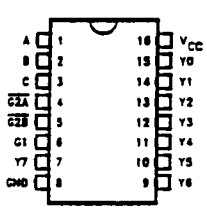
  74AHCT: -40°C to +85°C
  54AHCT: -55°C to +125°C

Function Table

Enable Inputs		Select Inputs			Outputs							
G1	$\overline{G2}$*	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	H	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	H	H	H	H	H	L	H	H	H	H
H	L	H	L	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	H	L	H	H
H	L	H	H	L	H	H	H	H	H	H	L	H
H	L	H	H	H	H	H	H	H	H	H	H	L

*$\overline{G2} = \overline{G2A} + \overline{G2B}$

Pin Configuration



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Description

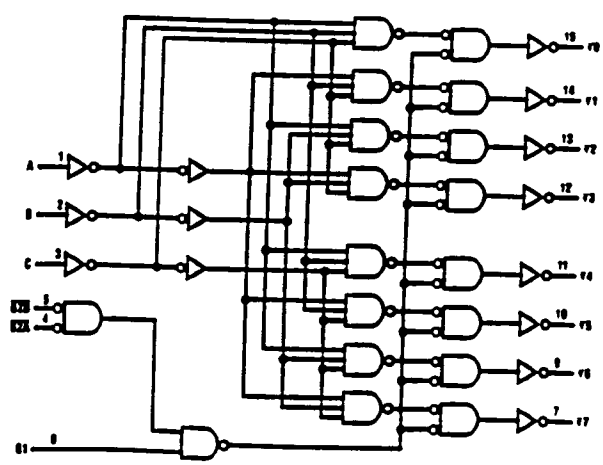
These devices are designed to be used in high-performance memory-decoding or data-routing applications requiring very short propagation delay times. In high-performance memory systems, these decoders can be used to minimize the effects of system decoding. When used with high-speed memories utilizing a fast-enable circuit, the delay times of these decoders and the enable time of the memory are usually less than the typical access time of the memory. This means that the effective system delay introduced by the decoder is negligible.

The conditions at the binary select inputs and the three enable inputs select one of eight input lines. Two active-low and one active-high enable inputs reduce the need for external gates or inverters when expanding. A 24-line decoder can be implemented without external inverters and a 32-line decoder requires only one inverter. An enable input can be used as a data input for demultiplexing applications.

Fabrication using ISI proprietary ICE-MOS process, these devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Logic Diagram



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Absolute Maximum Ratings*

Supply Voltage Range, V_{CC} .....-0.5V to 7V
DC Input Diode Current, I_{IK}
(V_I <-0.5V or V_I >V_{CC} + 0.5V)..... ±20 mA
DC Output Diode Current, I_{OK}
(V_O <-0.5V or V_O >V_{CC} + 0.5V)..... ±20 mA
Continuous Output Current Per Pin, I_O
(-0.5V<V_O<V_{CC} + 0.5V)..... ±35 mA
Continuous Current Through
V_{CC} or GND pins..... ±125 mA
Storage Temperature Range, T_{STG} .....-65°C to +150°C
Power Dissipation Per Package, P_D• .....500 mW

*Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

•Power Dissipation temperature derating:
Plastic Package (N): -12mW/°C from 65°C to 85°C
Ceramic Package (J): -12mW/°C from 100°C to 125°C

Recommended Operating Conditions

Supply Voltage, V_{CC} .....4.5V to 5.5V
DC Input & Output Voltages*, V_{IN}, V_{OUT} .....0V to V_{CC}

Operating Temperature

Range	74AHCT:	-40°C to +85°C
	54AHCT:	-55°C to +125°C

Input Rise & Fall Times, t_r , t_f .....Max 500 ns

*Unused inputs must always to tied to an appropriate logic voltage level (either V_{CC} or GND)

DC Electrical Characteristics (V_{CC} = 5V ±10% Unless Otherwise Specified)

Sym	Parameter	Test Conditions	T_A = 25°C	74AHCT T_A = -40°C to +85°C	54AHCT T_A = -55°C to +125°C	Unit
			Typ	Guaranteed Limits		
V_{IH}	Minimum High-Level Input Voltage			2.0	2.0	2.0	V
V_{IL}	Maximum Low-Level Input Voltage			0.8	0.8	0.8	V
V_{OH}	Minimum High-Level Output Voltage	V_{IN} = V_{IH} or V_{IL} I_O = -20 µA I_O = -4 mA	V_{CC} 4.2	V_{CC} - 0.1 3.98	V_{CC} - 0.1 3.84	V_{CC} - 0.1 3.7	V
V_{OL}	Maximum Low-Level Output Voltage	V_{IN}= V_{IH} or V_{IL} I_O = 20 µA I_O = 4 mA I_O = 8 mA	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND		±0.1	±1.0	±1.0	µA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND I_{OUT} = 0 µA		8.0	80.0	160.0	µA

AC Electrical Characteristics (Input t_r, $t_f \leq 2$ ns), AHCT138

Sym	Parameter	Conditions•	74AHCT T_A = 25°C VCC - 5.0V	74AHCT T_A = -40°C to +85°C V_{CC} = 5.0V ±10%	54AHCT T_A = -55°C to +125°C V_{CC} = 5.0V ±10%	Unit
			Typ	Guaranteed Limits		
t_{PLH}	Maximum Propagation Delay, A, B, C to any Y	C_L = 50 pF	12	20	24	ns
t_{PHL}			12	20	24	
t_{PLH}	Maximum Propagation Delay, G1 to any Y		10	17	20	ns
t_{PHL}			10	17	20	
t_{PLH}	Maximum Propagation Delay, $\overline{G2A}$ or $\overline{G2B}$ to any Y		10	17	20	ns
t_{PHL}			10	17	20	
C_{IN}	Maximum Input Capacitance		5			pF
C_{PD}	Power Dissipation Capacitance*		50			pF

*C_{PD} determines the no-load dynamic power consumption: $P_D = C_{PD}\ V_{CC}^2\ f + I_{CC}\ V_{CC}$
•For AC switching test circuits and timing waveforms see section 2.