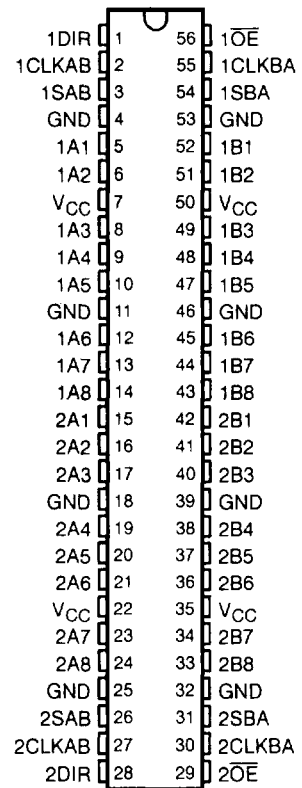


# SN54ABT16646, SN74ABT16646 16-BIT BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

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- Members of the Texas Instruments *Widebus™* Family
- State-of-the-Art *EPIC-IIB™* BICMOS Design Significantly Reduces Power Dissipation
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Typical  $V_{OLP}$  (Output Ground Bounce)  $< 1\text{ V}$  at  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$
- Distributed  $V_{CC}$  and GND Pin Configuration Minimizes High-Speed Switching Noise
- Flow-Through Architecture Optimizes PCB Layout
- High-Drive Outputs ( $-32\text{-mA } I_{OH}$ ,  $64\text{-mA } I_{OL}$ )
- Package Options Include Plastic 300-mil Shrink Small-Outline (DL) Package and 380-mil Fine-Pitch Ceramic Flat (WD) Package Using 25-mil Center-to-Center Spacings

SN54ABT16646 . . . WD PACKAGE  
SN74ABT16646 . . . DL PACKAGE  
(TOP VIEW)



## description

The 'ABT16646 consists of bus transceiver circuits, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or from the internal registers.

These devices can be used as two 8-bit transceivers or one 16-bit transceiver. Data on the A or B bus is clocked into the registers on the low-to-high transition of the appropriate clock (CLKAB or CLKBA) input. Figure 1 illustrates the four fundamental bus-management functions that can be performed with the 'ABT16646.

Output-enable ( $\overline{OE}$ ) and direction-control (DIR) inputs are provided to control the transceiver functions. In the transceiver mode, data present at the high-impedance port may be stored in either register or in both. The select-control (SAB and SBA) inputs can multiplex stored and real-time (transparent mode) data. The circuitry used for select control eliminates the typical decoding glitch that occurs in a multiplexer during the transition between stored and real-time data. The direction control (DIR) determines which bus receives data when  $\overline{OE}$  is low. In the isolation mode ( $\overline{OE}$  high), A data may be stored in one register and/or B data may be stored in the other register.

When an output function is disabled, the input function is still enabled and may be used to store and transmit data. Only one of the two buses, A or B, may be driven at a time.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74ABT16646 is available in TI's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

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PRODUCTION DATA Information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



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**description (continued)**

The SN54ABT16646 is characterized for operation over the full military temperature range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ .  
 The SN74ABT16646 is characterized for operation from  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ .

**FUNCTION TABLE**

INPUTS						DATA I/O		OPERATION OR FUNCTION
$\overline{\text{OE}}$	DIR	CLKAB	CLKBA	SAB	SBA	A1 THRU A8	B1 THRU B8	
X	X	↑	X	X	X	Input	Unspecified†	Store A, B unspecified†
X	X	X	↑	X	X	Unspecified†	Input	Store B, A unspecified†
H	X	↑	↑	X	X	Input	Input	Store A and B data
H	X	H or L	H or L	X	X	Input disabled	Input disabled	Isolation, hold storage
L	L	X	X	X	L	Output	Input	Real-time B data to A bus
L	L	X	H or L	X	H	Output	Input	Stored B data to A bus
L	H	X	X	L	X	Input	Output	Real-time A data to B bus
L	H	H or L	X	H	X	Input	Output	Stored A data to B bus

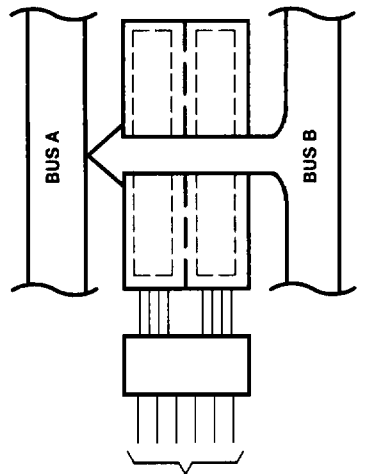
† The data output functions may be enabled or disabled by various signals at the  $\overline{\text{OE}}$  and DIR inputs. Data input functions are always enabled; i.e., data at the bus pins will be stored on every low-to-high transition of the clock inputs.



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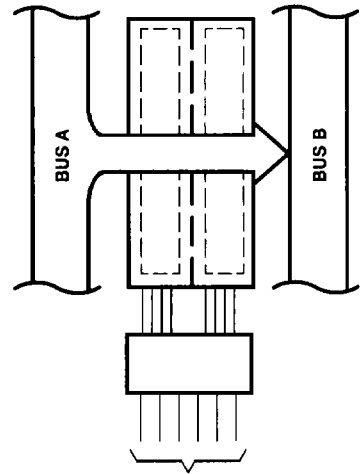
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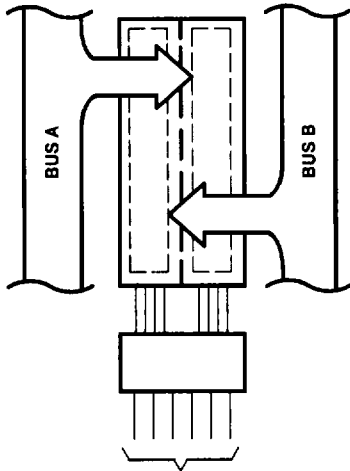
$\overline{OE}$	DIR	CLKAB	CLKBA	SAB	SBA
L	L	X	X	X	L

**REAL-TIME TRANSFER  
 BUS B TO BUS A**



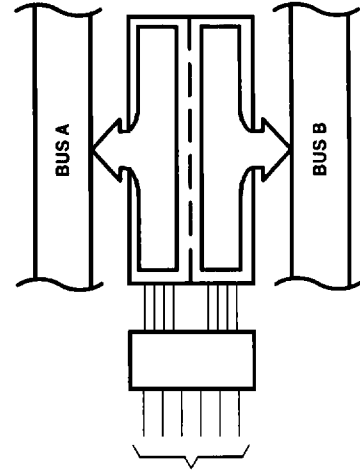
$\overline{OE}$	DIR	CLKAB	CLKBA	SAB	SBA
L	H	X	X	L	X

**REAL-TIME TRANSFER  
 BUS A TO BUS B**



$\overline{OE}$	DIR	CLKAB	CLKBA	SAB	SBA
X	X	↑	X	X	X
X	X	X	↑	X	X
H	X	↑	↑	X	X

**STORAGE FROM  
 A, B, OR A AND B**



$\overline{OE}$	DIR	CLKAB	CLKBA	SAB	SBA
L	L	X	L	X	H
L	H	L	X	H	X

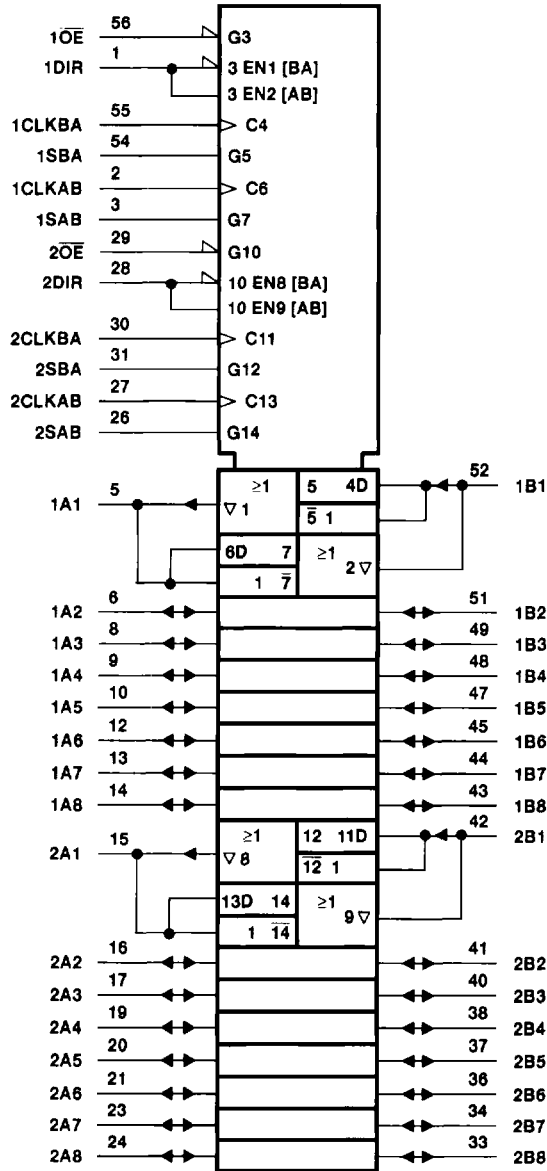
**TRANSFER STORED DATA  
 TO A AND/OR B**

**Figure 1. Bus-Management Functions**

**SN54ABT16646, SN74ABT16646**  
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logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

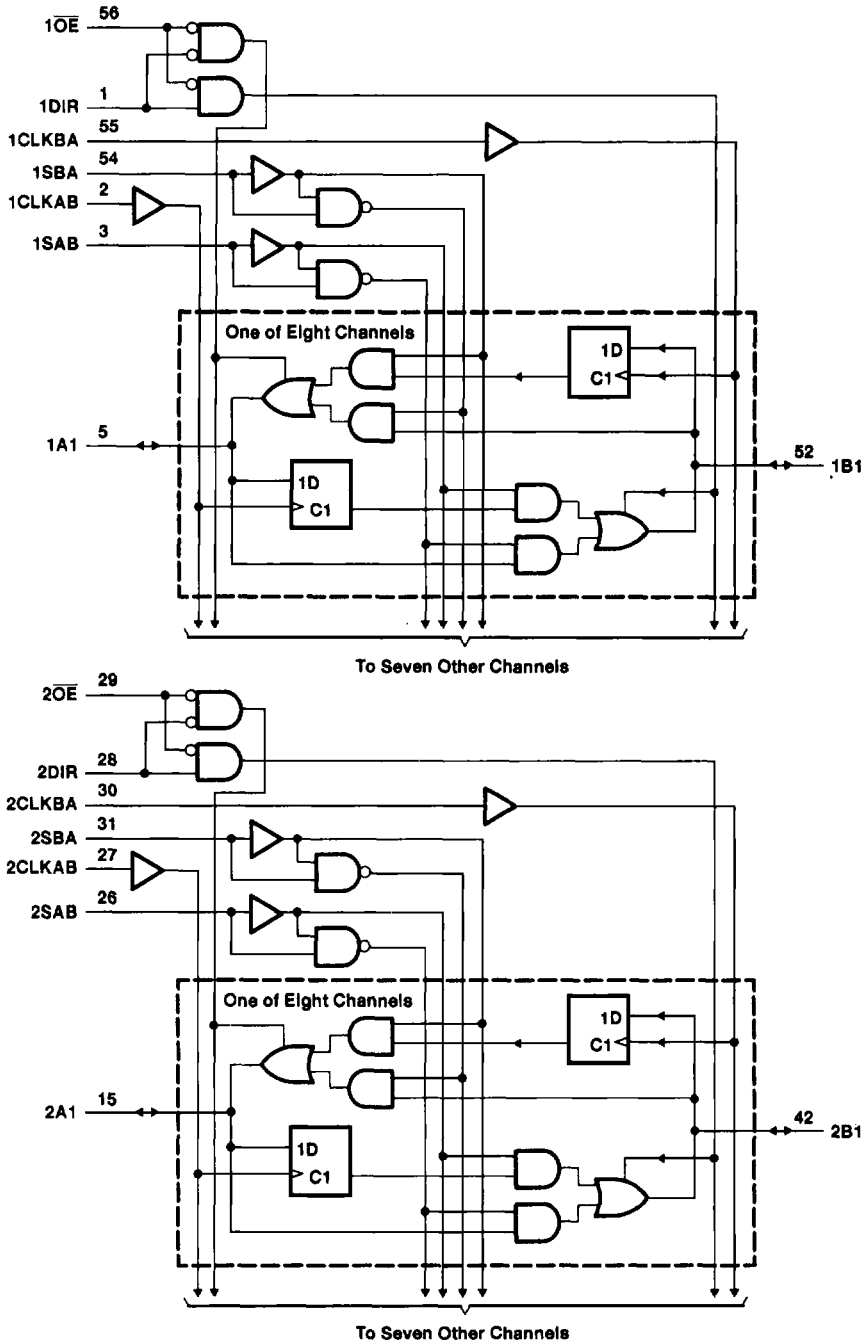


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logic diagram (positive logic)



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## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ .....	-0.5 V to 7 V
Input voltage range, $V_I$ (except I/O ports) (see Note 1) .....	-0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, $V_O$ .....	-0.5 V to 5.5 V
Current into any output in the low state, $I_O$ : SN54ABT16646 .....	96 mA
SN74ABT16646 .....	128 mA
Input clamp current, $I_{IK}$ ( $V_I < 0$ ) .....	-18 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ ) .....	-50 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air) (see Note 2): DL package .....	1.4 W
Storage temperature range .....	-65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.  
 2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note in the 1994 *ABT Advanced BiCMOS Technology Data Book*, literature number SCBD002B.

## recommended operating conditions (see Note 3)

		SN54ABT16646		SN74ABT16646		UNIT
		MIN	MAX	MIN	MAX	
$V_{CC}$	Supply voltage	4.5	5.5	4.5	5.5	V
$V_{IH}$	High-level input voltage	2		2		V
$V_{IL}$	Low-level input voltage		0.8		0.8	V
$V_I$	Input voltage	0	$V_{CC}$	0	$V_{CC}$	V
$I_{OH}$	High-level output current		-24		-32	mA
$I_{OL}$	Low-level output current		48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10	10	ns/V
$T_A$	Operating free-air temperature	-55	125	-40	85	°C

NOTE 3: Unused or floating pins (input or I/O) must be held high or low.



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**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER	TEST CONDITIONS	T <sub>A</sub> = 25°C			SN54ABT16646		SN74ABT16646		UNIT	
		MIN	TYP†	MAX	MIN	MAX	MIN	MAX		
V <sub>IK</sub>	V <sub>CC</sub> = 4.5 V, I <sub>I</sub> = -18 mA			-1.2		-1.2		-1.2	V	
V <sub>OH</sub>	V <sub>CC</sub> = 4.5 V, I <sub>OH</sub> = -3 mA	2.5			2.5			2.5	V	
	V <sub>CC</sub> = 5 V, I <sub>OH</sub> = -3 mA	3			3			3		
	V <sub>CC</sub> = 4.5 V				2			2		
V <sub>OL</sub>	V <sub>CC</sub> = 4.5 V	I <sub>OL</sub> = 48 mA		0.55		0.55			V	
		I <sub>OL</sub> = 64 mA		0.55*				0.55		
I <sub>I</sub>	Control inputs	V <sub>CC</sub> = 5.5 V, V <sub>I</sub> = V <sub>CC</sub> or GND		±1		±1		±1	µA	
	A or B ports	V <sub>CC</sub> = 5.5 V, V <sub>I</sub> = V <sub>CC</sub> or GND		±20		±20		±20		
I <sub>OZH</sub> ‡	V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 2.7 V		10		10		10	µA		
I <sub>OZL</sub> ‡	V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 0.5 V		-10		-10		-10	µA		
I <sub>off</sub>	V <sub>CC</sub> = 0, V <sub>I</sub> or V <sub>O</sub> ≤ 4.5 V			±100				±100	µA	
I <sub>CEX</sub>	Outputs high	V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 5.5 V		50		50		50	µA	
I <sub>O</sub> §		V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 2.5 V	-50	-100	-180	-50	-180	-50	-180	mA
I <sub>CC</sub>	A or B ports	V <sub>CC</sub> = 5.5 V, I <sub>O</sub> = 0, V <sub>I</sub> = V <sub>CC</sub> or GND	Outputs high		2		2		2	mA
			Outputs low		32		32		32	
			Outputs disabled		2		2		2	
ΔI <sub>CC</sub> ¶	Data inputs	V <sub>CC</sub> = 5.5 V, One input at 3.4 V, Other inputs at V <sub>CC</sub> or GND	Outputs enabled		50		50		50	µA
			Outputs disabled		50		50		50	
	Control inputs	V <sub>CC</sub> = 5.5 V, One input at 3.4 V, Other inputs at V <sub>CC</sub> or GND		50		50		50		
C <sub>i</sub>	Control inputs	V <sub>I</sub> = 2.5 V or 0.5 V		4					pF	
C <sub>io</sub>	A or B ports	V <sub>O</sub> = 2.5 V or 0.5 V		8					pF	

\* On products compliant to MIL-STD-883, Class B, this parameter does not apply.

† All typical values are at V<sub>CC</sub> = 5 V.

‡ The parameters I<sub>OZH</sub> and I<sub>OZL</sub> include the input leakage current.

§ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V<sub>CC</sub> or GND.

**timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 2)**

		V <sub>CC</sub> = 5 V, T <sub>A</sub> = 25°C		SN54ABT16646		SN74ABT16646		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
f <sub>clock</sub>	Clock frequency	0	125	0	125	0	125	MHz
t <sub>w</sub>	Pulse duration, CLK high or low	4.3		4.3		4.3		ns
t <sub>SU</sub>	Setup time, A or B before CLKAB↑ or CLKBA↑	3		4		3		ns
t <sub>H</sub>	Hold time, A or B after CLKAB↑ or CLKBA↑	0		0.5		0		ns



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switching characteristics over recommended ranges of supply voltage and operating free-air temperature,  $C_L = 50$  pF (unless otherwise noted) (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 5$ V, $T_A = 25^\circ$ C			SN54ABT16646		SN74ABT16646		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
$f_{max}$			125			125		125		MHz
$t_{PLH}$	CLKBA or CLKAB	A or B	1.5	3.1	4	1	5	1.5	4.9	ns
$t_{PHL}$			1.5	3.2	4.1	1	5	1.5	4.7	
$t_{PLH}$	A or B	B or A	1	2.3	3.2	0.6	4	1	3.9	ns
$t_{PHL}$			1	3	4.1	0.6	4.9	1	4.6	
$t_{PLH}$	SAB or SBA†	B or A	1	2.9	4.3	0.6	5.3	1	5	ns
$t_{PHL}$			1	3.1	4.3	0.6	5.3	1	5	
$t_{PZH}$	$\overline{OE}$	A or B	1	3.4	4.6	0.6	5.9	1	5.5	ns
$t_{PZL}$			1.5	3.5	4.9	1	6	1.5	5.7	
$t_{PHZ}$	$\overline{OE}$	A or B	1.5	3.9	4.9	1	6.4	1.5	5.4	ns
$t_{PLZ}$			1.5	3.1	4.1	1	4.7	1.5	4.5	
$t_{PZH}$	DIR	A or B	1	3.2	4.5	0.6	5.8	1	5.4	ns
$t_{PZL}$			1.5	3.4	4.8	1	6.7	1.5	5.6	
$t_{PHZ}$	DIR	A or B	2	4.2	5.7	1.2	7.1	2	6.7	ns
$t_{PLZ}$			1.5	3.6	5.1	1	6.2	1.5	5.9	

† These parameters are measured with the internal output state of the storage register opposite to that of the bus input.

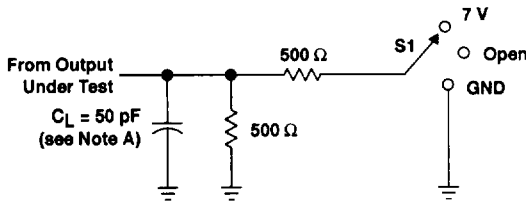




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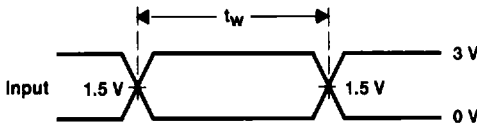
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**PARAMETER MEASUREMENT INFORMATION**

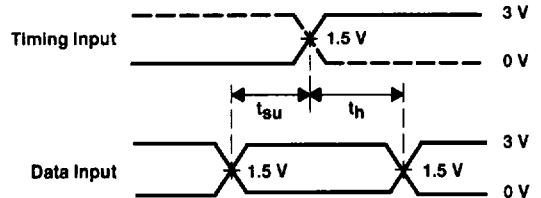


**LOAD CIRCUIT FOR OUTPUTS**

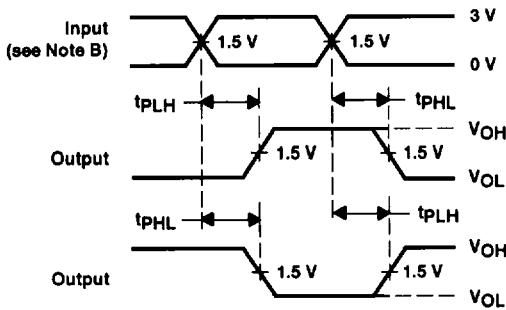
TEST	S1
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	7 V
$t_{PHZ}/t_{PZH}$	Open



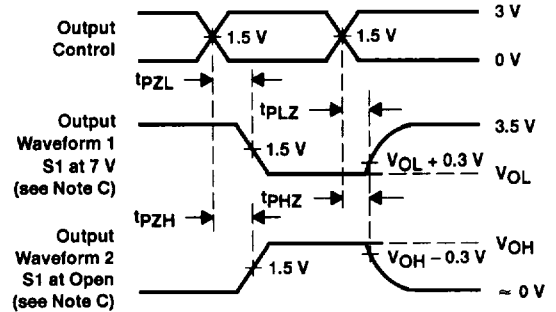
**VOLTAGE WAVEFORMS**  
PULSE DURATION



**VOLTAGE WAVEFORMS**  
SETUP AND HOLD TIMES



**VOLTAGE WAVEFORMS**  
PROPAGATION DELAY TIMES  
INVERTING AND NONINVERTING OUTPUTS



**VOLTAGE WAVEFORMS**  
ENABLE AND DISABLE TIMES  
LOW- AND HIGH-LEVEL ENABLING

- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10$  MHz,  $Z_O = 50 \Omega$ ,  $t_r \leq 2.5$  ns,  $t_f \leq 2.5$  ns.  
 C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
 D. The outputs are measured one at a time with one transition per measurement.

**Figure 2. Load Circuit and Voltage Waveforms**