IH5040-IH5047

JAN QUALIFIED High Reliability High-Level CMOS Analog Switch

GENERAL DESCRIPTION

The IH5040 family of solid state analog switches use an improved, high voltage CMOS monolithic technology. These devices provide ease-of-use and performance advantages not previously available from solid state switches. This improved CMOS technology provides input overvoltage capability to ±25 volts without damage to the device, and destructive latch-up has been eliminated. Early CMOS switches were destroyed when power supplies were removed with an input signal present. The IH5040 CMOS technology has eliminated this serious problem.

Key performance advantages of the 5040 series are TTL compatibility and ultra low-power operation. The quiescent current requirement is less than 1μA. Also, the 5040 guarantees Break-Before-Make switching, accomplished by extending the t_{on} time (300ns TYP.) so that it exceeds t_{off} time (200ns TYP.). This insures that an ON channel will be turned OFF before an OFF channel can turn ON. The need for external logic required to avoid channel to channel shorting during switching is eliminated.

Many of the 5040 series improve upon and are pin-for-pin and electrical replacements for other solid state switches.

FEATURES

- **Switches Greater Than 20Vpp Signals With ±15V Supplies**
- **Quiescent Current Less Than 1μA**
- **Overvoltage Protection to ±25V**
- **Break-Before-Make Switching t_{off} 200ns, t_{on} 300ns Typical**
- **TTL, DTL, CMOS, PMOS Compatible**
- **Non-Latching With Supply Turn-Off**
- **New DPDT & 4PST Configurations**
- **Complete Monolithic Construction**
- **IH5040–5045 JAN 38510 Approved**

ORDERING INFORMATION

IH5040 M JE

- JE — Package
  - DE – 16-Pin Ceramic DIP (Special Order Only)
  - FD-2 – 14-Pin Flatpak
  - JE – 16-Pin CERDIP
  - Y – 16-Pin S.O. (IH5043 only)
- M — Temperature Range
  - M – Military (−55°C to +125°C)
- IH5040 — Basic Part Number

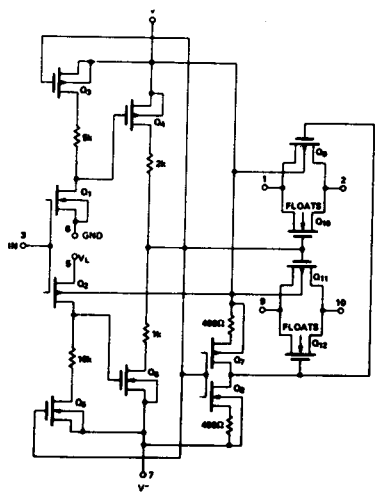

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Figure 1: Functional Driver, Typical Driver, Gate — IH5042

FUNCTIONAL DESCRIPTION

INTERSIL Part No.	Type	$r_{DS(on)}$	Pin for Pin Compatible
IH5040	SPST	75Ω	HI5040/DG5040
IH5041	Dual SPST	75Ω	HI5041/DG5041
IH5042	SPDT	75Ω	HI5042/DG5042
IH5043	Dual SPDT	75Ω	HI5043/DG5043
IH5044	DPST	75Ω	HI5044/DG5044
IH5045	Dual DPST	75Ω	HI5045/DG5045
IH5046	DPDT	75Ω	HI5046
IH5047	4PST	75Ω	HI5047

NOTE 1. See Switching State diagrams for applicable package equivalency.

ABSOLUTE MAXIMUM RATINGS

V^+-V^- ..... <36V
V^+-V_D ..... <30V
V_D-V^- ..... <30V
V_D-V_S ..... < ±22V
V_L-V^- ..... <33V
V_L-V_{IN} ..... <30V
V_L-GND ..... <20V
V_{IN}-GND ..... <20V

Current (Any Terminal) ..... <30mA
Storage Temperature ..... −65°C to +150°C
Operating Temperature
M ..... −55°C to +125°C
Lead Temperature (Soldering, 10sec) ..... 300°C
Power Dissipation 450mW
(All Leads Soldered to a P.C. Board)
Derate 6mW/°C Above 70°C

NOTE: *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

ELECTRICAL CHARACTERISTICS (@ 25°C, V^+ = +15V, V^- = −15V, V_L = +5V)

Per Channel		Test Conditions	Min/Max Limits			Units
			Military			
Symbol	Characteristic		−55°C	+25°C	+125°C	
$I_{IN(ON)}$	Input Logic Current	V_{IN} = 2.4V	±1	±1	10	µA
$I_{IN(OFF)}$	Input Logic Current	V_{IN} = 0.8V	±1	±1	10	µA
$r_{DS(on)}$	Drain-Source On Resistance	I_S = 10mA V_{ANALOG} = −10V to +10V	75	75	150	Ω
$\Delta r_{DS(ON)}$	Channel to Channel $r_{DS(ON)}$ Match			25 (typ)		Ω
V_{ANALOG}	Min. Analog Signal Handling Capability			±11 (typ)		V
$I_{D(OFF)}$/ $I_{S(OFF)}$	Switch OFF Leakage Current	V_{ANALOG} = −10V to +10V		±1	100	nA
$I_{D(ON)}$ + $I_{S(ON)}$	Switch On Leakage Current	V_D = V_S = −10V to +10V		±2	200	nA
t_{on}	Switch "ON" Time	R_L = 1kΩ, V_{ANALOG} = −10V to +10V See Fig. 3		1000		ns
t_{off}	Switch "OFF" Time	R_L = 1kΩ, V_{ANALOG} = −10V to +10V See Fig. 3		500		ns
$Q_{(INJ.)}$	Charge Injection	See Fig. 3		15 (typ)		mV
OIRR	Min. Off Isolation Rejection Ratio	f = 1MHz, R_L = 100Ω, C_L ≤ 5pF See Fig. 5		54 (typ)		dB
I^+_Q	V^+ Power Supply Quiescent Current		±1	±1	10	µA
I^-_Q	V^- Power Supply Quiescent Current	V^+ = +15V, V^- = −15V, V_L = +5V	±1	±1	10	µA
I^-_{LQ}	+5V Supply Quiescent Current		±1	±1	10	µA
I_{GND}	Gnd Supply Quiescent Current		±1	1	10	µA
CCRR	Min. Channel to Channel Cross Coupling Rejection Ratio	One Channel Off; Any Other Channel Switches as per Fig. 6		54 (typ)		dB

Note: Typical values are for design aid only, not guaranteed and not subject to production testing.

IH5040-IH5047

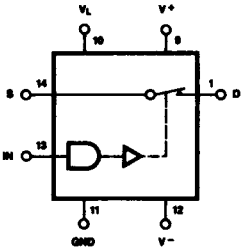
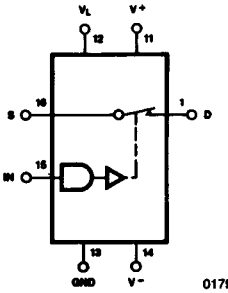
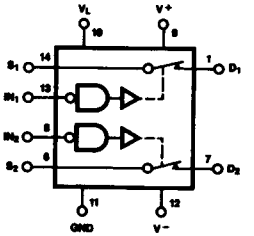
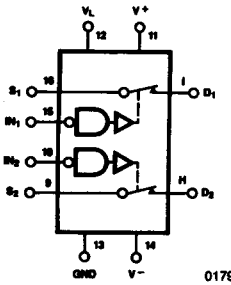
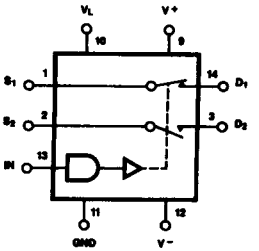
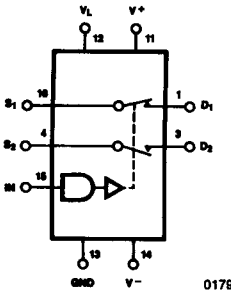
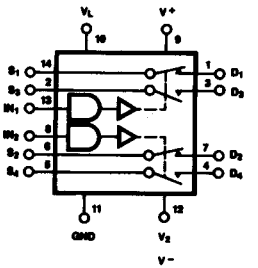
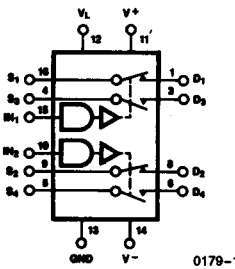
SWITCH STATES ARE FOR LOGIC "1" INPUT	(OUTLINE DWG FD-2)	(OUTLINE DWGS DE, JE)
SPST IH5040 ($r_{DS(on)}$ <75Ω)	 0179-2	 0179-3
DUAL SPST IH5041 ($r_{DS(on)}$ <75Ω)	 0179-4	 0179-5
SPDT IH5042 ($r_{DS(on)}$ <75Ω)	 0179-7	 0179-8
DUAL SPDT IH5043 ($r_{DS(on)}$ <75Ω)	 0179-10	 0179-11

Figure 2: Switching State Diagrams

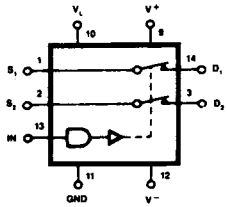
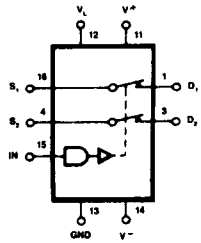
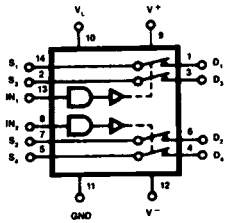
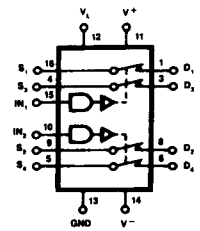
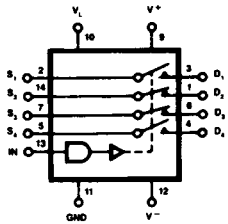
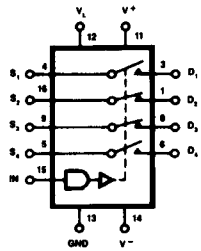
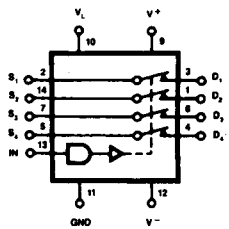
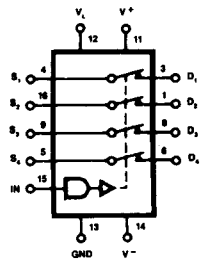
SWITCH STATES ARE FOR LOGIC "1" INPUT	(OUTLINE DWG FD-2)	(OUTLINE DWGS DE, JE)
DPST IH5044 ($r_{DS(on)}$ <75Ω)	 0179-12	 0179-13
DUAL DPST IH5045 ($r_{DS(on)}$ <75Ω)	 0179-15	**(DG185 EQUIVALENT)**  0179-16
DPDT IH5046 ($r_{DS(ON)}$ <75Ω)	 0179-17	 0179-18
4PST IH5047 ($r_{DS\ (ON)}$ <75Ω)	 0179-19	 0179-20

Figure 2: Switching State Diagrams (Cont.)

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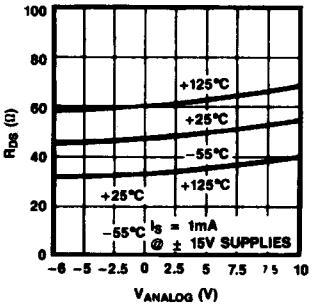
TYPICAL PERFORMANCE CHARACTERISTICS (Per Channel)

$R_{DS(on)}$ vs V_{ANALOG} SIGNAL



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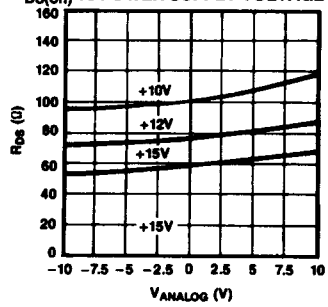
$R_{DS(on)}$ vs POWER SUPPLY VOLTAGE



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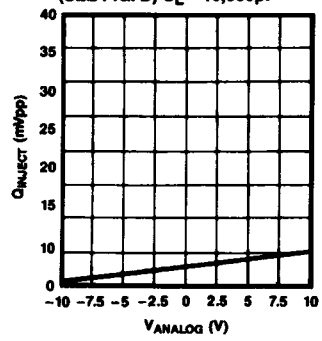
CHARGE INJECTION vs V_{ANALOG} (SEE FIG. B) C_L = 10,000pF



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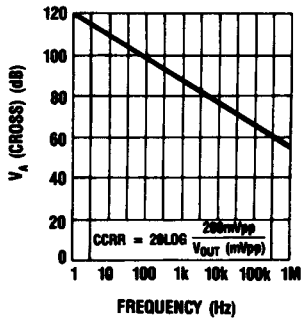

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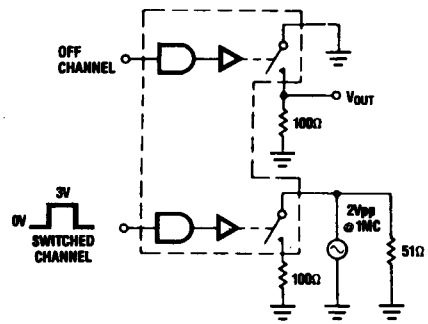

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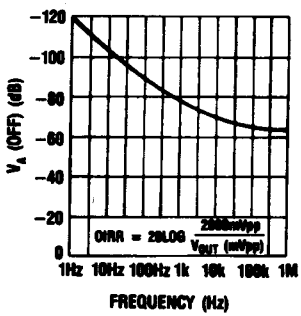

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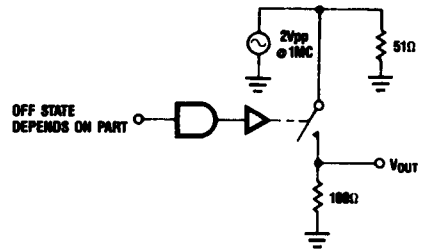

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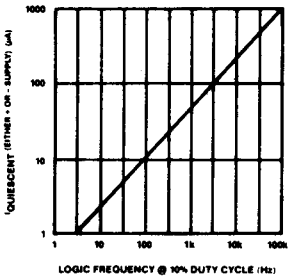
TYPICAL PERFORMANCE CHARACTERISTICS (CONT.)

POWER SUPPLY QUIESCENT CURRENT vs LOGIC FREQUENCY RATE



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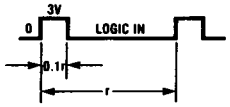

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TEST CIRCUITS

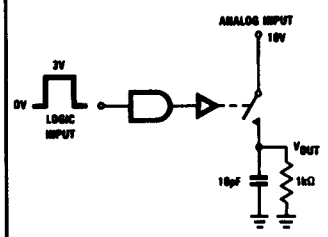

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Figure 3

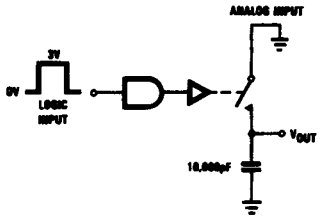

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Figure 4

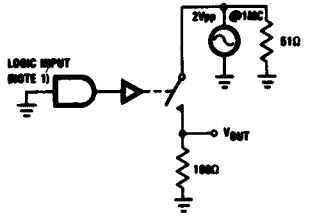

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Figure 5

NOTE 1: Some channels are turned on by high "1" logic inputs and other channels are turned on by low "0" inputs; however 0.8V to 2.4V describes the min. range for switching properly. Refer to logic diagrams to see absolute value of logic input required to produce "ON" or "OFF" state.

APPLICATIONS

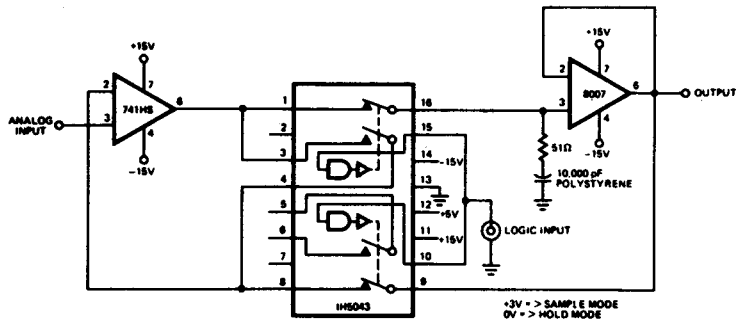

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Figure 6: Improved Sample & Hold Using IH5043

APPLICATIONS (Continued)

EXAMPLE: If $-V_{ANALOG} = -10VDC$ and $+V_{ANALOG} = +10VDC$ then Ladder Legs are switched between $\pm 10VDC$, depending upon state of Logic Strobe.

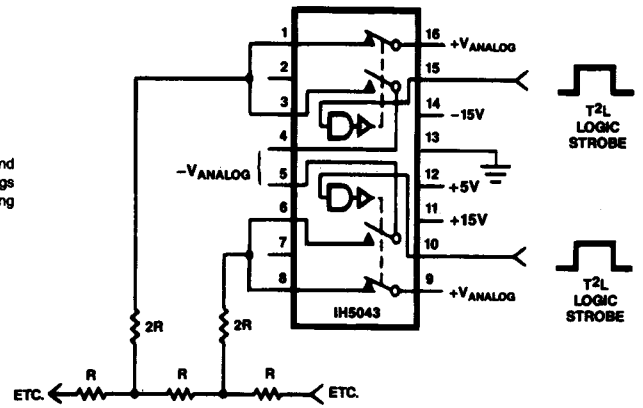

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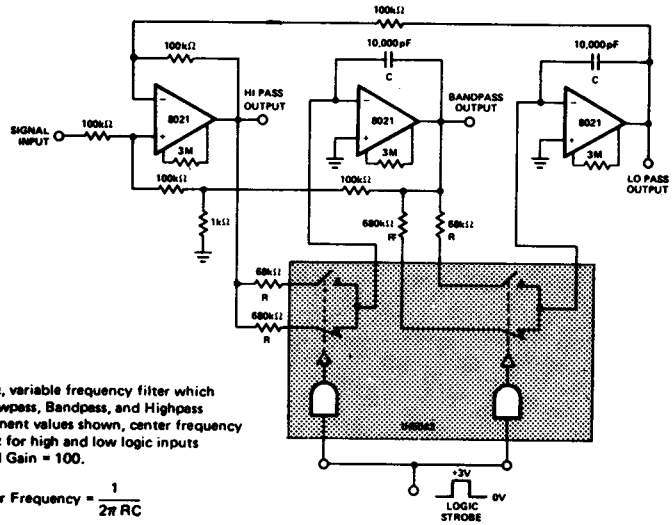
Figure 7: Using the CMOS Switch to Drive an R/2R Ladder Network (2 Legs)



Constant gain, constant Q, variable frequency filter which provides simultaneous Lowpass, Bandpass, and Highpass outputs. With the component values shown, center frequency will be 235Hz and 23.5Hz for high and low logic inputs respectively, Q = 100, and Gain = 100.

$$f_n = \text{Center Frequency} = \frac{1}{2\pi RC}$$

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Figure 8: Digitally Tuned Low Power Active Filter

APPLICATIONS (Continued)

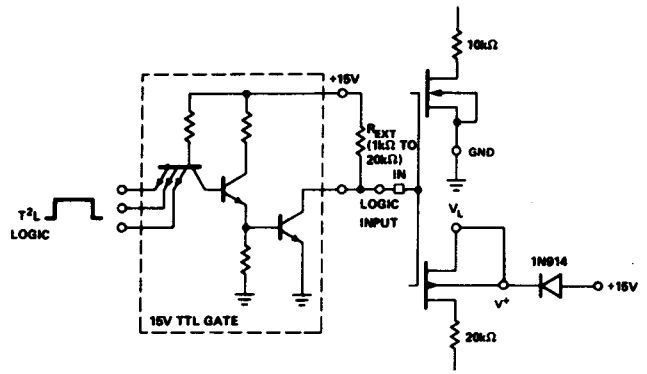

Figure 9: Interfacing with TTL Open Collector Logic (Typ. Example for + 15V Case Shown)

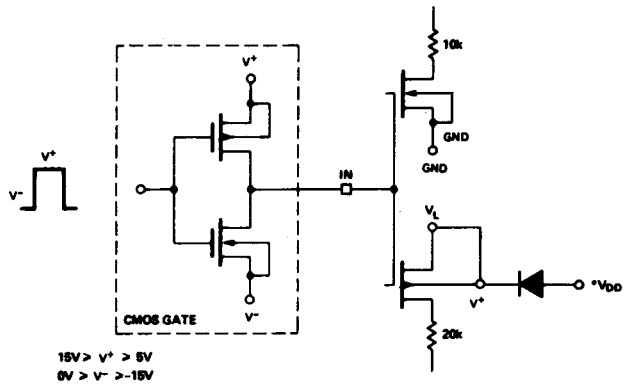

Figure 10: Interfacing with CMOS Logic

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APPLICATIONS (Continued)

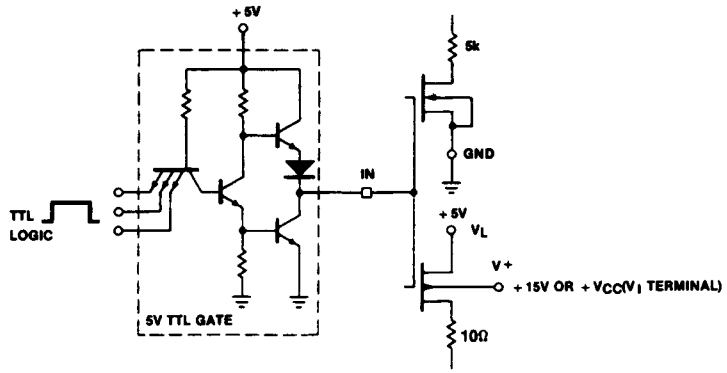

Figure 11: TTL Logic Interface