

- Member of the Texas Instruments *Widebus™* Family
- *EPIC™* (Enhanced-Performance Implanted CMOS) Submicron Process
- *DOC™* (Dynamic Output Control) Circuit Dynamically Changes Output Impedance, Resulting in Noise Reduction Without Speed Degradation
- Dynamic Drive Capability Is Equivalent to Standard Outputs With I_{OH} and I_{OL} of ± 24 mA at 2.5-V V_{CC}
- Over-Voltage-Tolerant Inputs/Outputs Allow Mixed-Voltage-Mode Data Communications
- I_{off} Feature Supports Partial Power-Down Mode Operation
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Package Options Include Plastic Thin Shrink Small-Outline (DGG) and Thin Very Small-Outline (DGV) Packages

description

A Dynamic Output Control (DOC) circuit is implemented, which, during the transition, initially lowers the output impedance to effectively drive the load and, subsequently, raises the impedance to reduce noise. Figure 1 shows typical V_{OL} vs I_{OL} and V_{OH} vs I_{OH} curves to illustrate the output impedance and drive capability of the circuit. At the beginning of the signal transition, the DOC circuit provides a maximum dynamic drive that is equivalent to a high-drive standard-output device. For more information, refer to the TI application reports, *AVC Logic Family Technology and Applications*, literature number SCEA006, and *Dynamic Output Control (DOC™) Circuitry Technology and Applications*, literature number SCEA009.

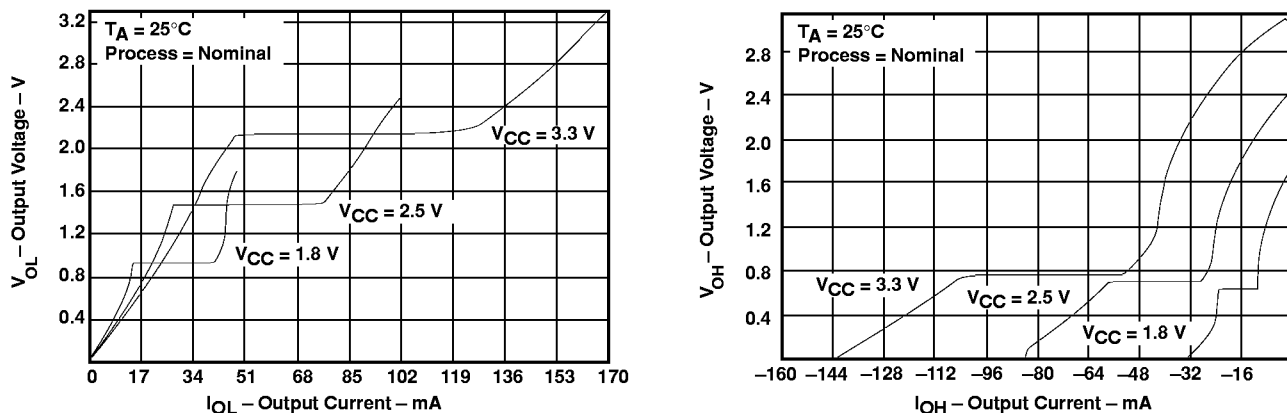


Figure 1. Output Voltage vs Output Current

This 16-bit bus transceiver and register is operational at 1.5-V to 3.6-V V_{CC} , but designed specifically for 1.65-V to 3.6-V V_{CC} operation.

The SN74AVCH16646 can be used as two 8-bit transceivers or one 16-bit transceiver. Data on the A or B bus is clocked into the registers on the low-to-high transition of the appropriate clock (CLKAB or CLKBA) input. Figure 2 illustrates the four fundamental bus-management functions that can be performed with the SN74AVCH16646.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

DOC, EPIC, and Widebus are trademarks of Texas Instruments Incorporated.

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.



SN74AVCH16646

16-BIT BUS TRANSCEIVER AND REGISTER WITH 3-STATE OUTPUTS

SCES182 – DECEMBER 1998

description (continued)

Output-enable (\overline{OE}) and direction-control (DIR) inputs are provided to control the transceiver functions. In the transceiver mode, data present at the high-impedance port can be stored in either register or in both. The select-control (SAB and SBA) inputs can multiplex stored and real-time (transparent mode) data. The circuitry used for select control eliminates the typical decoding glitch that occurs in a multiplexer during the transition between stored and real-time data. DIR determines which bus receives data when \overline{OE} is low. In the isolation mode (\overline{OE} high), A data may be stored in one register and/or B data may be stored in the other register.

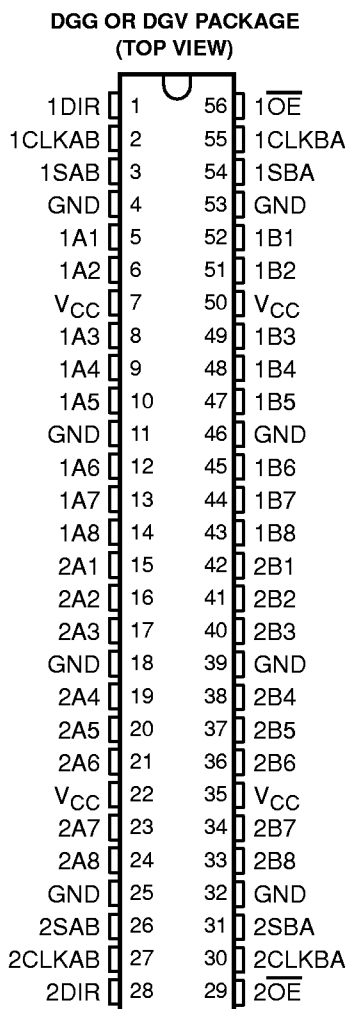
When an output function is disabled, the input function is still enabled and may be used to store and transmit data. Only one of the two buses, A or B, can be driven at a time.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74AVCH16646 is characterized for operation from -40°C to 85°C .

terminal assignments



PRODUCT PREVIEW

SN74AVCH16646
16-BIT BUS TRANSCEIVER AND REGISTER
WITH 3-STATE OUTPUTS

SCES182 – DECEMBER 1998

FUNCTION TABLE

INPUTS						DATA I/Os		OPERATION OR FUNCTION
\overline{OE}	DIR	CLKAB	CLKBA	SAB	SBA	A1–A8	B1–B8	
X	X	↑	X	X	X	Input	Unspecified†	Store A, B unspecified†
X	X	X	↑	X	X	Unspecified†	Input	Store B, A unspecified†
H	X	↑	↑	X	X	Input	Input	Store A and B data
H	X	H or L	H or L	X	X	Input disabled	Input disabled	Isolation, hold storage
L	L	X	X	X	L	Output	Input	Real-time B data to A bus
L	L	X	H or L	X	H	Output	Input	Stored B data to A bus
L	H	X	X	L	X	Input	Output	Real-time A data to B bus
L	H	H or L	X	H	X	Input	Output	Stored A data to B bus

† The data-output functions may be enabled or disabled by various signals at \overline{OE} and DIR. Data-input functions are always enabled; i.e., data at the bus terminals is stored on every low-to-high transition of the clock inputs.

PRODUCT PREVIEW



SN74AVCH16646
16-BIT BUS TRANSCEIVER AND REGISTER
WITH 3-STATE OUTPUTS

SCES182 – DECEMBER 1998

PRODUCT PREVIEW

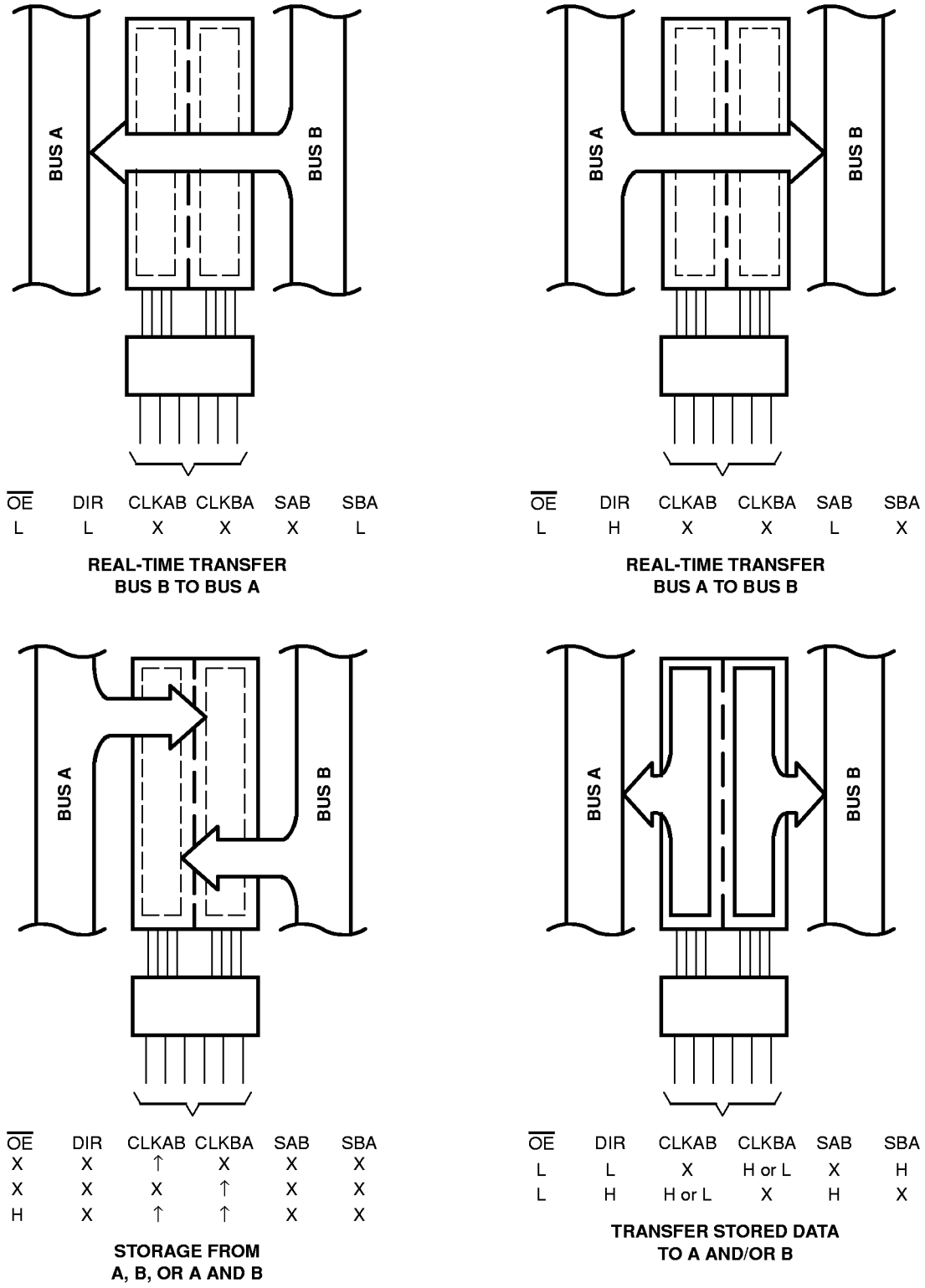
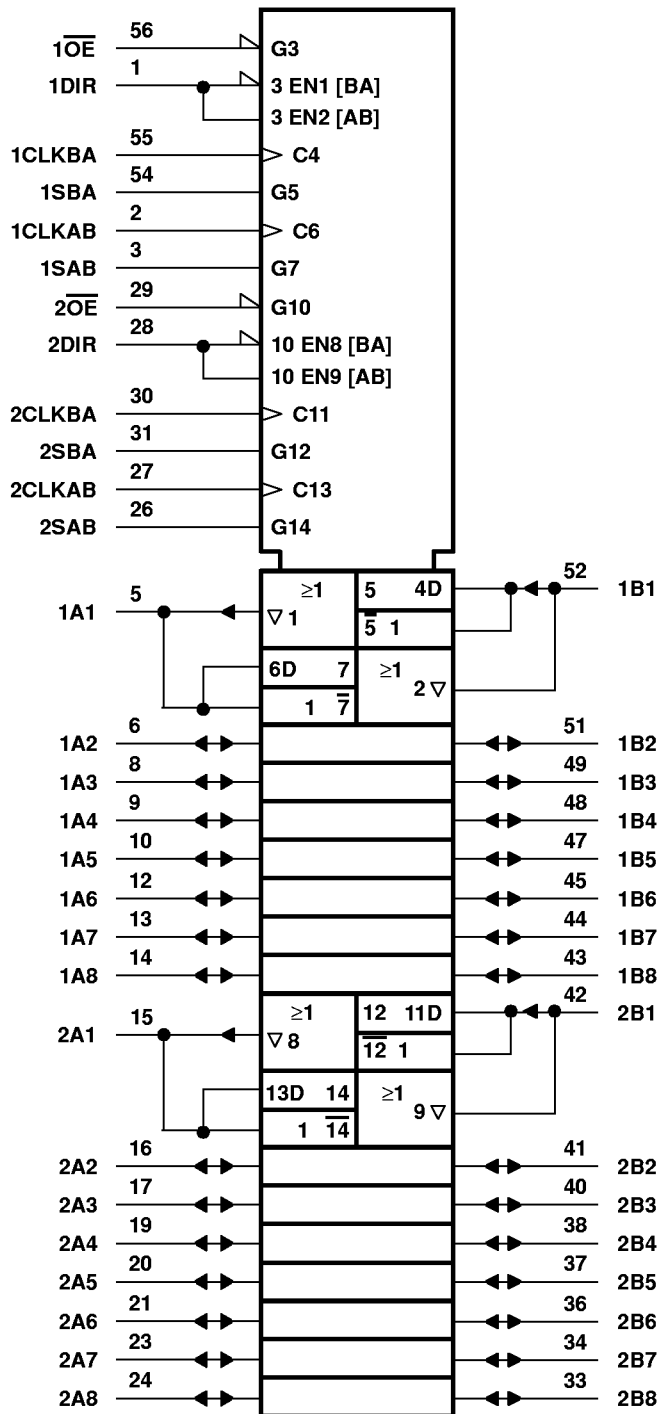


Figure 2. Bus-Management Functions

SN74AVCH16646 16-BIT BUS TRANSCEIVER AND REGISTER WITH 3-STATE OUTPUTS

SCES182 - DECEMBER 1998

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

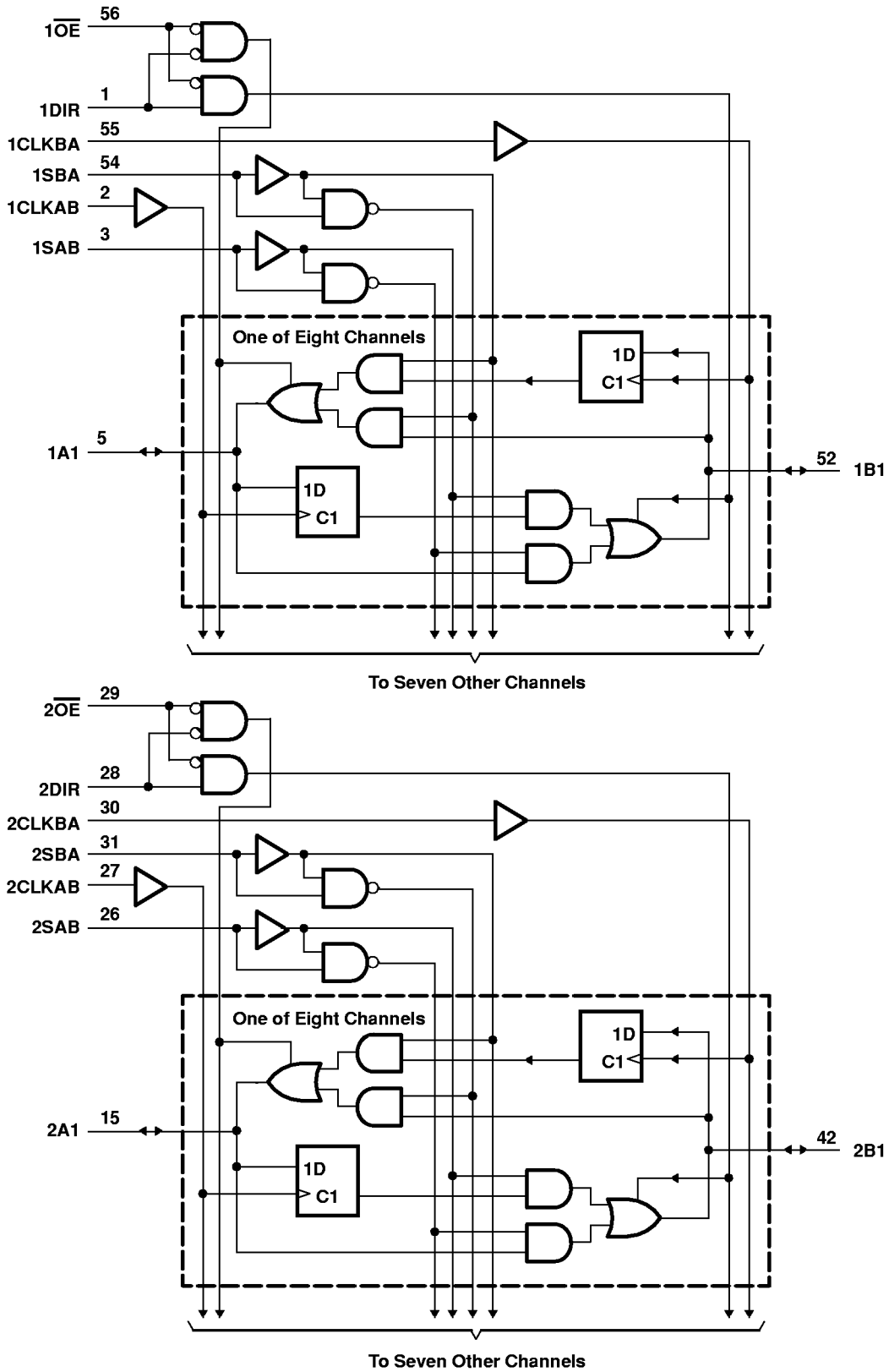
PRODUCT PREVIEW



SN74AVCH16646
16-BIT BUS TRANSCEIVER AND REGISTER
WITH 3-STATE OUTPUTS

SCES182 – DECEMBER 1998

logic diagram (positive logic)



PRODUCT PREVIEW



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

SN74AVCH16646

16-BIT BUS TRANSCEIVER AND REGISTER WITH 3-STATE OUTPUTS

SCES182 – DECEMBER 1998

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	–0.5 V to 4.6 V
Input voltage range, V_I : Except I/O ports (see Note 1)	–0.5 V to 4.6 V
I/O ports (see Notes 1 and 2)	–0.5 V to $V_{CC} + 0.5$ V
Voltage range applied to any output in the high-impedance or power-off state, V_O (see Note 1)	–0.5 V to 4.6 V
Voltage range applied to any output in the high or low state, V_O (see Notes 1 and 2)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	–50 mA
Output clamp current, I_{OK} ($V_O < 0$)	–50 mA
Continuous output current, I_O	±50 mA
Continuous current through each V_{CC} or GND	±100 mA
Package thermal impedance, θ_{JA} (see Note 3): DGG package	81°C/W
DGV package	86°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
 2. The output positive-voltage rating may be exceeded up to 4.6 V maximum if the output current rating is observed.
 3. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 4)

		MIN	MAX	UNIT
V_{CC} Supply voltage	Operating	1.65	3.6	V
	Data retention only	1.2		
V_{IH} High-level input voltage	$V_{CC} = 1.2$ V	V_{CC}		V
	$V_{CC} = 1.65$ V to 1.95 V	$0.65 \times V_{CC}$		
	$V_{CC} = 2.3$ V to 2.7 V	1.7		
	$V_{CC} = 3$ V to 3.6 V	2		
V_{IL} Low-level input voltage	$V_{CC} = 1.2$ V	GND		V
	$V_{CC} = 1.65$ V to 1.95 V	$0.35 \times V_{CC}$		
	$V_{CC} = 2.3$ V to 2.7 V	0.7		
	$V_{CC} = 3$ V to 3.6 V	0.8		
V_I Input voltage		0	3.6	V
V_O Output voltage	Active state	0	V_{CC}	V
	3-state	0	3.6	V
I_{OHS} Static high-level output current‡	$V_{CC} = 1.65$ V to 1.95 V		–4	mA
	$V_{CC} = 2.3$ V to 2.7 V		–8	
	$V_{CC} = 3$ V to 3.6 V		–12	
I_{OLS} Static low-level output current‡	$V_{CC} = 1.65$ V to 1.95 V		4	mA
	$V_{CC} = 2.3$ V to 2.7 V		8	
	$V_{CC} = 3$ V to 3.6 V		12	
$\Delta t/\Delta v$ Input transition rise or fall rate	$V_{CC} = 1.65$ V to 3.6 V		5	ns/V
T_A Operating free-air temperature		–40	85	°C

‡ Dynamic drive capability is equivalent to standard outputs with I_{OH} and I_{OL} of ±24 mA at 2.5-V V_{CC} . See Figure 1 for V_{OL} vs I_{OL} and V_{OH} vs I_{OH} characteristics. Refer to the TI application reports, **AVC Logic Family Technology and Applications**, literature number **SCEA006**, and **Dynamic Output Control (DOC™) Circuitry Technology and Applications**, literature number **SCEA009**.

NOTE 4: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, **Implications of Slow or Floating CMOS Inputs**, literature number **SCBA004**.

PRODUCT PREVIEW



SN74AVCH16646

16-BIT BUS TRANSCEIVER AND REGISTER

WITH 3-STATE OUTPUTS

SCES182 – DECEMBER 1998

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V _{CC}	MIN	TYP†	MAX	UNIT
V _{OH}		I _{OHS} = -100 μA	1.65 V to 3.6 V	V _{CC} -0.2			V
		I _{OHS} = -4 mA, V _{IH} = 1.07 V	1.65 V	1.2			
		I _{OHS} = -8 mA, V _{IH} = 1.7 V	2.3 V	1.75			
		I _{OHS} = -12 mA, V _{IH} = 2 V	3 V	2.3			
V _{OL}		I _{OLS} = 100 μA	1.65 V to 3.6 V			0.2	V
		I _{OLS} = 4 mA, V _{IL} = 0.57 V	1.65 V			0.45	
		I _{OLS} = 8 mA, V _{IL} = 0.7 V	2.3 V			0.55	
		I _{OLS} = 12 mA, V _{IL} = 0.8 V	3 V			0.7	
I _I	Control inputs	V _I = V _{CC} or GND	3.6 V			±2.5	μA
I _{BHL} ‡		V _I = 0.57 V	1.65 V	25			μA
		V _I = 0.7 V	2.3 V	45			
		V _I = 0.8 V	3 V	75			
I _{BHH} §		V _I = 1.07 V	1.65 V	-25			μA
		V _I = 1.7 V	2.3 V	-45			
		V _I = 2 V	3 V	-75			
I _{BHLO} ¶		V _I = 0 to V _{CC}	1.95 V	200			μA
			2.7 V	300			
			3.6 V	500			
I _{BHHO} #		V _I = 0 to V _{CC}	1.95 V	-200			μA
			2.7 V	-300			
			3.6 V	-500			
I _{off}		V _I = 0 or 3.6 V	0			±10	μA
I _{OZ}		V _O = V _{CC} or GND	3.6 V			±12.5	μA
I _{CC}		V _I = V _{CC} or GND, I _O = 0	3.6 V			40	μA
C _i	Control inputs	V _I = V _{CC} or GND	2.5 V	3			pF
			3.3 V	3			
C _{io}	A or B ports	V _O = V _{CC} or GND	2.5 V	10			pF
			3.3 V	10			

† Typical values are measured at T_A = 25°C.

‡ The bus-hold circuit can sink at least the minimum low sustaining current at V_{IL} max. I_{BHL} should be measured after lowering V_{IN} to GND and then raising it to V_{IL} max.

§ The bus-hold circuit can source at least the minimum high sustaining current at V_{IH} min. I_{BHH} should be measured after raising V_{IN} to V_{CC} and then lowering it to V_{IH} min.

¶ An external driver must source at least I_{BHLO} to switch this node from low to high.

An external driver must sink at least I_{BHHO} to switch this node from high to low.

|| For I/O ports, the parameter I_{OZ} includes the input leakage current.

PRODUCT PREVIEW



SN74AVCH16646
16-BIT BUS TRANSCEIVER AND REGISTER
WITH 3-STATE OUTPUTS

SCES182 – DECEMBER 1998

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figures 4 through 6)

		$V_{CC} = 1.8\text{ V}$ $\pm 0.15\text{ V}$		$V_{CC} = 2.5\text{ V}$ $\pm 0.2\text{ V}$		$V_{CC} = 3.3\text{ V}$ $\pm 0.3\text{ V}$		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency							MHz
t_w	Pulse duration	CLKAB or CLKBA high or low						ns
t_{su}	Setup time	A before CLKAB \uparrow or B before CLKBA \uparrow						ns
t_h	Hold time	A after CLKAB \uparrow or B after CLKBA \uparrow						ns

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 3 through 6)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 1.5\text{ V}$		$V_{CC} = 1.8\text{ V}$ $\pm 0.15\text{ V}$		$V_{CC} = 2.5\text{ V}$ $\pm 0.2\text{ V}$		$V_{CC} = 3.3\text{ V}$ $\pm 0.3\text{ V}$		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f_{max}											MHz
t_{pd}	A or B	B or A									ns
	CLKAB or CLKBA	A or B									
	SAB or SBA										
t_{en}	$\overline{\text{OE}}$	A or B									ns
t_{dis}	$\overline{\text{OE}}$	A or B									ns
t_{en}	DIR	A or B									ns
t_{dis}	DIR	A or B									ns

operating characteristics, $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	$V_{CC} = 1.8\text{ V}$	$V_{CC} = 2.5\text{ V}$	$V_{CC} = 3.3\text{ V}$	UNIT	
			TYP	TYP	TYP		
C_{pd}	Power dissipation capacitance	Outputs enabled	$C_L = 0, \quad f = 10\text{ MHz}$				pF
	Outputs disabled						

PRODUCT PREVIEW

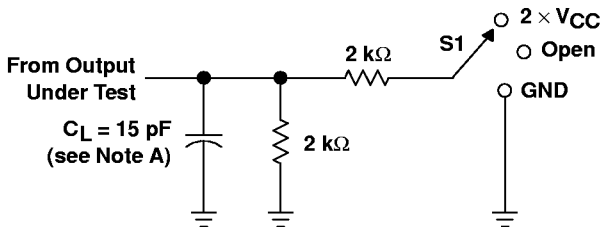


SN74AVCH16646
16-BIT BUS TRANSCEIVER AND REGISTER
WITH 3-STATE OUTPUTS

SCES182 – DECEMBER 1998

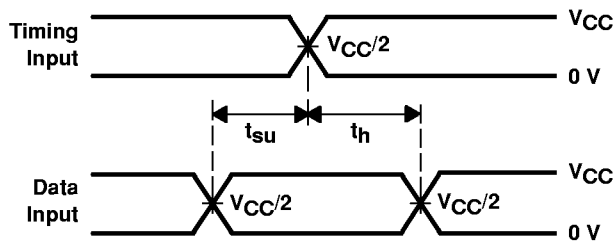
PARAMETER MEASUREMENT INFORMATION

$V_{CC} = 1.5\text{ V}$

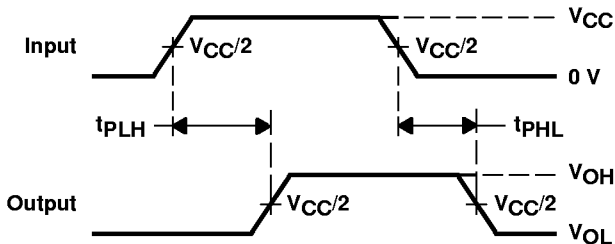


LOAD CIRCUIT

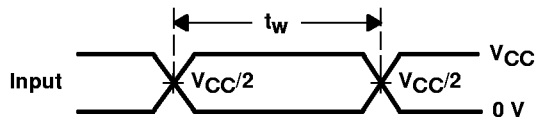
TEST	S1
t_{pd}	Open
t_{pLZ}/t_{pZL}	2 x V_{CC}
t_{PHZ}/t_{PZH}	GND



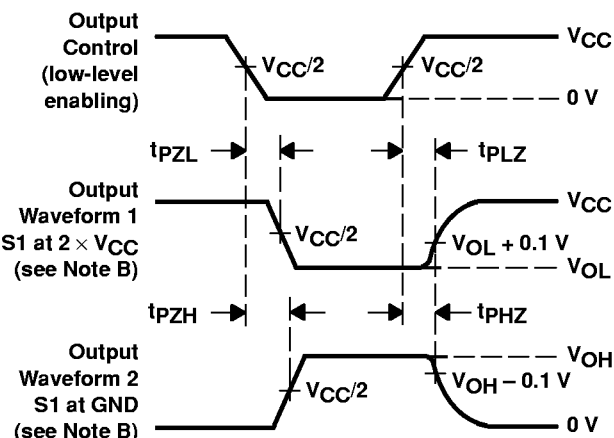
**VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES**



**VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES**



**VOLTAGE WAVEFORMS
PULSE DURATION**



**VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES**

- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r \leq 2\text{ ns}$, $t_f \leq 2\text{ ns}$.
 - D. The outputs are measured one at a time with one transition per measurement.
 - E. t_{pLZ} and t_{pHZ} are the same as t_{dis} .
 - F. t_{pZL} and t_{pZH} are the same as t_{en} .
 - G. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 3. Load Circuit and Voltage Waveforms

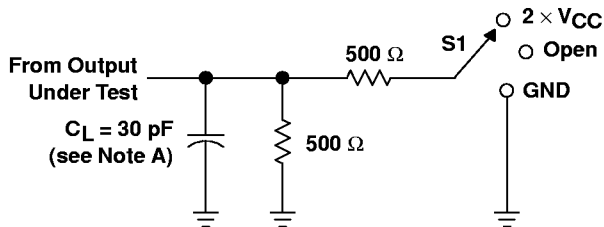
PRODUCT PREVIEW

SN74AVCH16646
16-BIT BUS TRANSCEIVER AND REGISTER
WITH 3-STATE OUTPUTS

SCES182 – DECEMBER 1998

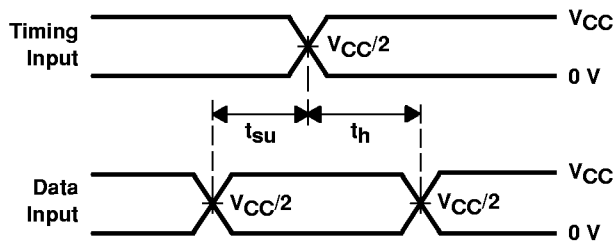
PARAMETER MEASUREMENT INFORMATION

$V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$

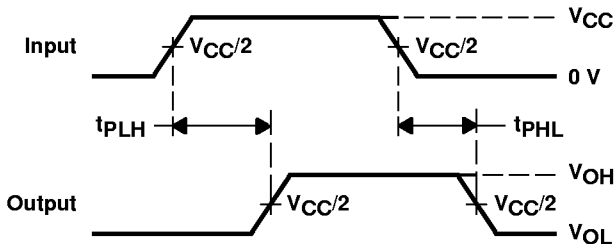


LOAD CIRCUIT

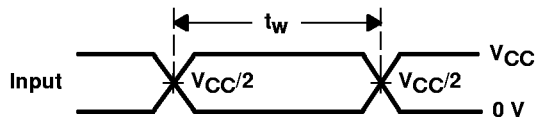
TEST	S1
t_{pd}	Open
t_{pLZ}/t_{pZL}	$2 \times V_{CC}$
t_{PHZ}/t_{PZH}	GND



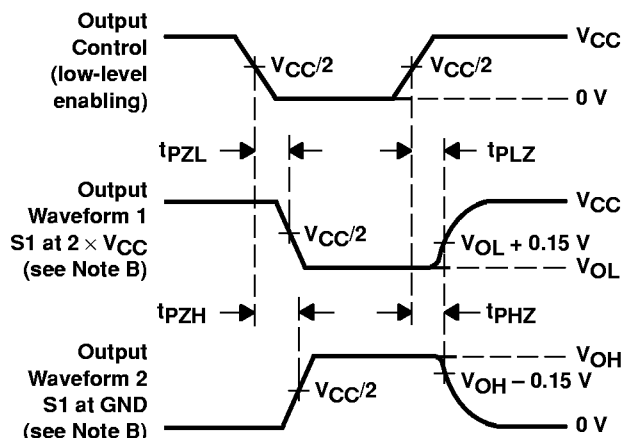
**VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES**



**VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES**



**VOLTAGE WAVEFORMS
PULSE DURATION**



**VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES**

- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r \leq 2\text{ ns}$, $t_f \leq 2\text{ ns}$.
 - D. The outputs are measured one at a time with one transition per measurement.
 - E. t_{pLZ} and t_{pHZ} are the same as t_{dis} .
 - F. t_{pZL} and t_{pZH} are the same as t_{en} .
 - G. t_{PLH} and t_{PHL} are the same as t_{pd} .

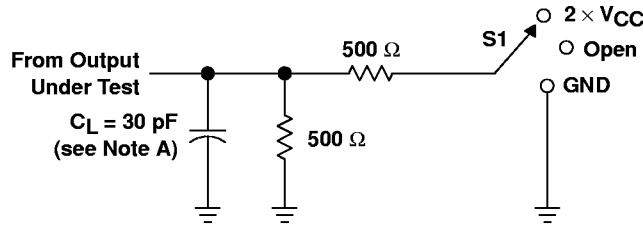
Figure 5. Load Circuit and Voltage Waveforms

PRODUCT PREVIEW



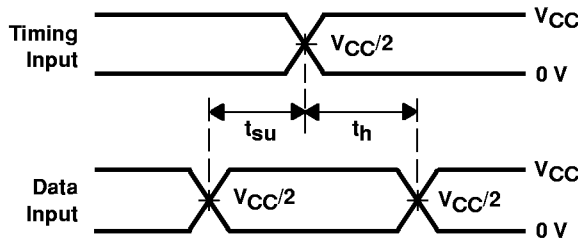
PARAMETER MEASUREMENT INFORMATION

$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$

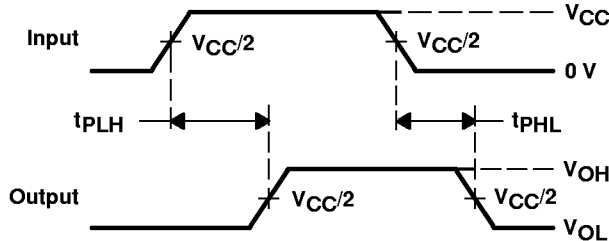


LOAD CIRCUIT

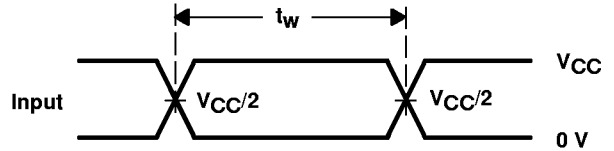
TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	$2 \times V_{CC}$
t_{PHZ}/t_{PZH}	GND



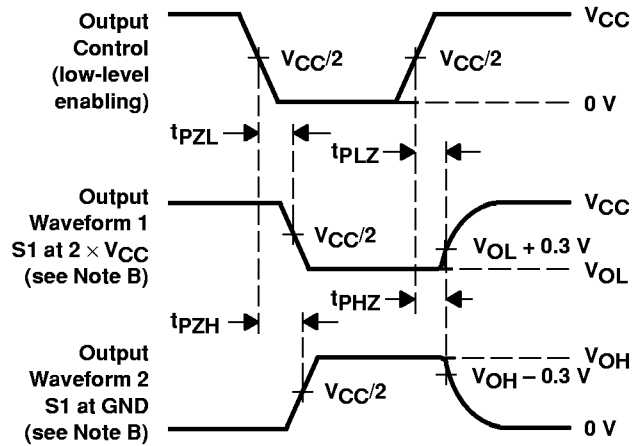
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: PRR $\leq 10\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r \leq 2\text{ ns}$, $t_f \leq 2\text{ ns}$.
 - D. The outputs are measured one at a time with one transition per measurement.
 - E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - F. t_{PZL} and t_{PZH} are the same as t_{en} .
 - G. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 6. Load Circuit and Voltage Waveforms

PRODUCT PREVIEW

IMPORTANT NOTICE

Texas Instruments and its subsidiaries (TI) reserve the right to make changes to their products or to discontinue any product or service without notice, and advise customers to obtain the latest version of relevant information to verify, before placing orders, that information being relied on is current and complete. All products are sold subject to the terms and conditions of sale supplied at the time of order acknowledgement, including those pertaining to warranty, patent infringement, and limitation of liability.

TI warrants performance of its semiconductor products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

CERTAIN APPLICATIONS USING SEMICONDUCTOR PRODUCTS MAY INVOLVE POTENTIAL RISKS OF DEATH, PERSONAL INJURY, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE ("CRITICAL APPLICATIONS"). TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS. INCLUSION OF TI PRODUCTS IN SUCH APPLICATIONS IS UNDERSTOOD TO BE FULLY AT THE CUSTOMER'S RISK.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance or customer product design. TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used. TI's publication of information regarding any third party's products or services does not constitute TI's approval, warranty or endorsement thereof.