



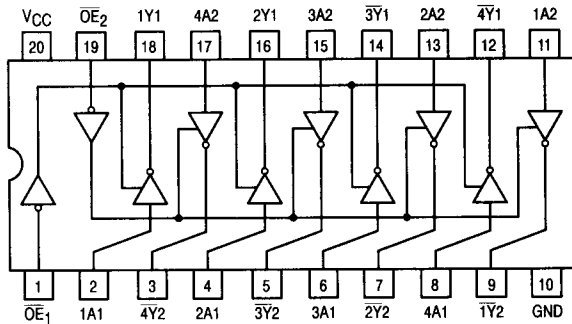
# Octal Buffer With Active Low Enable 3-State Inverted Outputs

ELECTRICALLY TESTED PER:  
MIL-M-38510/33201

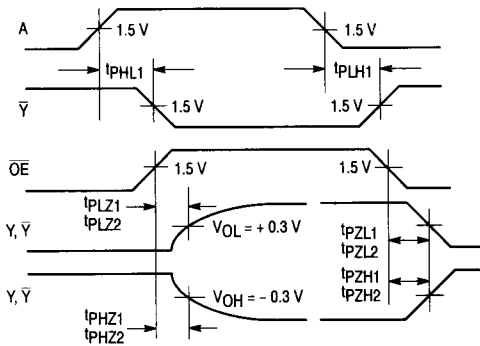
The F240 is an octal buffer and line driver designed to be employed as a memory address driver, clock driver and bus oriented transmitter/receiver which provides improved PC board density.

- 3-State Outputs Drive Bus Lines or Buffer Memory Address Register
- Outputs Sink 64 mA
- 15 mA Source Current
- Input Clamp Diodes Limit High Speed Termination Effects

### LOGIC DIAGRAM



### WAVEFORMS



## Military 54F240



### AVAILABLE AS:

- 1) JAN: JM38510/33201BXA
- 2) SMD: N/A
- 3) 883: 54F240/BXAJC

X = CASE OUTLINE AS FOLLOWS:  
PACKAGE: CERDIP: R  
CERFLAT: S  
LCC: 2

THE LETTER "M" APPEARS  
BEFORE THE / ON LCC.

### PIN ASSIGNMENTS

FUNCT.	DIL 732-03	FLATS 737-02	LCC 756A-02	BURN-IN (COND. A)
OE <sub>1</sub>	1	1	1	VCC
1A1	2	2	2	VCC
4Y <sub>2</sub>	3	3	3	OPEN
2A1	4	4	4	VCC
3Y <sub>2</sub>	5	5	5	OPEN
3A1	6	6	6	VCC
2Y <sub>2</sub>	7	7	7	OPEN
4A1	8	8	8	VCC
1Y <sub>2</sub>	9	9	9	OPEN
GND	10	10	10	GND
1A2	11	11	11	VCC
4Y <sub>1</sub>	12	12	12	OPEN
2A2	13	13	13	VCC
3Y <sub>1</sub>	14	14	14	OPEN
3A2	15	15	15	VCC
2Y <sub>1</sub>	16	16	16	OPEN
4A2	17	17	17	VCC
1Y <sub>1</sub>	18	18	18	OPEN
OE <sub>2</sub>	19	19	19	VCC
VCC	20	20	20	VCC

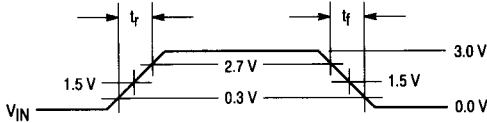
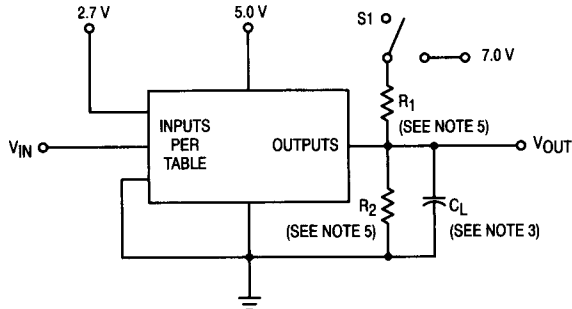
BURN-IN CONDITIONS:  
VCC = 5.0 V MIN/6.0 V MAX

### TRUTH TABLE

Inputs		Output
OE <sub>1</sub> , OE <sub>2</sub>	D	
L	L	H
L	H	L
H	X	Z

H = HIGH Voltage Level      X = Immaterial  
L = LOW Voltage Level      Z = HIGH Impedance

AC TEST CIRCUIT



REFERENCE NOTES ON PAGE 4-105

Test Type	S1
tPLH	open
tPHL	open
tPHZ	open
tPZH	open
tPLZ	closed
tPZL	closed

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Symbol	Parameter	Limits						Unit	Test Condition (Unless Otherwise Specified)
		+ 25°C		+ 125°C		- 55°C			
		Subgroup 1		Subgroup 2		Subgroup 3			
		Min	Max	Min	Max	Min	Max		
VOH	Logical "1" Output Voltage	2.4		2.4		2.4		V	VCC = 4.5 V, IOH = -3.0 mA, VIL = 0.8 V (all inputs).
VOL	Logical "0" Output Voltage		0.55		0.55		0.55	V	VCC = 4.5 V, IOL = 48 mA, VIL = 0.8 V, VIH = 2.0 V.
VIC	Input Clamping Voltage		-1.2					V	VCC = 4.5 V, IIN = -18 mA, other inputs are open.
IiH	Logical "1" Input Current		20		20		20	µA	VCC = 5.5 V, VIH = 2.7 V, other inputs are open.
IiHH	Logical "1" Input Current		100		100		100	µA	VCC = 5.5 V, VIHH = 7.0 V, other inputs are open.
IOD	Diode Current	65		65		65		mA	VCC = 4.5 V, VIN = GND, other input = 5.5 V, VOUT = 2.5 V.
IiL	Logical "0" Input Current	-0.03	-1.0	-0.03	-1.0	-0.03	-1.0	mA	VCC = 5.5 V, VIN = 0.5 V, other inputs are open.
IOS	Output Short Circuit Current	-100	-325	-100	-325	-100	-325	mA	VCC = 5.5 V, VIN = 0 V (all inputs).
IiOZH	Output Off Current High		50		50		50	µA	VCC = 5.5 V, VIN = 2.0 V, other input = 4.5 V, VOUT = 2.4 V.
IiOZL	Output Off Current Low		-50		-50		-50	µA	VCC = 5.5 V, VIN = 2.0 V, other input = 0 V, VOUT = 0.5 V.
IcCH	Power Supply Current		35		35		35	mA	VCC = 5.5 V, VIN = 0 V (all inputs).
IcCL	Power Supply Current		75		75		75	mA	VCC = 5.5 V, VIN = 4.5 V, other input = 0 V.
IcCZ	Power Supply Current Off		75		75		75	mA	VCC = 5.5 V, VIN = 4.5 V, OE2 = 4.5 V, other input is open.
VIH	Logical "1" Input Voltage	2.0		2.0		2.0		V	VCC = 4.5 V.
VIL	Logical "0" Input Voltage		0.8		0.8		0.8	V	VCC = 4.5 V.

## 54F240

Symbol	Parameter	Limits			Unit	Test Condition (Unless Otherwise Specified)
		+ 25°C	+ 125°C	- 55°C		
	Functional Tests	Subgroup 7		Subgroup 8A	Subgroup 8B	per Truth Table with $V_{CC} =$ (See Note 6), $V_{INL} = 0.55 \text{ V}$ , $V_{INH} = 2.4 \text{ V}$ .

Symbol	Parameter	Limits						Unit	Test Condition (Unless Otherwise Specified)
		+ 25°C		+ 125°C		- 55°C			
		Subgroup 9		Subgroup 10		Subgroup 11			
		Min	Max	Min	Max	Min	Max		
t <sub>PHL1</sub>	Propagation Delay /Data-Output Output High-Low	1.0	4.7	1.0	6.0	1.0	6.0	ns	$V_{CC} =$ (See Note 6), $C_L = 50 \text{ pF}$ , $R_1 = R_2 = 500 \Omega$ .
t <sub>PLH1</sub>	Propagation Delay /Data-Output Output Low-High	1.0	7.0	1.0	9.0	1.0	9.0	ns	$V_{CC} =$ (See Note 6), $C_L = 50 \text{ pF}$ , $R_1 = R_2 = 500 \Omega$ .
t <sub>PLZ1</sub>	Propagation Delay /Data-Output Output Low-High	2.0	10	2.0	12.5	2.0	12.5	ns	$V_{CC} =$ (See Note 6), $C_L = 50 \text{ pF}$ , $R_1 = R_2 = 500 \Omega$ .
t <sub>PHZ1</sub>	Propagation Delay /Data-Output Output High-Low	2.0	6.0	2.0	6.5	2.0	6.5	ns	$V_{CC} =$ (See Note 6), $C_L = 50 \text{ pF}$ , $R_1 = R_2 = 500 \Omega$ .
t <sub>PZL1</sub>	Propagation Delay /Data-Output Output Low-High	2.0	9.0	2.0	10.5	2.0	10.5	ns	$V_{CC} =$ (See Note 6), $C_L = 50 \text{ pF}$ , $R_1 = R_2 = 500 \Omega$ .
t <sub>PZH1</sub>	Propagation Delay /Data-Output Output High-Low	2.0	6.0	2.0	6.5	2.0	6.5	ns	$V_{CC} =$ (See Note 6), $C_L = 50 \text{ pF}$ , $R_1 = R_2 = 500 \Omega$ .

**NOTES:**

1. Pulse generator has the following characteristics:  $t_r = t_f \leq 2.5 \text{ ns}$ ,  $\text{PRR} \leq 1.0 \text{ MHz}$  and  $Z_{OUT} = 50 \Omega$ .
2. Terminal conditions (pins not designated may be high  $\geq 2.0 \text{ V}$ , low  $\leq 0.8 \text{ V}$ , or open).
3.  $C_L = 50 \text{ pF} \pm 10\%$  including scope probe, wiring and stray capacitance, without package in test fixture.
4. Voltage measurements are to be made with respect to network ground terminal.
5.  $R_1 = R_2 = 500 \Omega \pm 5.0\%$ .
6. Perform functional tests at  $V_{CC} = 4.5 \text{ V}$  (**repeat at**)  $V_{CC} = 5.0 \text{ V}$ , and  $V_{CC} = 5.5 \text{ V}$  (Motorola imposed).