



3.3V CMOS 16-BIT REGISTERED TRANSCEIVER WITH 3-STATE OUTPUTS, 5 VOLT TOLERANT I/O, BUS-HOLD

IDT74LVCH162543A
ADVANCE
INFORMATION

FEATURES:

- Typical $t_{SK(O)}$ (Output Skew) < 250ps
- ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
- 0.635mm pitch SSOP, 0.50mm pitch TSSOP and 0.40mm pitch TVSOP packages
- Extended commercial range of -40°C to +85°C
- $V_{CC} = 3.3V \pm 0.3V$, Normal Range
- $V_{CC} = 2.7V$ to 3.6V, Extended Range
- CMOS power levels (0.4μW typ. static)
- All inputs, outputs and I/O are 5 Volt tolerant
- Supports hot insertion

Drive Features for LVCH162543A:

- Balanced Output Drivers: ± 12 mA
- Low switching noise

APPLICATIONS:

- 5V and 3.3V mixed voltage systems
- Data communication and telecommunication systems

DESCRIPTION:

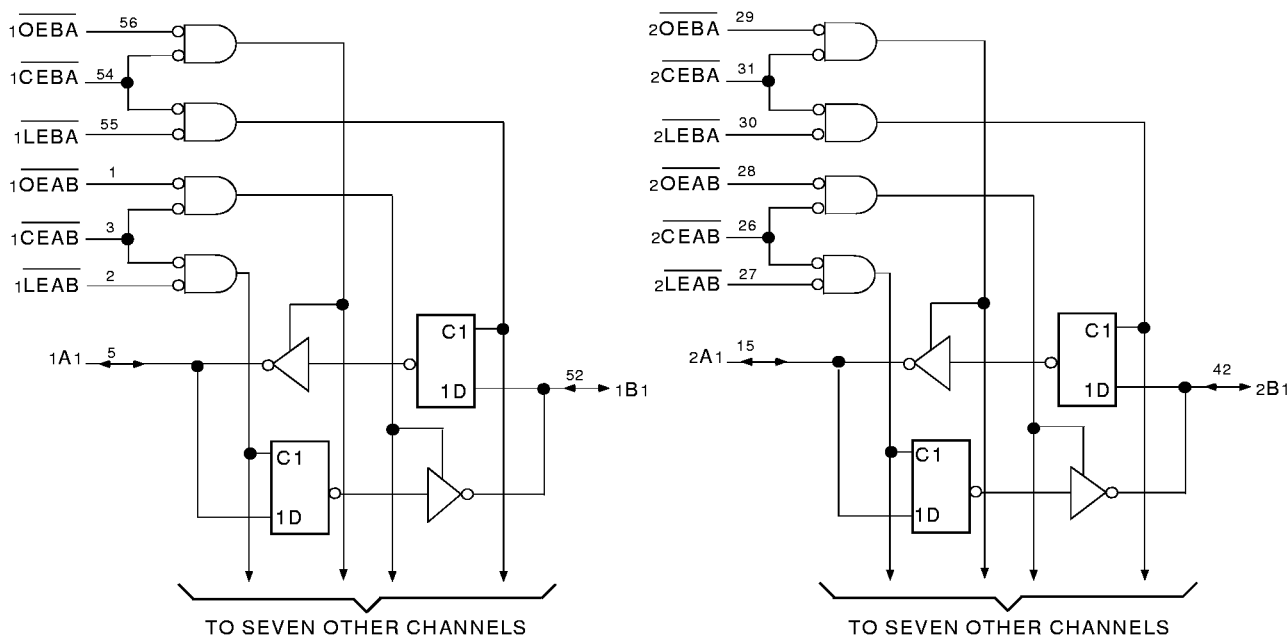
The LVCH162543A 16-bit registered transceiver is built using advanced dual metal CMOS technology. The LVCH162543A device can be used as two independent 8-bit transceivers or one 16-bit transceiver. Separate latch-enable (\overline{LEAB} or \overline{LEBA}) and output-enable (\overline{OEAB} or \overline{OEBA}) inputs are provided for each register to permit independent control in either direction of data flow. The A-to-B enable (\overline{CEAB}) must be low in order to enter data from A or to output data from B. If \overline{CEAB} is low and \overline{LEAB} is low, the A-to-B latches are transparent; a subsequent low-to-high transition of \overline{LEAB} puts the A latches in the storage mode. With \overline{CEAB} and \overline{OEAB} both low, the 3-state B outputs are active and reflect the data present at the output of the A latches. Data flow from B to A is similar, but requires using the \overline{CEBA} , \overline{LEBA} , and \overline{OEBA} inputs. To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current sinking capability of the driver.

The LVCH162543A has series resistors in the device output structure which will significantly reduce line noise when used with light loads. The driver has been designed to drive ± 12 mA at the designated threshold levels.

Inputs can be driven from either 3.3V or 5V devices. This feature allows the use of this device as a translator in a mixed 3.3V/5V supply system.

The LVCH162543A has "bus-hold" which retains the input's last state whenever the input goes to a high impedance. This prevents floating inputs and eliminates the need for pull-up/down resistors.

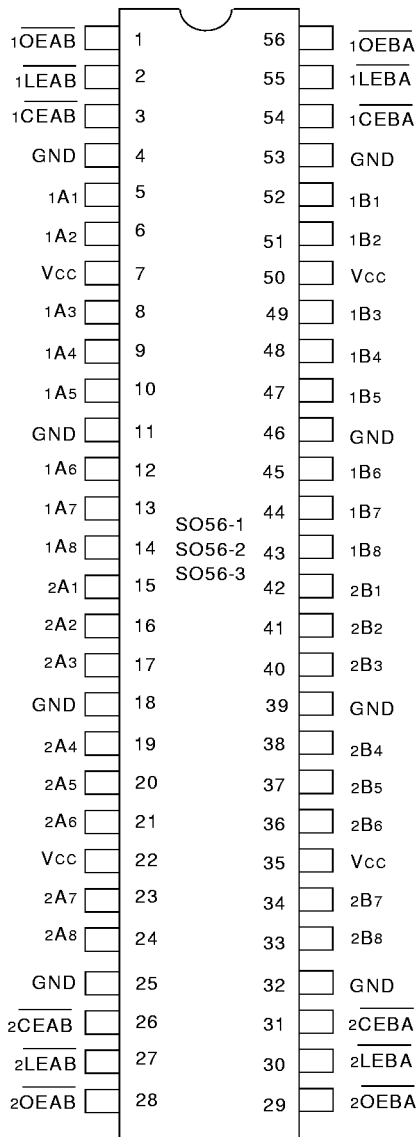
Functional Block Diagram



EXTENDED COMMERCIAL TEMPERATURE RANGE

FEBRUARY 1999

PIN CONFIGURATION



SSOP/ TSSOP/ TVSOP
TOP VIEW

PIN DESCRIPTION

Pin Names	Description
\overline{xOEAB}	A-to-B Output Enable Input (Active LOW)
$\overline{xOEB\overline{A}}$	B-to-A Output Enable Input (Active LOW)
\overline{xCEAB}	A-to-B Enable Input (Active LOW)
$\overline{xCEB\overline{A}}$	B-to-A Enable Input (Active LOW)
\overline{xLEAB}	A-to-B Latch Enable Input (Active LOW)
$\overline{xLEB\overline{A}}$	B-to-A Latch Enable Input (Active LOW)
xAx	A-to-B Data Inputs or B-to-A 3-State Outputs ⁽¹⁾
xBx	B-to-A Data Inputs or A-to-B 3-State Outputs ⁽¹⁾

NOTE:

1. These pins have "Bus-hold". All other pins are standard inputs, outputs, or I/Os.

ABSOLUTE MAXIMUM RATINGS (1)

Symbol	Description	Max.	Unit
$V_{TERM}^{(2)}$	Terminal Voltage with Respect to GND	-0.5 to +6.5	V
$V_{TERM}^{(3)}$	Terminal Voltage with Respect to GND	-0.5 to +6.5	V
TSTG	Storage Temperature	-65 to +150	°C
IOUT	DC Output Current	-50 to +50	mA
I _{IK} I _{OK}	Continuous Clamp Current, $V_I < 0$ or $V_O < 0$	-50	mA
I _{CC} I _{SS}	Continuous Current through each V _{CC} or GND	±100	mA

LVC Link

NOTES:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. V_{CC} terminals.
3. All terminals except V_{CC}.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter ⁽¹⁾	Conditions	Typ.	Max.	Unit
C _{IN}	Input Capacitance	V _{IN} = 0V	4.5	6	pF
C _{OUT}	Output Capacitance	V _{OUT} = 0V	6.5	8	pF
C _{I/O}	I/O Port Capacitance	V _{IN} = 0V	6.5	8	pF

LVC Link

NOTE:

1. As applicable to the device type.

FUNCTION TABLE (each 8-bit section) (1, 2)

Inputs				Output
\overline{xCEAB}	\overline{xLEAB}	\overline{xOEAB}	xAx	xBx
H	X	X	X	Z
X	X	H	X	Z
L	H	L	X	B ₀ ⁽³⁾
L	L	L	L	L
L	L	L	H	H

NOTES:

1. H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
Z = High-Impedance
2. A-to-B data flow is shown; B-to-A flow control is the same except using \overline{CEBA} , \overline{LEBA} , and \overline{OEBA} .
3. Before \overline{LEAB} LOW-to-HIGH Transition

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Operating Condition: $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$

Symbol	Parameter	Test Conditions		Min.	Typ. ⁽¹⁾	Max.	Unit
V _{IH}	Input HIGH Voltage Level	V _{CC} = 2.3V to 2.7V		1.7	—	—	V
		V _{CC} = 2.7V to 3.6V		2	—	—	
V _{IL}	Input LOW Voltage Level	V _{CC} = 2.3V to 2.7V		—	—	0.7	V
		V _{CC} = 2.7V to 3.6V		—	—	0.8	
I _{IH} I _{IL}	Input Leakage Current	V _{CC} = 3.6V	V _I = 0 to 5.5V	—	—	±5	μA
I _{OZH} I _{OZL}	High Impedance Output Current (3-State Output pins)	V _{CC} = 3.6V	V _O = 0 to 5.5V	—	—	±10	μA
I _{OFF}	Input/Output Power Off Leakage	V _{CC} = 0V, V _{IN} or V _O ≤ 5.5V		—	—	±50	μA
V _{IK}	Clamp Diode Voltage	V _{CC} = 2.3V, I _{IN} = -18mA		—	-0.7	-1.2	V
V _H	Input Hysteresis	V _{CC} = 3.3V		—	100	—	mV
I _{CCL} I _{CCH} I _{CCZ}	Quiescent Power Supply Current	V _{CC} = 3.6V	V _{IN} = GND or V _{CC}	—	—	10	μA
			3.6 ≤ V _{IN} ≤ 5.5V ⁽²⁾	—	—	10	
ΔI _{CC}	Quiescent Power Supply Current Variation	One input at V _{CC} - 0.6V other inputs at V _{CC} or GND		—	—	500	μA

LVC Link

NOTES:

- Typical values are at V_{CC} = 3.3V, +25°C ambient.
- This applies in the disabled state only.

BUS-HOLD CHARACTERISTICS

Symbol	Parameter ⁽¹⁾	Test Conditions		Min.	Typ. ⁽²⁾	Max.	Unit
I _{BHH} I _{BHL}	Bus-Hold Input Sustain Current	V _{CC} = 3.0V	V _I = 2.0V	-75	—	—	μA
			V _I = 0.8V	75	—	—	
I _{BHH} I _{BHL}	Bus-Hold Input Sustain Current	V _{CC} = 2.3V	V _I = 1.7V	—	—	—	μA
			V _I = 0.7V	—	—	—	
I _{BHHO} I _{BHLO}	Bus-Hold Input Overdrive Current	V _{CC} = 3.6V	V _I = 0 to 3.6V	—	—	±500	μA

LVC Link

NOTES:

- Pins with Bus-hold are identified in the pin description.
- Typical values are at V_{CC} = 3.3V, +25°C ambient.

OUTPUT DRIVE CHARACTERISTICS

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Max.	Unit
V _{OH}	Output HIGH Voltage	V _{CC} = 2.3V to 3.6V	I _{OH} = -0.1mA	V _{CC} - 0.2	—	V
		V _{CC} = 2.3V	I _{OH} = -4mA	1.9	—	
			I _{OH} = -6mA	1.7	—	
		V _{CC} = 2.7V	I _{OH} = -4mA	2.2	—	
			I _{OH} = -8mA	2	—	
		V _{CC} = 3.0V	I _{OH} = -6mA	2.4	—	
I _{OH} = -12mA	2		—			
V _{OL}	Output LOW Voltage	V _{CC} = 2.3V to 3.6V	I _{OL} = 0.1mA	—	0.2	V
		V _{CC} = 2.3V	I _{OL} = 4mA	—	0.4	
			I _{OL} = 6mA	—	0.55	
		V _{CC} = 2.7V	I _{OL} = 4mA	—	0.4	
			I _{OL} = 8mA	—	0.6	
		V _{CC} = 3.0V	I _{OL} = 6mA	—	0.55	
I _{OL} = 12mA	—		0.8			

LVC Link

NOTE:

- V_{IH} and V_{IL} must be within the min. or max. range shown in the DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE table for the appropriate V_{CC} range. T_A = -40°C to +85°C.

OPERATING CHARACTERISTICS, V_{CC} = 3.3V ± 0.3V, T_A = 25°C

Symbol	Parameter	Test Conditions	Typical	Unit
CPD	Power Dissipation Capacitance per transceiver Outputs enabled	C _L = 0pF, f = 10Mhz		pF
CPD	Power Dissipation Capacitance per transceiver Outputs disabled			pF

SWITCHING CHARACTERISTICS (1)

Symbol	Parameter	V _{CC} = 2.7V		V _{CC} = 3.3V±0.3V		Unit
		Min.	Max.	Min.	Max.	
t _{PLH} t _{PHL}	Propagation Delay x _A to x _B or x _B to x _A	1.5	7	1.5	6	ns
t _{PLH} t _{PHL}	Propagation Delay x _{LEB} to x _A , x _{LEA} to x _B	1.5	8	1.5	7	ns
t _{PZH} t _{PZL}	Output Enable Time x _{CEB} or x _{CEA} to x _A or x _B	1.5	9	1.5	8	ns
t _{PZH} t _{PZL}	Output Enable Time x _{OEB} or x _{OEA} to x _A or x _B	1.5	9	1.5	8	ns
t _{PHZ} t _{PLZ}	Output Disable Time x _{CEB} or x _{CEA} to x _A or x _B	1.5	7.5	1.5	6.5	ns
t _{PHZ} t _{PLZ}	Output Disable Time x _{OEB} or x _{OEA} to x _A or x _B	1.5	7.5	1.5	6.5	ns
t _{SU}	Set-up Time HIGH or LOW x _A or x _B to x _{LEA} or x _{LEB} , x _{CEA} ↓ or x _{CEB} ↓	2	—	2	—	ns
t _H	Hold Time HIGH or LOW x _A or x _B to x _{LEA} or x _{LEB} , x _{CEA} ↓ or x _{CEB} ↓	2	—	2	—	ns
t _W	Pulse Duration x _{LEA} or x _{LEB} , x _{CEA} or x _{CEB} LOW	5	—	5	—	ns
t _{sk(o)}	Output Skew ⁽²⁾	—	—	—	500	ps

NOTES:

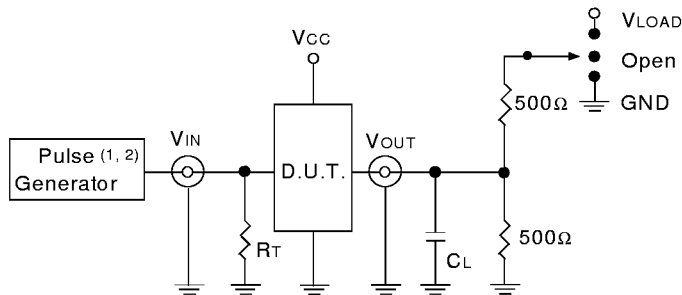
1. See test circuits and waveforms. T_A = -40°C to +85°C.
2. Skew between any two outputs of the same package and switching in the same direction.

TEST CIRCUITS AND WAVEFORMS

TEST CONDITIONS

Symbol	Vcc(1)= 3.3V ±0.3V	Vcc(1)= 2.7V	Vcc(2)= 2.5V ±0.2V	Unit
V _{LOAD}	6	6	2 x V _{cc}	V
V _{IH}	2.7	2.7	V _{cc}	V
V _T	1.5	1.5	V _{cc} / 2	V
V _{LZ}	300	300	150	mV
V _{HZ}	300	300	150	mV
C _L	50	50	30	pF

TEST CIRCUITS FOR ALL OUTPUTS



DEFINITIONS:

CL = Load capacitance: includes jig and probe capacitance.
 RT = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

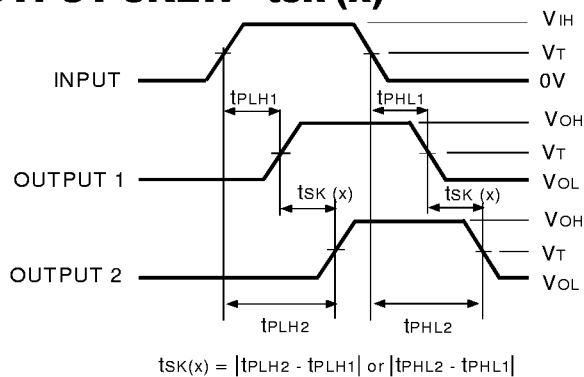
NOTE:

1. Pulse Generator for All Pulses: Rate ≤ 10MHz; t_F ≤ 2.5ns; t_R ≤ 2.5ns.
2. Pulse Generator for All Pulses: Rate ≤ 10MHz; t_F ≤ 2ns; t_R ≤ 2ns.

SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	V _{LOAD}
Disable High Enable High	GND
All Other tests	Open

OUTPUT SKEW - t_{SK}(x)

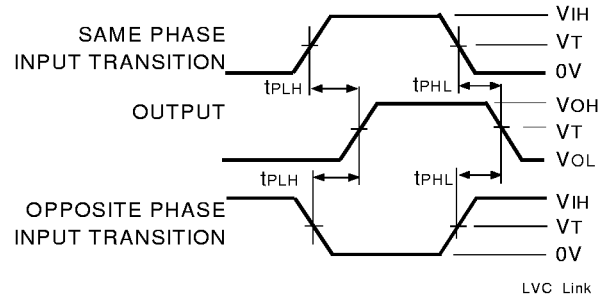


$$t_{SK}(x) = |t_{PLH2} - t_{PLH1}| \text{ or } |t_{PHL2} - t_{PHL1}|$$

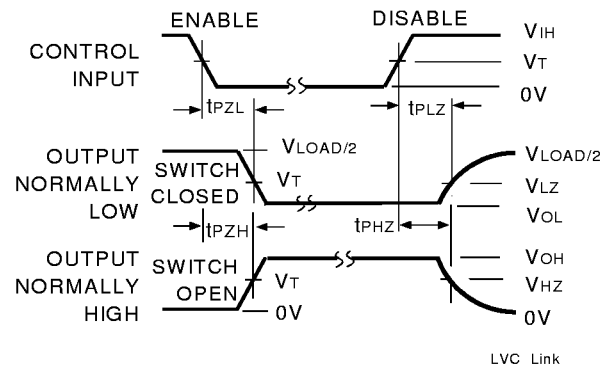
NOTES:

1. For t_{SK}(o) OUTPUT1 and OUTPUT2 are any two outputs.
2. For t_{SK}(b) OUTPUT1 and OUTPUT2 are in the same bank.

PROPAGATION DELAY



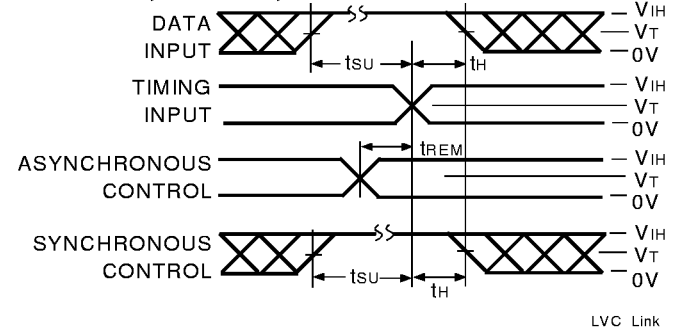
ENABLE AND DISABLE TIMES



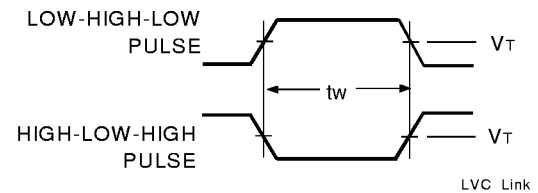
NOTE:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.

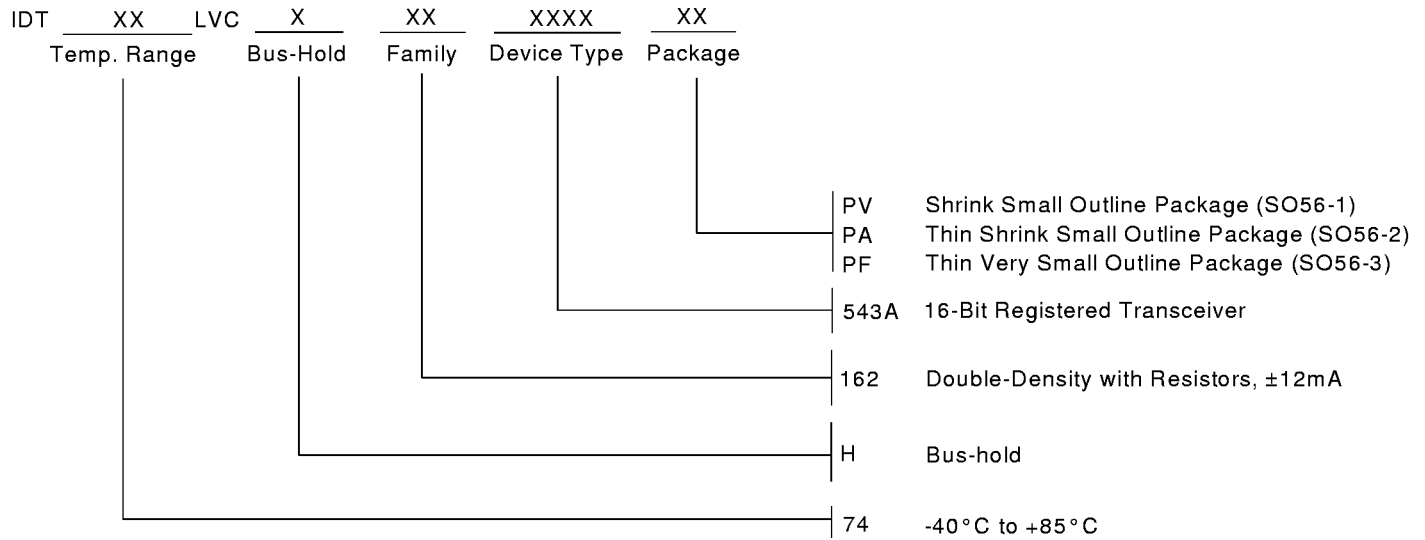
SET-UP, HOLD, AND RELEASE TIMES



PULSE WIDTH



ORDERING INFORMATION



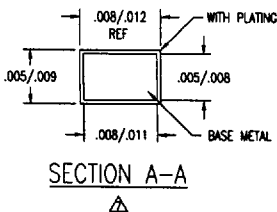
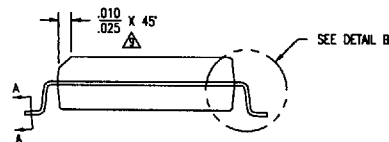
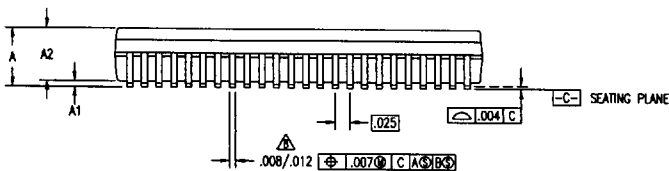
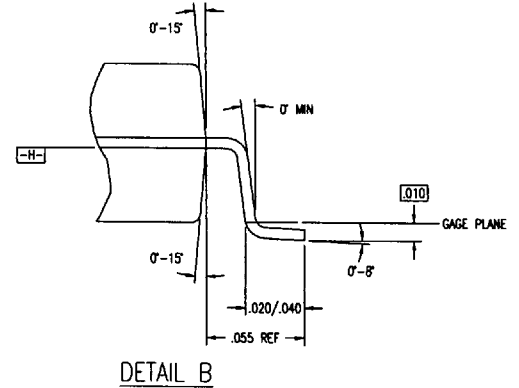
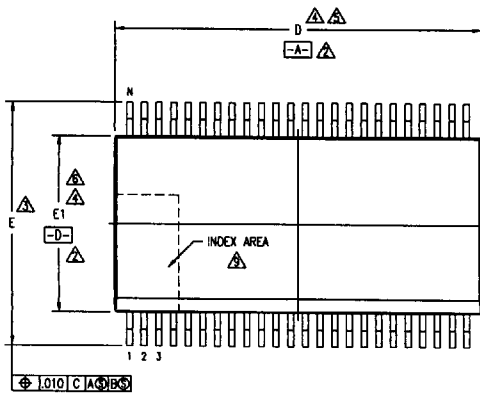
CORPORATE HEADQUARTERS
 2975 Stender Way
 Santa Clara, CA 95054

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PACKAGE DIAGRAM OUTLINES
SSOP

REVISIONS				
DCN	REV	DESCRIPTION	DATE	APPROVED
17893	00	INITIAL RELEASE	07/15/90	A. FUNCELL
22377	01	REMOVE CHAMFER FROM PACKAGE	04/15/92	T. WJ
27492	02	REDRAW TO JEDEC FORMAT	02/01/95	



TOLERANCES UNLESS SPECIFIED		Integrated Device Technology, Inc. 2975 Slender Way, Santa Clara, CA 95054 PHONE: (408) 727-8118 FAX: (408) 462-8874 TWC: 910-338-2070	
DECIMAL	ANGULAR	APPROVALS DATE TITLE PV PACKAGE OUTLINE .300" BODY WIDTH SSOP .025" PITCH	
DRWN	CHKD	SIZE C DRAWING No. PSC-4029	REV 02
CHECKED		DO NOT SCALE DRAWING	

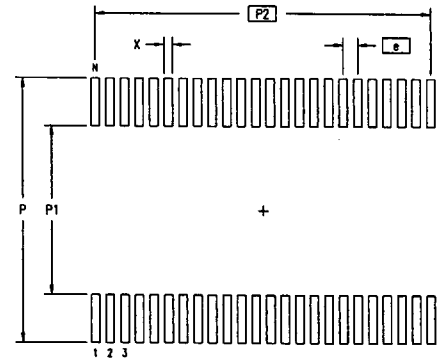
PACKAGE DIAGRAM OUTLINES

SSOP (Continued)

REVISIONS				
DCN	REV	DESCRIPTION	DATE	APPROVED
17893	00	INITIAL RELEASE	07/15/90	A. FUNCELL
22377	01	REMOVE CHAMFER FROM PACKAGE	04/15/92	T. WU
27492	02	REDRAW TO JEDEC FORMAT	02/01/95	

SYMBOL	DWG # S048-1				DWG # S056-1			
	JEDEC VARIATION			NOTE	JEDEC VARIATION			NOTE
	AA				AB			
	MIN	NOM	MAX		MIN	NOM	MAX	
A	.095	.102	.110		.095	.102	.110	
A1	.008	.012	.016		.008	.012	.016	
A2	.088	.090	.092		.088	.090	.092	
D	.620	.625	.630	4,5	.720	.725	.730	4,5
E	.395	.405	.420	3	.395	.405	.420	3
E1	.291	.295	.299	4,6	.291	.295	.299	4,6
N	48				56			

LAND PATTERN DIMENSIONS



	MIN	MAX	MIN	MAX
P	.450	.458	.450	.458
P1	.282	.290	.282	.290
P2	.575 BSC		.675 BSC	
X	.010	.018	.010	.018
e	.025 BSC		.025 BSC	
N	48		56	

NOTES:

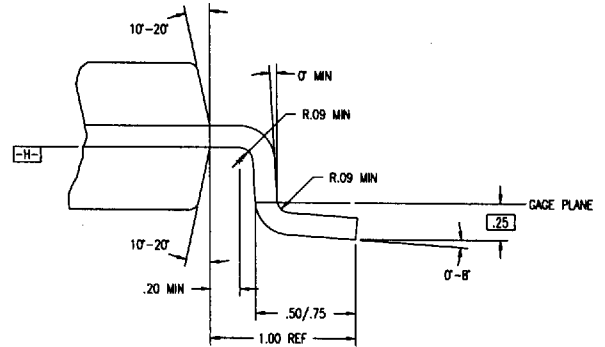
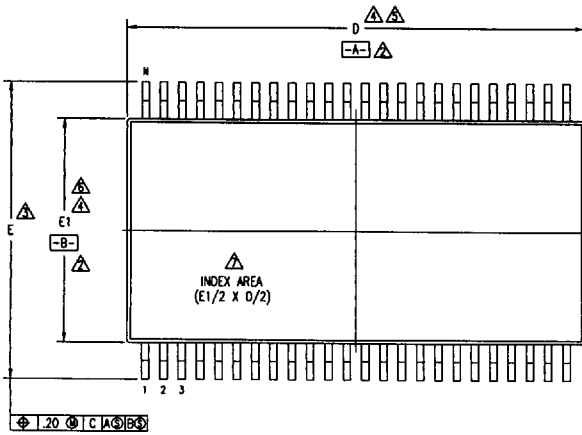
- ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5M-1982
- DATUMS **-A-** AND **-B-** TO BE DETERMINED AT DATUM PLANE **-H-**
- DIMENSION E TO BE DETERMINED AT SEATING PLANE **-C-**
- DIMENSIONS D AND E1 ARE TO BE DETERMINED AT DATUM PLANE **-H-**
- DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED .006 PER SIDE
- DIMENSION E1 DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS. INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED .015 PER SIDE
- THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN .005 AND .010 FROM LEAD TIP
- LEAD WIDTH DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION IS .004 IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT
- THE CHAMFER ON THE PACKAGE BODY IS OPTIONAL. IF IT IS NOT PRESENT, A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE ZONE INDICATED
- ALL DIMENSIONS ARE IN INCHES
- THIS OUTLINE CONFORMS TO JEDEC PUBLICATION 95 REGISTRATION MO-118, VARIATION AA & AB

TOLERANCES UNLESS SPECIFIED		Integrated Device Technology, Inc. 2975 Stoner Way, Santa Clara, CA 95054 PHONE: (408) 727-8116 FAX: (408) 482-8874 TWC: 810-338-2070	
DECIMAL	ANGULAR		
X.XX	±		
X.XXX			
X.XXX			
APPROVALS	DATE	TITLE	
DRAWN <i>Ad</i>	08/15/90	PV PACKAGE OUTLINE .300" BODY WIDTH SSOP .025" PITCH	
CHECKED		SIZE	REV
		C	02
		DRAWING No.	
		PSC-4029	
DO NOT SCALE DRAWING			

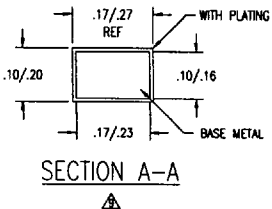
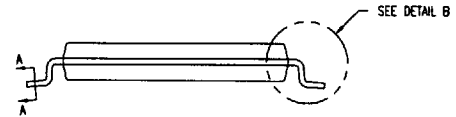
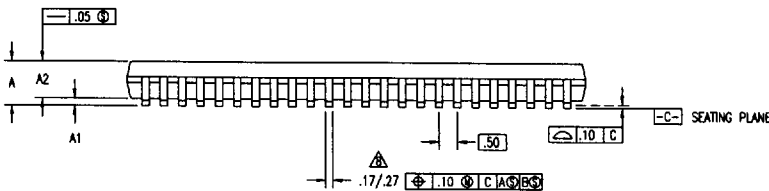
PACKAGE DIAGRAM OUTLINES

TSSOP

REVISIONS				
DCN	REV	DESCRIPTION	DATE	APPROVED
23757	00	INITIAL RELEASE	02/15/93	T. VJ
26315	01	CHANGE DIMS A1 & A2	05/18/94	DG
26490	02	CHANGE DIM A1	07/21/94	T. VJ
27494	03	REDRAW TO JEDEC FORMAT	03/06/95	



DETAIL B



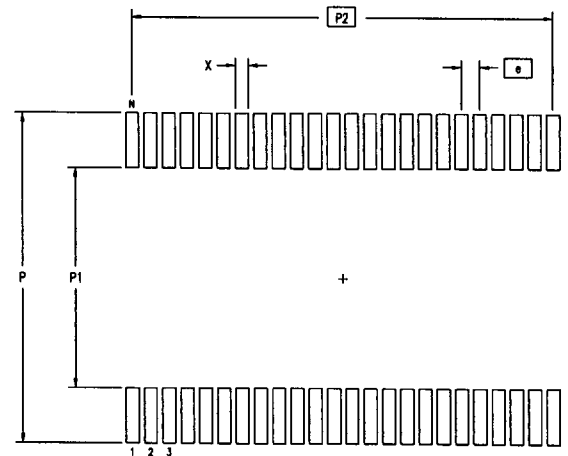
TOLERANCES UNLESS SPECIFIED		Integrated Device Technology, Inc. 2975 Slender Way, Santa Clara, CA 95054 PHONE: (408) 727-8118 FAX: (408) 492-8674 TWC: 910-338-2070
DECIMAL	ANGULAR	
XXX.X	±	
APPROVALS		TITLE PA PACKAGE OUTLINE 6.10 mm BODY WIDTH TSSOP .50 mm PITCH
DRAWN	DATE	
CHECKED		SIZE C DRAWING No. PSC-4039 REV 03 DO NOT SCALE DRAWING

PACKAGE DIAGRAM OUTLINES
TSSOP (Continued)

REVISIONS				
DCN	REV	DESCRIPTION	DATE	APPROVED
23757	00	INITIAL RELEASE	02/15/93	T. WU
26315	01	CHANGE DIMS A1 & A2	05/18/94	DG
26490	02	CHANGE DIM A1	07/21/94	T. WU
27494	03	REDRAW TO JEDEC FORMAT	03/08/95	

SYMBOL	DWG # S048-2			NOTE	DWG # S056-2			NOTE
	JEDEC VARIATION				JEDEC VARIATION			
	ED	EE			ED	EE		
MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX
A	-	-	1.10		-	-	1.10	
A1	.05	-	.15		.05	-	.15	
A2	.85	1.00	1.05		.85	1.00	1.05	
D	12.40	12.50	12.60	4,5	13.90	14.00	14.10	4,5
E	7.95	8.10	8.25	3	7.95	8.10	8.25	3
E1	6.00	6.10	6.20	4,6	6.00	6.10	6.20	4,6
N	48				56			

LAND PATTERN DIMENSIONS



	MIN	MAX	MIN	MAX
P	8.90	9.10	8.90	9.10
P1	5.90	6.10	5.90	6.10
P2	11.50	BSC	13.50	BSC
X	.30	.40	.30	.40
e	.50	BSC	.50	BSC
N	48		56	

NOTES:

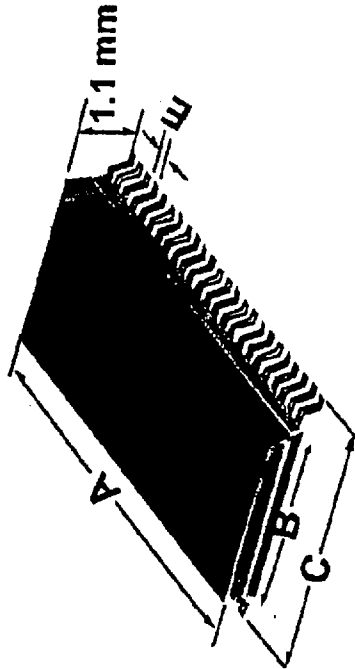
- 1 ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5M-1982
- △ DATUMS \square -A- AND \square -B- TO BE DETERMINED AT DATUM PLANE \square -H-
- △ DIMENSION E TO BE DETERMINED AT SEATING PLANE \square -C-
- △ DIMENSIONS D AND E1 ARE TO BE DETERMINED AT DATUM PLANE \square -H-
- △ DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED .15 mm PER SIDE
- △ DIMENSION E1 DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS. INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED .25 mm PER SIDE
- △ DETAIL OF PIN 1 IDENTIFIER IS OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED
- △ LEAD WIDTH DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION IS .08 mm IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT
- △ THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN .10 AND .25 mm FROM THE LEAD TIP
- 10 ALL DIMENSIONS ARE IN MILLIMETERS
- 11 THIS OUTLINE CONFORMS TO JEDEC PUBLICATION 95 REGISTRATION MQ-153, VARIATION ED & EE

TOLERANCES UNLESS SPECIFIED		Integrated Device Technology, Inc.	
DECIMAL	ANGULAR	2975 Slender Way, Santa Clara, CA 95054	
±	±	PHONE: (408) 727-8118	
HOLE & POSITION		FAX: (408) 482-8874 TWC: 910-338-2070	
APPROVALS	DATE	TITLE PA PACKAGE OUTLINE	
DRAWN	01/19/93	6.10 mm BODY WIDTH TSSOP	
CHECKED		.50 mm PITCH	
SIZE	DRAWING No.	REV	
C	PSC-4039	03	
DO NOT SCALE DRAWING			



TVSOP

The Most Compact Double Density Package

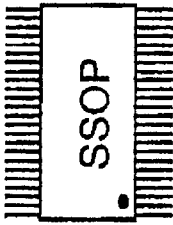


TVSOP Package	Typical Dimensions (in mm)				Area (mm ²)
	A	B	C	E	
48 Pin	9.80	4.40	6.40	0.40	63.00
56 Pin	11.30	4.40	6.40	0.40	72.30
80 Pin	17.00	6.10	8.10	0.40	137.80
100 Pin	20.80	6.10	8.10	0.40	168.50



Double Density Packaging

48-Pin



16.0 x 10.3 x 2.6 mm
pin pitch = 0.635 mm
Area = 164.8 mm²

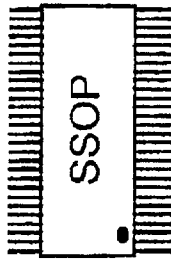


12.5 x 8.1 x 1.1 mm
pin-pitch = 0.5 mm
Area = 101.3 mm²



9.8 x 6.4 x 1.1 mm
pin-pitch = 0.4 mm
Area = 62.7 mm²

56-Pin



18.4 x 10.3 x 2.6 mm
pin-pitch = 0.635 mm
Area = 189.5 mm²



14.0 x 8.1 x 1.1 mm
pin-pitch = 0.5 mm
Area = 113.4 mm²



11.3 x 6.4 x 1.1 mm
pin-pitch = 0.4 mm
Area = 72.3 mm²

TVSOP	Area (mm ²)	%Smaller Than SSOP	%Smaller Than TSSOP
48 pin	63.00	61.9	38.0
56 pin	72.30	62.2	36.0