MOTOROLA

MC74AC175
MC74ACT175

Product Preview

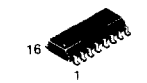
Quad D Flip-Flop

QUAD D FLIP-FLOP

The MC74AC175/74ACT175 is a high-speed quad D flip-flop. The device is useful for general flip-flop requirements where clock and clear inputs are common. The information on the D inputs is stored during the LOW-to-HIGH clock transition. Both true and complemented outputs of each flip-flop are provided. A Master Reset input resets all flip-flops, independent of the Clock or D inputs, when LOW.

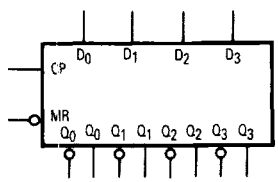
- Edge-Triggered D-Type Inputs
- Buffered Positive Edge-Triggered Clock
- Asynchronous Common Reset
- True and Complement Output
- Outputs Source/Sink 24 mA
- 'ACT175 Has TTL Compatible Inputs

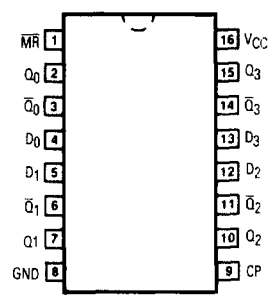
N SUFFIX
CASE 648-08
PLASTIC



D SUFFIX
CASE 751B-03
PLASTIC

LOGIC SYMBOL





PIN NAMES

D_0–D_3	Data Inputs
CP	Clock Pulse Input
$\overline{MR}$	Master Reset Input
Q_0–Q_3	True Outputs
$\overline{Q}_0$–$\overline{Q}_3$	Complement Outputs

TRUTH TABLE

Inputs	Outputs	
@ t_n, $\overline{MR}$ = H	@ t_{n+1}	
D_n	Q_n	$\overline{Q}_n$
L	L	H
H	H	L

H = HIGH Voltage Level
L = LOW Voltage Level
t_n = Bit Time before Clock Pulse
t_{n+1} = Bit Time after Clock Pulse

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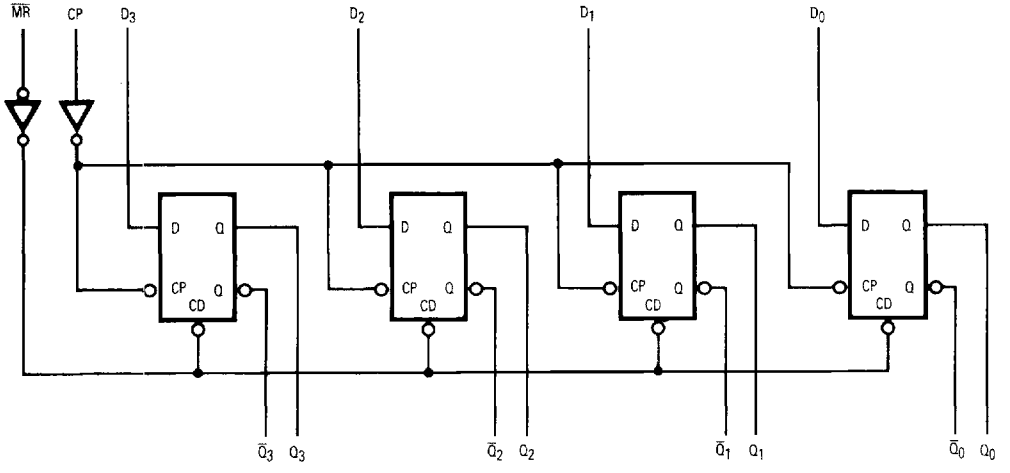
This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

FUNCTIONAL DESCRIPTION

The MC74AC175/74ACT175 consists of four edge-triggered D flip-flops with individual D inputs and Q and $\overline{Q}$ outputs. The Clock and Master Reset are common. The four flip-flops will store the state of their individual D inputs on the LOW-to-HIGH clock (CP) transition, causing individual Q and $\overline{Q}$ outputs to follow. A LOW input on the Master Reset ($\overline{MR}$) will force all Q outputs LOW and $\overline{Q}$ outputs HIGH independent of Clock or Data inputs. The MC74AC175/74ACT175 is useful for general logic applications where a common Master Reset and Clock are acceptable.

LOGIC DIAGRAM



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

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DC CHARACTERISTICS (unless otherwise specified)

Symbol	Parameter	Value	Units	Test Conditions
I_{CC}	Maximum Quiescent Supply Current	80	μA	$V_{IN} = V_{CC}$ or Ground, $V_{CC} = 5.5$ V, $T_A =$ Worst Case
I_{CC}	Maximum Quiescent Supply Current	8.0	μA	$V_{IN} = V_{CC}$ or Ground, $V_{CC} = 5.5$ V, $T_A = 25°C$
I_{CCT}	Maximum Additional I_{CC}/Input ('ACT175)	1.5	mA	$V_{IN} = V_{CC} - 2.1$ V $V_{CC} = 5.5$ V, $T_A =$ Worst Case

AC CHARACTERISTICS (For Figures and Waveforms — See Section 3)

Symbol	Parameter	V_{CC}* (V)	74AC $T_A = +25°C$ $C_L = 50$ pF			74AC $T_A = -40°C$ to $+85°C$ $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max		
f_{max}	Maximum Clock Frequency	3.3 5.0		118 160				MHz	3-3
t_{PLH}	Propagation Delay CP to Q_n or $\overline{Q}_n$	3.3 5.0		9.5 7.0				ns	3-6
t_{PHL}	Propagation Delay CP to Q_n or $\overline{Q}_n$	3.3 5.0		8.5 6.0				ns	3-6
t_{PHL}	Propagation Delay $\overline{MR}$ to Q_n	3.3 5.0		7.5 5.5				ns	3-6
t_{PLH}	Propagation Delay $\overline{MR}$ to $\overline{Q}_n$	3.3 5.0		8.5 6.0				ns	3-6

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

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AC OPERATING REQUIREMENTS

Symbol	Parameter	V_{CC}* (V)	74AC T_A = +25°C, C_L = 50 pF		74AC T_A = −40°C to +85°C, C_L = 50 pF	Units	Fig. No.
			Typ	Guaranteed Minimum			
t_s	Setup Time, HIGH or LOW D_n to CP	3.3 5.0	4.5 3.0			ns	3-9
t_h	Hold Time, HIGH or LOW D_n to CP	3.3 5.0	0 0			ns	3-9
t_w	CP Pulse Width HIGH or LOW	3.3 5.0	5.5 4.0			ns	3-6
t_w	$\overline{MR}$ Pulse Width, LOW	3.3 5.0	5.5 4.0			ns	3-6
t_{rec}	Recovery Time $\overline{MR}$ to CP	3.3 5.0	0 0			ns	3-9

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

AC CHARACTERISTICS (For Figures and Waveforms — See Section 3)

Symbol	Parameter	V_{CC}* (V)	74ACT T_A = +25°C, C_L = 50 pF			74ACT T_A = −40°C to +85°C, C_L = 50 pF		Units	Fig. No.
			Min	Typ	Max	Min	Max		
f_{max}	Maximum Clock Frequency	5.0	175	160		145		MHz	3-3
t_{PLH}	Propagation Delay CP to Q_n or $\overline{Q}_n$	5.0	1.0	6.0	10	1.0	11	ns	3-6
t_{PHL}	Propagation Delay CP to Q_n or $\overline{Q}_n$	5.0	1.0	7.0	11	1.0	12	ns	3-6
t_{PLH}	Propagation Delay $\overline{MR}$ to Q_n	5.0	1.0	6.0	9.5	1.0	10.5	ns	3-6
t_{PHL}	Propagation Delay $\overline{MR}$ to Q_n	5.0	1.0	5.5	9.5	1.0	10.5	ns	3-6

*Voltage Range 5.0 is 5.0 V ± 0.5 V

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AC OPERATING REQUIREMENTS

Symbol	Parameter	V_{CC}* (V)	74ACT T_A = +25°C, C_L = 50 pF		74ACT T_A = −40°C to +85°C, C_L = 50 pF	Units	Fig. No.
			Typ	Guaranteed Minimum			
t_s (H) t_s (L)	Setup Time D_n to CP	5.0	3.0 3.0	2.0 2.5	2.0 2.5	ns	3-9
t_h	Hold Time, HIGH or LOW D_n to CP	5.0	0	1.0	1.0	ns	3-9
t_w	CP Pulse Width HIGH or LOW	5.0	4.0	3.0	3.5	ns	3-6
t_w	$\overline{MR}$ Pulse Width, LOW	5.0	4.0	3.5	4.0	ns	3-6
t_{rec}	Recovery Time $\overline{MR}$ to CP	5.0	0	0	0	ns	3-9

*Voltage Range 5.0 is 5.0 V ± 0.5 V

CAPACITANCE

Symbol	Parameter	Value Typ	Units	Test Conditions
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = 5.0 V
C_{PD}	Power Dissipation Capacitance	45	pF	V_{CC} = 5.0 V