Texas Instruments

TPS92314 TPS92314A

Off-Line Primary Side Sensing Controller with PFC

General Description

The TPS92314/14A is an off-line controller specifically designed to drive high power LEDs for lighting applications. Features include adaptive constant on-time control and quasi-resonant switching. Resonant switching allows for a reduced EMI signature and increased system efficiency. Thus, the device introduces a low external parts count and high level of integration. The control algorithm of TPS92314/14A adjusts the on time with reference to the primary side inductor peak current and secondary side inductor discharge time dynamically, the response time of which is set by an external capacitor.

The over current protection is implemented by a cycle by cycle current limit of the primary inductor current. TPS92314A has a higher OCP threshold which is more suitable for universal line application and TPS92314 can optimize the system cost. Other supervisory features of the TPS92314/14A include VCC over voltage protection and under-voltage lockout, output LEDs over-voltage protection and controller thermal shutdown. The TPS92314/14A is available in 8 pin SOIC package.

Features

- Regulates LED current without secondary side sensing
- Adaptive ON-time control with inherent PFC
- Critical-Conduction-Mode (CRM) with Zero-Current Detection (ZCD) for valley switching
- Programmable switch turn ON delay
- Programmable Constant ON-Time (COT)
- Over Current Limit Options:
  TPS92314: 1.15V
  TPS92314A: 2.0V
- Advanced Over Current and Over Voltage Protection
- Internal Over-temperature Protection
- 8-Pin SOIC Package

Applications

- Residential LED Lamps: A19 (E26/27, E14), PAR30/38, GU10
- Solid State Lighting

Typical Application

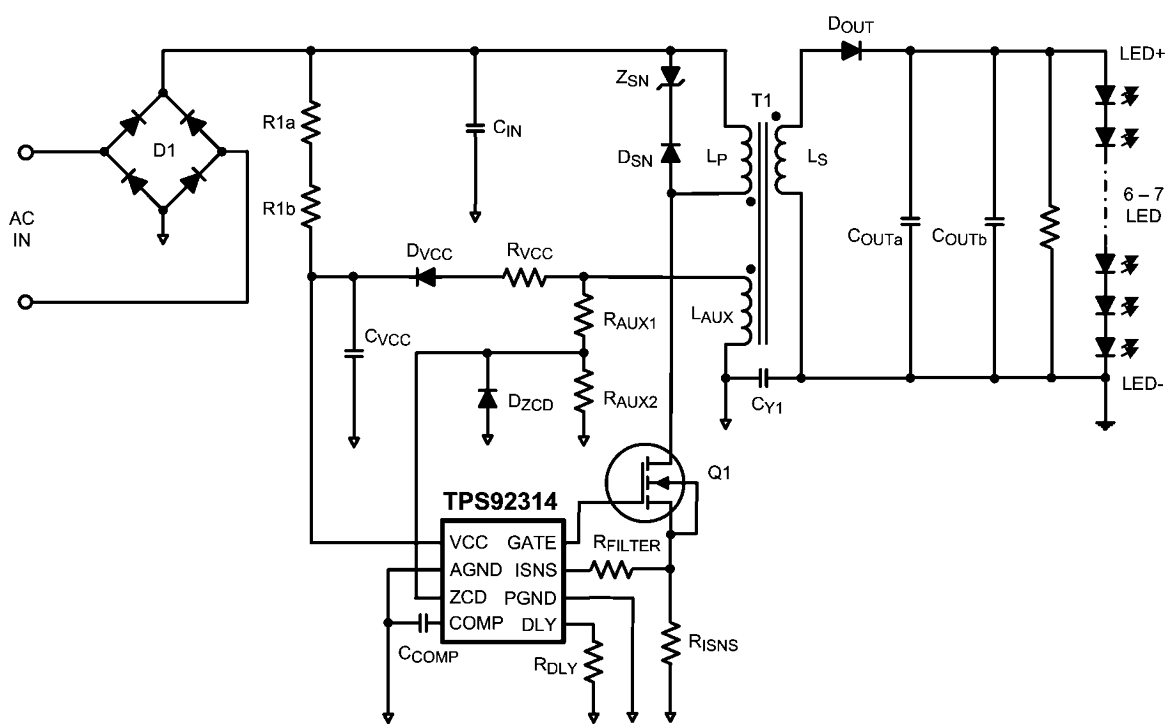

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FIGURE 1.

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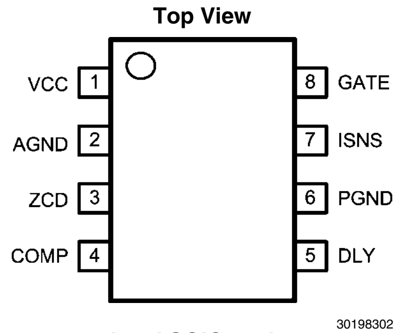
Connection Diagram



8–Lead SOIC package

Ordering Information

Order Number	Package Type	Package QTY	Supplied As
TPS92314D	SOIC-8	75	Rails
TPS92314DR	SOIC-8	2500	Tape and Reel
TPS92314AD	SOIC-8	75	Rails
TPS92314ADR	SOIC-8	2500	Tape and Reel

Pin Descriptions

Pin	Name	Description	Application Information
1	VCC	Power supply Input	This pin provides power to the internal control , connect a 10μF~20μF capacitor to ground for filtering.
2	AGND	Small signal Ground	Control signal ground return.
3	ZCD	Zero crossing detection input	The pin senses the voltage of the auxiliary winding for zero current detection.
4	COMP	Compensation network	Output of the error amplifier. Connect a capacitor from this pin to ground to determine the frequency response of average current control loop.
5	DLY	Delay control input	Connect a resistor from this pin to ground to set the delay between switching ON and OFF periods.
6	PGND	Power Ground	Gate driver ground return.
7	ISNS	Current sense voltage feedback	Switching MOSFET current sense pin.
8	GATE	Gate driver output	The output provides the gate driver of the power switching MOSFET.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.

VCC to GND	-0.3V to 40V
DLY,COMP,ZCD to GND	-0.3V to 7V
ISNS to GND	-0.3V to 7V
GATE to GND	(5ns,-6V) -0.3V to 12V
ESD Susceptibility:	
HBM (Note 3)	±2 kV
Storage Temperature Range	-65°C to +150°C
Junction Temperature (T_{J-MAX})	+150°C
Maximum Lead Temperature (Solder and Reflow)	260°C

Operating Conditions

Supply Voltage range VCC	13V to 35V
Junction Temperature (T_J)	-40°C to +125°C
Thermal Resistance (θ_{JA}) (Note 5)	162°C/W

Electrical Characteristics

V_{CC} = 18V unless otherwise indicated. Typicals and limits appearing in plain type apply for $T_A = T_J = +25°C$. Limits appearing in **boldface** type apply over the full Operating Temperature Range. Data sheet minimum and maximum specification limits are guaranteed by design, test or statistical analysis.

Symbol	Parameter	Conditions	Min	Typ (Note 4)	Max	Units
SUPPLY VOLTAGE INPUT (VCC)						
$V_{CC-UVLO}$	VCC Turn on threshold		22.5 / **21.7**	25.4	28.3 / **29.5**	V
	VCC Turn off threshold		10.4 / **10.1**	12.9	15.3 **/ 16.0**	V
	Hysteresis			12.5		
$I_{STARTUP}$	Startup Current	$V_{CC=}V_{CC-UVLO}$–3.0V		22.2	**25.8**	µA
V_{CC-OVP}	Over voltage protection threshold		**32.7**	35.5	**38.0**	V
I_{VCC}	Operating supply current	Not switching ,	**0.8**	1.2	**1.8**	mA
		65kHz switching		2.3	3.0	mA
ZERO CROSS DETECT (ZCD)						
I_{ZCD}	ZCD bais current	V_{ZCD}= 5V		0.01	1	uA
$V_{ZCD-OVP}$	ZCD over-voltage threshold		**3.9**	4.3	**4.7**	V
T_{OVP}	Over voltage de-bounce time			3		cycle
$V_{ZCD-ARM}$	ZCD Arming threshold	V_{ZCD} = Increasing	**1.04**	1.23	**1.42**	V
$V_{ZCD-TRIG}$	ZCD Trigger threshold	V_{ZCD} = Decreasing	**0.48**	0.6	**0.77**	V
$V_{ZCD-HYS}$	ZCD Hysteresis	$V_{ZCD-ARM}$-$V_{ZCD-TRIG}$		0.61		V
COMPENSATION (COMP)						
$I_{COMP-SOURCE}$	Internal reference current for primary side current regulation	V_{COMP} = 2.0V, V_{ISNS} = 0V, Measure at COMP pin		27		µA
gm_{ISNS}	ISNS error amp trans-conductance	ΔV_{ISNS} to ΔI_{COMP} @ V_{COMP} = 2.5V		96		µmho

Symbol	Parameter	Conditions	Min	Typ (Note 4)	Max	Units
DELAY CONTROL (DLY)						
V_{DLY}	DLY pin internal reference voltage		**1.21**	1.24	**1.3**	V
$I_{DLY\text{-}MAX}$	DLY source current	V_{DLY}= 0V	**250**	450		μA
CURRENT SENSE (ISNS)						
$V_{ISNS\text{-}OCP}$	Over Current Limit Detection Threshold	TPS92314	1.07	1.15	1.22	V
$V_{ISNS\text{-}OCP}$	Over Current Limit Detection Threshold	TPS92314A	1.90	2.0	2.10	V
I_{ISNS}	Current Sense Bias Current	V_{ISNS}= 5V	-1		1	μA
T_{OCP}	Over current Limit Detection Propagation Delay	Measure ISNS pin pulse width with V_{ISNS} = 5V		256		ns
GATE DRIVER (GATE)						
$V_{GATE\text{-}H}$	GATE low voltage	IGATE = 50mA source	**7.6**	9.4		V
$V_{GATE\text{-}L}$	GATE high drive voltage	IGATE = 50mA sink		85	**125**	mV
$t_{GATE\text{-}RISE}$	Rise Time	CLOAD = 1nF		94		ns
$t_{GATE\text{-}FALL}$	Fall Time	CLOAD = 1nF		16		ns
$T_{ON\text{-}MIN}$	Minimum ON time	With ZCD signal.	**311**	500	**900**	ns
$T_{ON\text{-}MAX}$	Maximum ON time		**27**	43.9	**61**	μs
$T_{OFF\text{-}MIN}$	Minimum OFF time		**1.00**	1.50	**1.93**	μs
$T_{OFF\text{-}MAX}$	Maximum OFF time	ZCD = GND	**67**	117	**151**	μs
$T_{OFF\text{-}START}$	Maximum OFF time when start up.	Maximum OFF time at first 511 switching after UVLO	**44**	78	**102**	μs
$T_{OFF\text{-}OCP}$	Maximum OFF time when OCP	OFF time when V_{ISNS} =4V.		233		μs
THERMAL SHUTDOWN						
TSD	Thermal shutdown temperature	(Note 2)		165		°C
	Thermal Shutdown hysteresis			20		°C

Note 1: Absolute maximum ratings are limits beyond which damage to the device may occur. Operating Ratings are conditions for which the device is intended to be functional, but device parameter specifications may not be guaranteed. For guaranteed specifications and test conditions, see the Electrical Characteristics. All voltages are with respect to the potential at the GND pin, unless otherwise specified.

Note 2: Internal thermal shutdown circuitry protects the device from permanent damage. Thermal shutdown engages at T_J = 165°C (typ.) and disengages at T_J = 145°C (typ).

Note 3: Human Body Model, applicable std. JESD22-A114-C.

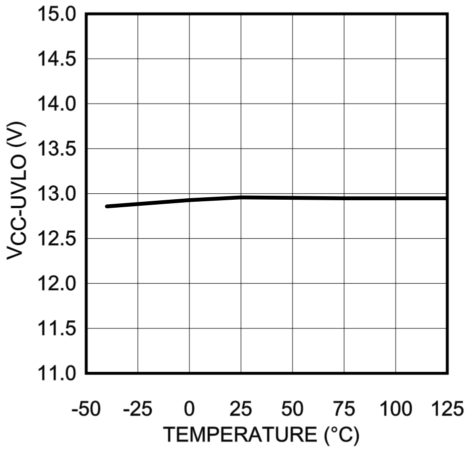
Note 4: Typical numbers are at 25°C and represent the most likely norm.

Note 5: This $R_{\theta JA}$ typical value determined using JEDEC specifications JESD51-1 to JESD51-11. However junction-to-ambient thermal resistance is highly boardlayout dependent. In applications where high maximum power dissipation exists, special care must be paid to thermal dissipation issues during board design. In high-power dissipation applications, the maximum ambient temperature may have to be derated. Maximum ambient temperature ($T_{A\text{-}MAX}$) is dependent on the maximum operating junction temperature ($T_{J\text{-}MAX\text{-}OP}$ = 125°C), the maximum power dissipation of the device in the application ($P_{D\text{-}MAX}$), and the junction-to ambient thermal resistance of the part/package in the application ($R_{\theta JA}$), as given by the following equation: $T_{A\text{-}MAX} = T_{J\text{-}MAX\text{-}OP} - (R_{\theta JA} \times P_{D\text{-}MAX})$.

Typical Performance Characteristics

All curves taken at V_{CC}=18V with configuration in typical application for driving seven power LEDs with I_{LED}=350mA shown in this datasheet. T_A=25°C, unless otherwise specified.

$V_{CC-UVLO}$ vs Temperature



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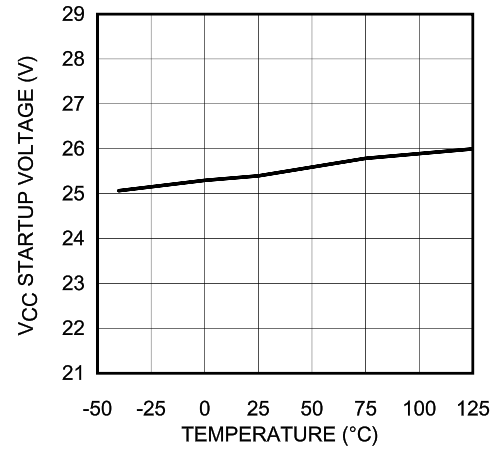
V_{CC} Startup Voltage vs Temperature



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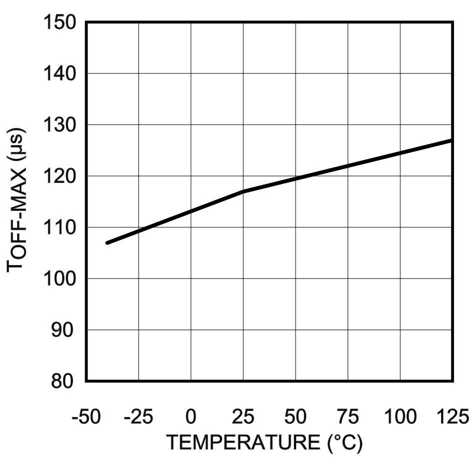
$T_{OFF-MAX}$ vs Temperature



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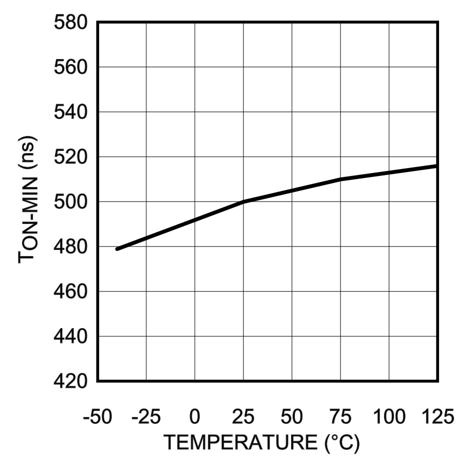
T_{ON-MIN} vs Temperature



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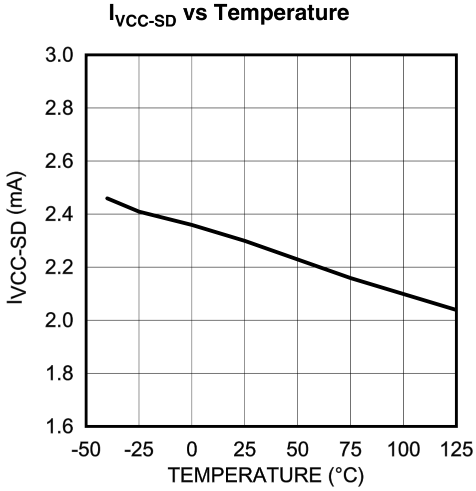
I_{VCC-SD} vs Temperature



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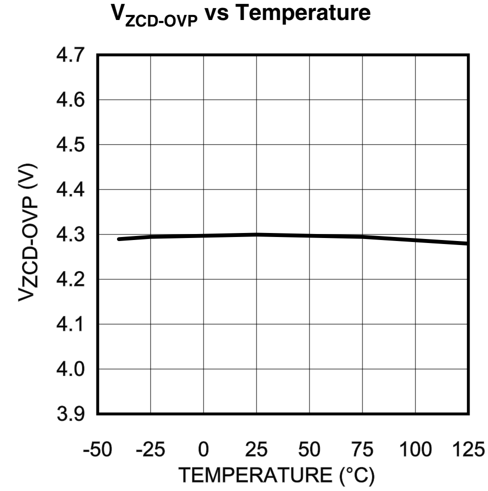
$V_{ZCD-OVP}$ vs Temperature



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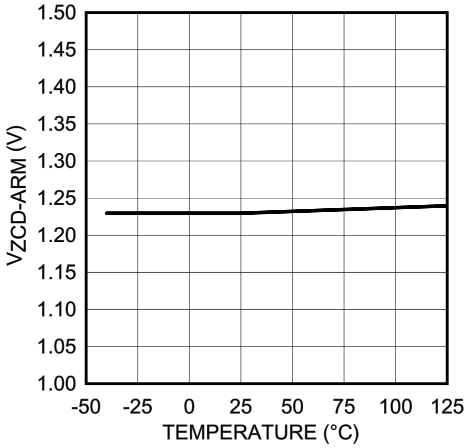
$V_{ZCD-ARM}$ vs Temperature



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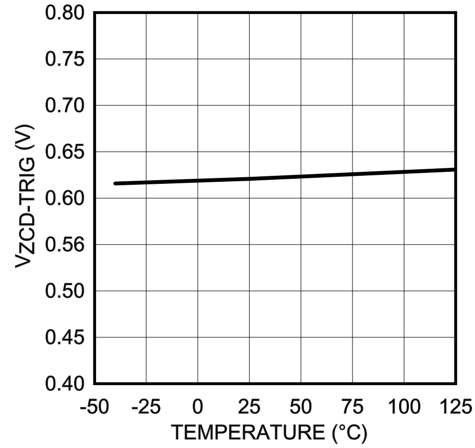
$V_{ZCD-TRIG}$ vs Temperature



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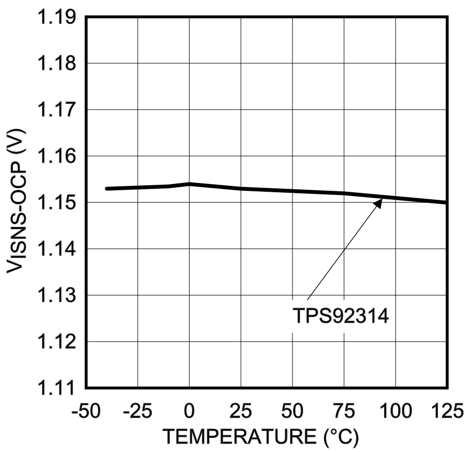
V_{ISNS_OCP} vs Temperature



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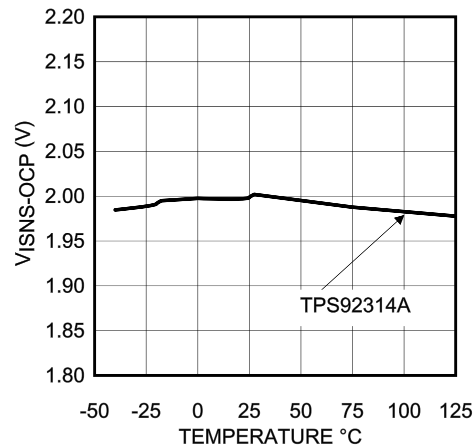
V_{ISNS_OCP} vs Temperature



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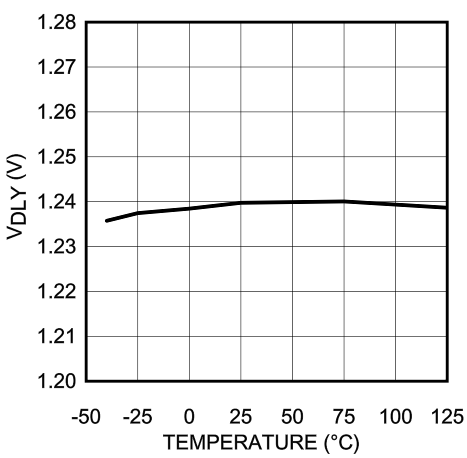
V_{DLY} vs Temperature



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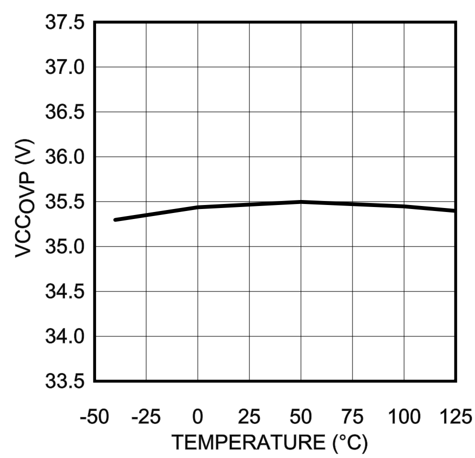
V_{CC-OVP} vs Temperature



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Simplified Internal Block Diagram

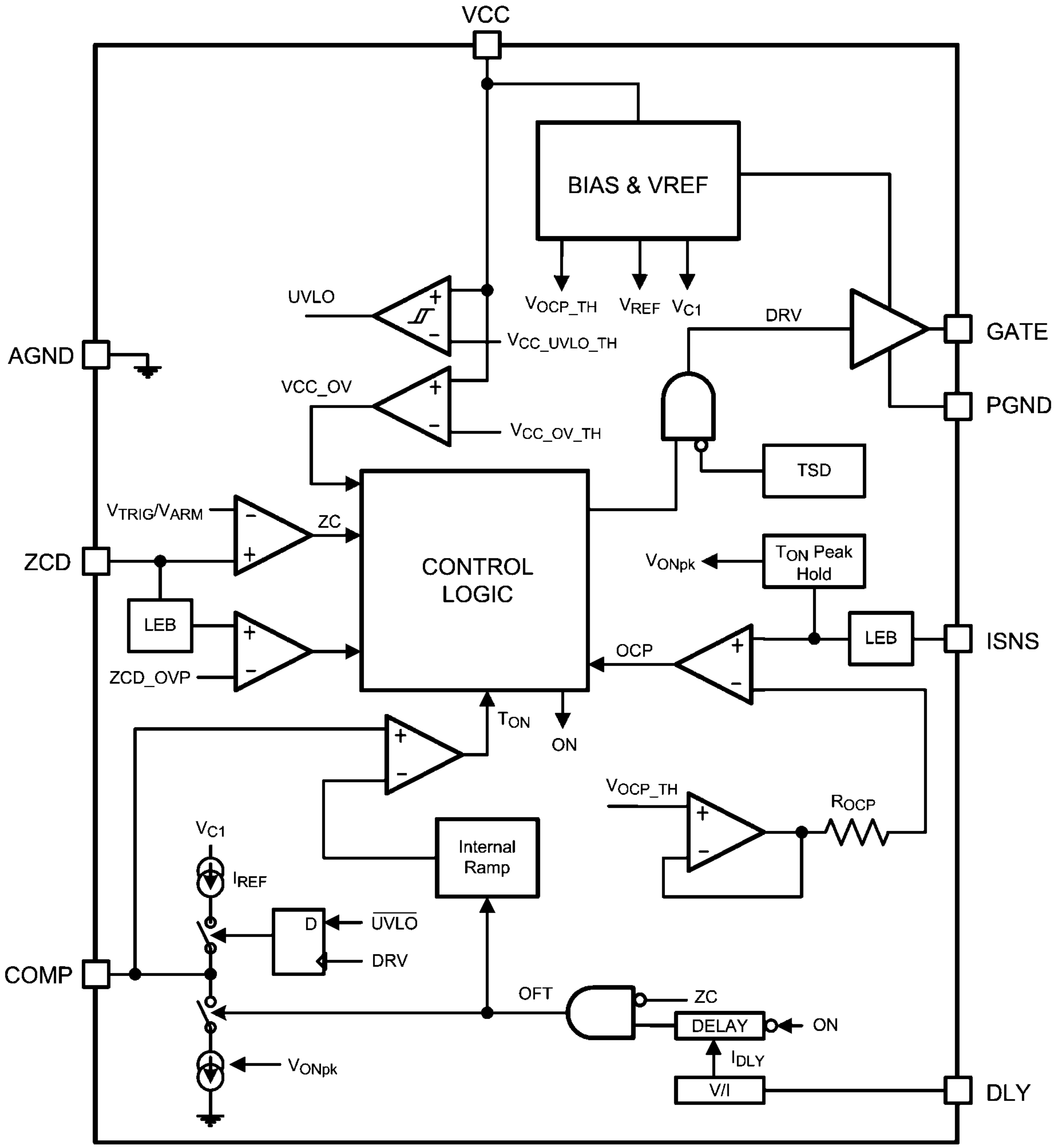


FIGURE 2. Simplified Block Diagram

Application Information

The TPS92314/14A is an off-line controller specifically designed to drive LEDs. This device operates in Critical Conduction Mode (CRM) with adaptive Constant ON-Time control, so that high power factor can be achieved naturally. The TPS92314/14A can be configured as an isolated or non-isolated off-line converter. Please refer to TPS92314/14A typical schematic Figure 1, on the front page, in the following discussion. The TPS92314/14A flyback converter consists of a transformer which includes three windings L_P, L_S and L_{AUX}.An external MOSFET Q_1 and inductor current sensing resistor R_{ISNS}. Secondary side components are secondary side transformer winding L_S, output diode D_{OUT}, and output capacitor C_{OUT}. An auxiliary winding is required, and serves two functions. Auxiliary power is developed from the winding to power the TPS92314/14A after start-up, and detect the zero crossing point due to the end of a complete switching cycle. During the on-period, Q_1 is turned on, and current flows through L_P, Q_1 and R_{ISNS} to ground, input energy is stored in the primary inductor L_P. Simultaneously, the I_{SNS} pin of the device monitors the voltage of the current sensing resistor R_{ISNS} to perform the cycle-by-cycle inductor current limit function. During the time MOSFET Q_1 is off, current flow in L_P ceases and the energy stored during the on cycle is released to output and auxiliary circuits. During Q_1 off-time current in the secondary winding L_S charges the output capacitor C_{OUT} through D_{OUT} and supplies the LED load. During Q_1 on-time, C_{OUT} is responsible to supply load current to LED load during subsequent on-period. Also during Q_1 off-time current is delivered to the auxiliary winding through D_{VCC} and powers the TPS92314/14A. The voltage across L_{AUX}, V_{LAUX} is fed back to the ZCD pin through a resistor divider network formed by R_{AUX1} and R_{AUX2} to perform zero crossing detection of V_{LAUX}, which determines the end of the off-period of a switching cycle. The next on period of a new cycle will be initiated after an inserted delay of 2 x t_{DLY}. The t_{DLY} is programmable by a single resistor connecting the DLY pin and ground. The setting of the delay time, t_{DLY} will be described in a separate paragraph. The driver signal t_{ON} time width is generated by comparing an internal generated saw-tooth waveform with the voltage on the COMP pin (V_{COMP}). Since V_{COMP} is slow varying, t_{ON} is nearly constant within an AC line cycle. The duration of the off-period (t_{OFF}) is determined by the rate of discharging of the secondary current through the transformer. Also,

$$I_{LS\text{-}PEAK} = n \times I_{LP\text{-}PEAK}$$

where n is the turn ratio of L_P and L_S. Figure 3 shows the typical waveforms in normal operation.

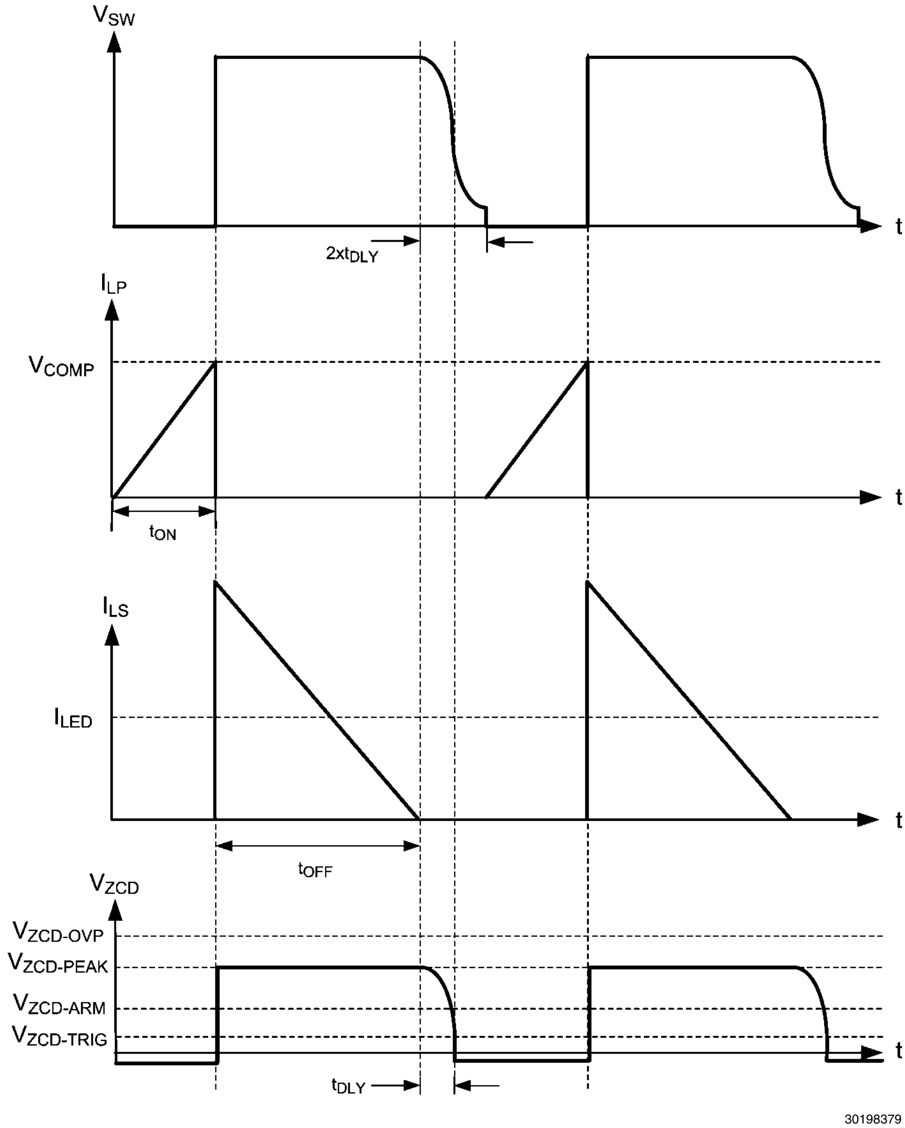


FIGURE 3. Primary and Secondary Side Current Waveforms

Startup Bias and UVLO

During startup, the TPS92314/14A is powered from the AC line through R_1 and bridge diode D_1 (Figure 1). In the startup state, most of the internal circuits of the TPS92314/14A are shut down in order to minimize internal quiescent current. When V_{CC} reaches the rising threshold of the $V_{CC\text{-}UVLO}$ (typically 26V), the TPS92314/14A is operating in a low switching frequency mode, where t_{ON} and t_{OFF} are fixed to 1.5µs and 72µs. When $V_{ZCD-PEAK}$ is higher than $V_{ZCD\text{-}ARM}$, the TPS92314/14A enters normal operation.

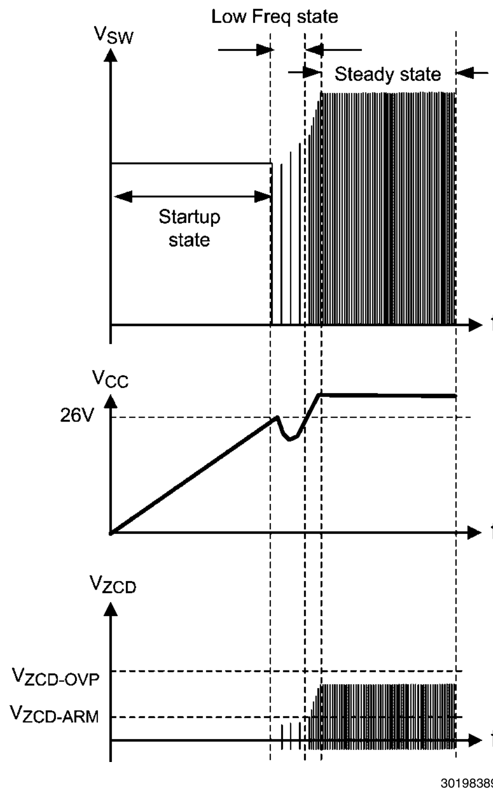


FIGURE 4. Start up Bias Waveforms

Zero Crossing Detection

To minimized the switching loss of the power MOSFET, a zero crossing detection circuit is embedded in the TPS92314/14A. V_{LAUX} is AC voltage coupled from V_{SW} by means of the transformer, with the lower part of the waveform clipped by D_{ZCD}. V_{LAUX} is fed back to the ZCD pin to detect a zero crossing point through a resistor divider network which consists of R_{AUX1} and R_{AUX2}. The next turn on time of Q_1 is selected V_{SW} is the minimum, an instant corresponding to a small delay after the zero crossing occurs. (Figure 5) The actual delay time depends on the drain capacitance of the Q_1 and the primary inductance of the transformer (L_P). Such delay time is set by a single external resistor as described in Delay Setting section.

During the off-period at steady state, V_{ZCD} reaches its maximum $V_{ZCD-PEAK}$ (Figure 3), which is scalable by the turn ratio of the transformer and the resistor divider network R_{AUX1} and R_{AUX2}. It is recommended that $V_{ZCD-PEAK}$ is set to 3V during normal operation.

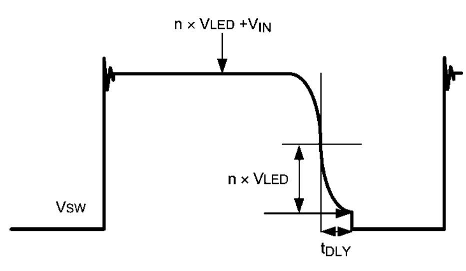


FIGURE 5. Switching Node Waveforms

Delay Time Setting

In order to reduce EMI and switching loss, the TPS92314/14A inserts a delay between the off-period and the on-period. The delay time is set by a single resistor which connects across the DLY pin and ground, and their relationship is shown in Figure 6. The optimal delay time depends on the resonance frequency between L_P and the drain to source capacitance of Q_1 (C_{DS}). Circuit designers should optimize the delay time according to the following equation.

$$f_{SW} = \frac{1}{2\pi\sqrt{L_P C_{DS}}}$$

$$t_{DLY} = \frac{\pi\sqrt{L_P C_{DS}}}{2}$$

After determining the delay time, t_{DLY} can be implemented by setting R_{DLY} according to the following equation:

$$R_{DLY} = K_{DLY}(t_{DLY} - 105ns)$$

where K_{DLY} = 32MΩ/ns is a constant.

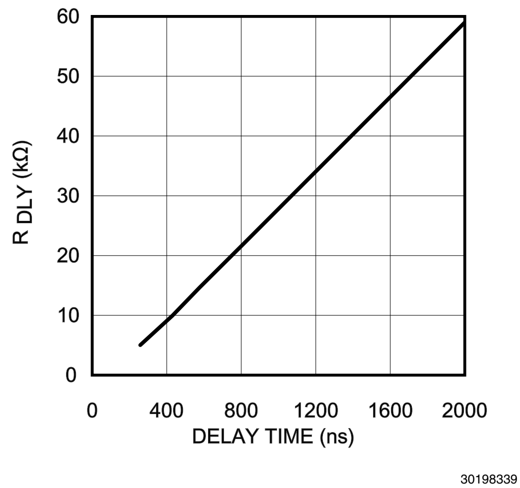


FIGURE 6. Delay Time Setting

Protection Features

OUTPUT OPEN CIRCUIT PROTECTION

The open circuit protection can be trigger through ZCD pin or VCC pin. If the LED string is disconnected from the output of the TPS92314/14A, The secondly output voltage (V_{LED}) and AUX wiring voltage $V_{ZCD\text{-}PEAK}$ will increases. IF $V_{ZCD\text{-}PEAK}$ is greater than $V_{ZCD\text{-}OVP}$ for 3 continues switching cycles or VCC voltage higher than V_{CCOVP} threshold, Over Voltage Protection (OVP) protection will be trigger. At the meantime, switching of Q_1 will stop and V_{CC} will decreases until it drops below the falling threshold of $V_{CC\text{-}UVLO}$, the controller will restarts automatically and enter into startup state (Figure 8).

VCC OVP PROTECTION

The TPS92314/14A has a built-in over voltage protection feature. It can be trigger through the VCC pin when over $V_{CC\text{-}OVP}$ threshold. Once the $V_{CC\text{-}OVP}$ triggered, the output gate signal will pull low and VCC will decrease until it drops below the $V_{CC\text{-}UVLO}$, the controller will restarts automatically.

OUTPUT SHORT CIRCUIT PROTECTION

If the LED string is shorted, the voltage of AUX wiring ($V_{ZCD\text{-}PEAK}$) will decrease, and as $V_{ZCD\text{-}PEAK}$ voltage decrease below $V_{ZCD\text{-}TRIG}$, the TPS92314/14A will enter low switching frequency operation. During low switching frequency operation, power supplied from L_{AUX} to V_{CC} is not enough to maintain V_{CC}. If the short remains V_{CC} will drop below the falling threshold of $V_{CC\text{-}UVLO}$, the TPS92314/14A will attempt to restart at this time (Figure 7). When the short is removed the TPS92314/14A will restore to steady state operation.

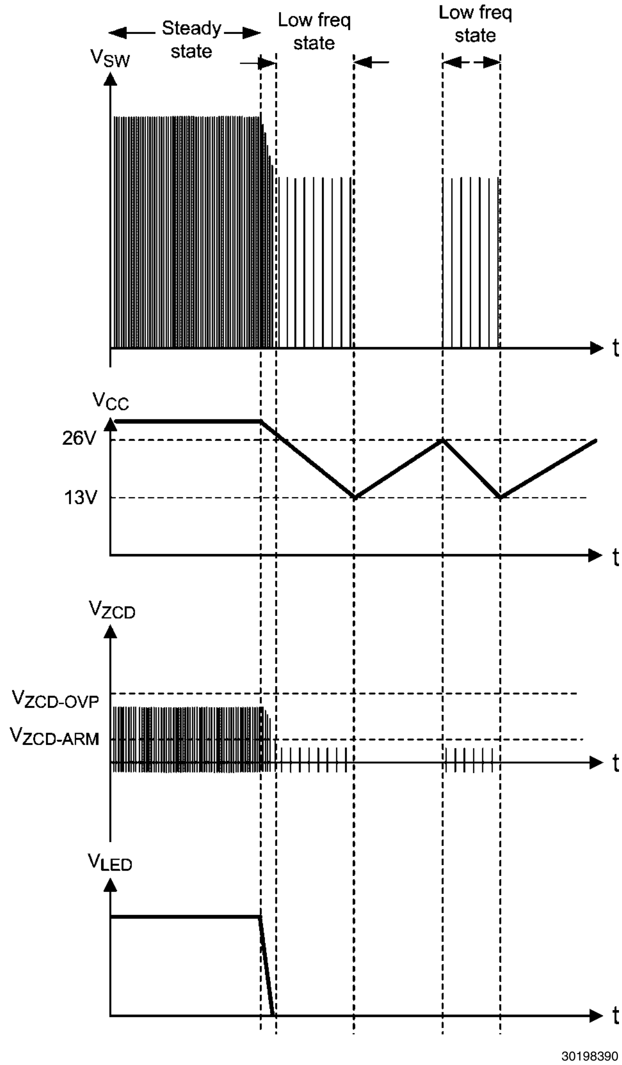


FIGURE 7. Output Short Circuit waveforms

OVER CURRENT PROTECTION

Over Current Protection (OCP) limits the drain current of MOSFET and prevents inductor / transformer saturation. When V_{ISNS} reaches a threshold, OCP function will be triggered, controller gate drive will pull low and OFF time will extends to 233µs, also C_{COMP} capacitor will be discharged by internal switch and gate drive ON time will force to minimum in next cycle.

THERMAL PROTECTION

Thermal protection is implemented by an internal thermal shutdown circuit, which activates at 165°C (typically). In this case, the switching power MOSFET will turn off. Capacitor C_{VCC} will discharge until UVLO. If the junction temperature of the TPS92314/14A falls back below 145°C, the TPS92314/14A resumes normal operation.

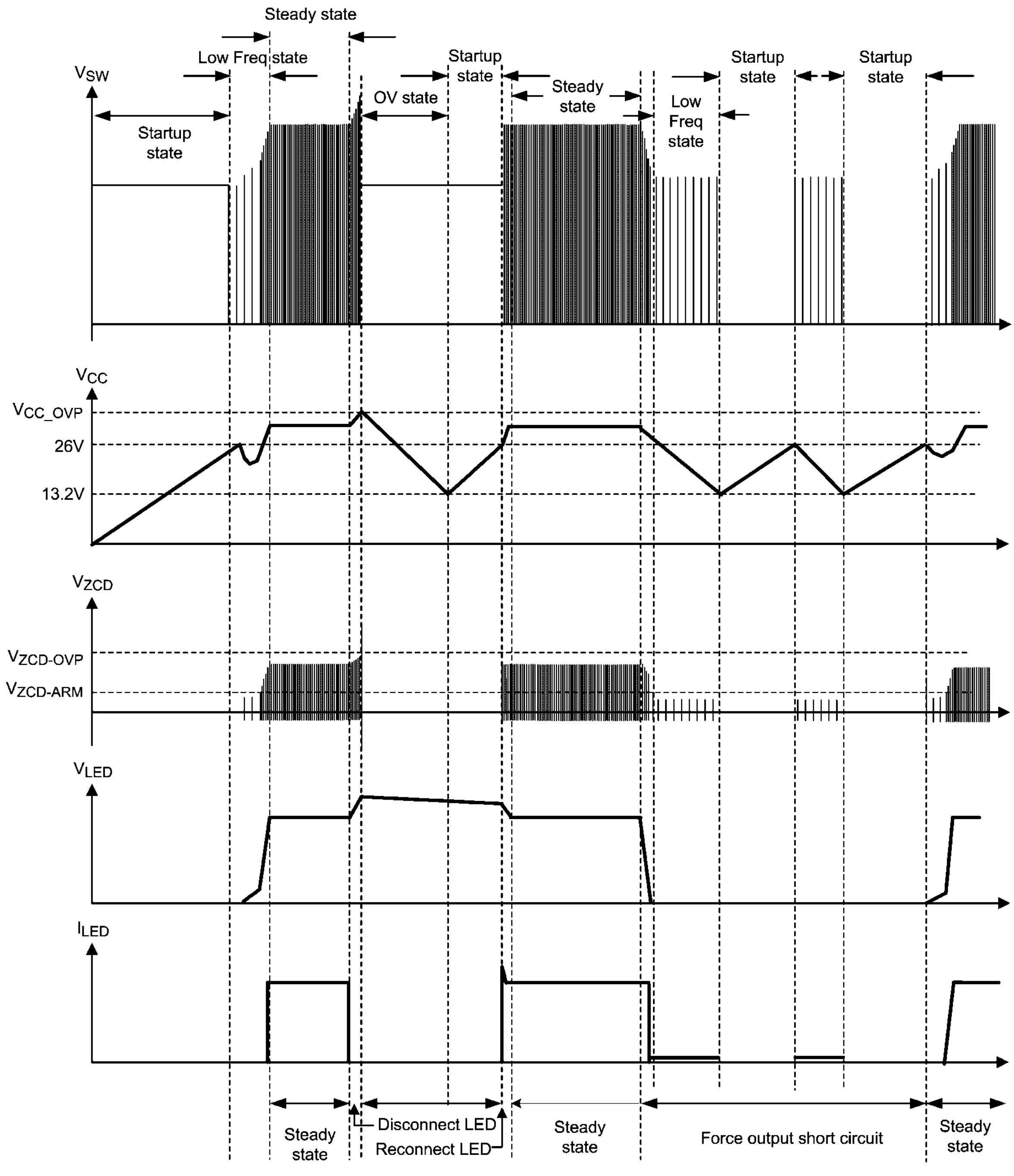


FIGURE 8. Auto Restart Operation

Design Example

The following design example illustrates the procedures to calculate the external component values for the TPS92314/14A isolated single stage fly-back LED driver with PFC.

Design Specifications:

Input voltage range, V_{AC_RMS} = 85VAC – 132VAC

Nominal input voltage, $V_{AC\_RMS(NOM)}$ = 110VAC

Number of LED in serial =7

LED current, I_{LED} = 350mA

Forward voltage drop of single LED = 3.0V

Forward voltage of LED stack, V_{LED} = 21V

Key operating Parameters:

Converter minimum switching frequency, f_{SW} = 75kHz

Output rectifier maximum reverse voltage, $V_{DOUT(MAX)}$ = 100V

Power MOSFET rating, $V_{Q1(MAX)}$ =800V

Power MOSFET Output Capacitance, C_{DS} = 37pF (estimated)

Nominal output power, P_{OUT} = 8W

START UP BIAS RESISTOR

During start up, the V_{CC} will be powered by the rectified line voltage through external resistor, R_1. The V_{CC} start up current, $I_{VCC(SU)}$ must set in the range $I_{VCC(MIN)} > I_{VCC(SU)} > I_{STARTUP(MAX)}$ to ensure proper restart operation during OVP fault at maximum voltage input. In this example, a value of 0.88mA is suggested. The resistance of R_1 can be calculated by dividing the nominal input voltage in RMS by the start up current suggested.

So, R_{AC} = 132V / 0.88mA = 150KΩ is recommended.

TRANSFORMER TURN RATIO

The transformer winding turn ratio, n is governed by the MOSFET Q1 maximum rated voltage, ($V_{Q1(MAX)}$), highest line input peak voltage ($V_{AC\text{-}PEAK}$) and output diode maximum reverse voltage rating ($V_{OUT(MAX)}$). The output diode rating limits the lower bound of the turn ratio and the power MOSFET rating provide the upper bound of the turn ratio. The transformer turn ratio must be selected in between the bounds. If the maximum reverse voltage of D_{OUT} ($V_{DOUT(MAX)}$) is 100V. the minimum transformer turn ratio can be calculated with the equation in below.

$$n > \frac{V_{AC\text{-}PEAK}}{\left(V_{DOUT(MAX)} - V_{LED}\right)}$$

$$n > \frac{132 \times \sqrt{2}}{100-30} = 2.33$$

In operation, the voltage at the switching node, V_{SW} must be small than the MOSFET maximum rated voltage $V_{Q1(MAX)}$, For reason of safety, 10% safety margin is recommended. Hence, 90% of $V_{Q1(MAX)}$ is used in the following equation.

$$n < \frac{V_{Q1(MAX)} \times 0.9 - V_{AC\text{-}PEAK} - V_{os}}{V_{LED(MAX)}}$$

$$n < \frac{800 \times 0.9 - 132\sqrt{2} - 50}{30} = 18.8$$

where V_{OS} is the maximum switching node overshoot voltage allowed, in this example, 50V is assumed. As a rule of thumb, lower turn ratio of transformer can provide a better line regulation and lower secondly side peak current. In here, turn ratio n = 3.8 is recommended.

SWITCHING FREQUENCY SELECTION

TPS92314/14A can operate at high switching frequency in the range of 60kHz to 150kHz. In most off-line applications, with considering of efficiency degradation and EMC requirements, the recommended switching frequency range will be 60kHz to 80kHz. In this design example, switching frequency at 75kHz is selected.

SWITCHING ON TIME

The maximum power switch on-time, t_{ON} depends on the low line condition of $85V_{AC}$. At $85V_{AC}$ the switching frequency was chosen at 75kHz. This transformer design will follow the formulae as shown below.

$$t_{ON}=\frac{1}{f_{sw}\left(\frac{V_{AC\_MIN\_PEAK}}{n x V_{LED}}+1\right)}$$

$$t_{ON}=\frac{1}{75000\left(\frac{85\sqrt{2}}{3.8 \times 21}+1\right)}=5.3\,\mu s$$

TRANSFORMER PRIMARY INDUCTANCE

The primary inductance, L_P of the transformer is related to the minimum operating switching frequency f_{SW}, converter output power P_{OUT}, system efficiency η and minimum input line voltage $V_{AC\_RMS(MIN)}$. For CRM operation, the output power, P_{OUT} can be described by the equation in below.

$$P_{OUT}=\eta x \frac{1}{2} L_P x I_{LP\text{-}PEAK}{}^2 x f_{SW}$$

By re-arranging terms, the transformer primary inductance required in this design example can be calculated with the equation follows:

$$L_P=\frac{\eta x V_{AC\_RMS(MIN)}{}^2 t_{ON}{}^2}{2 x P_{OUT} x \frac{1}{f_{sw}}}$$

The converter minimum switching frequency is 75kHz, t_{ON} is 5.3µs, $V_{AC\_RMS(MIN)}$ = 85V and P_{OUT} = 8W, assume the system efficiency, η = 85%. Then,

$$L_P=\frac{0.85 x (85)^2 x (5.3\,\mu)^2}{2x8x13.3\,\mu}=0.81 mH$$

From the calculation in above, the inductance of the primary winding required is 0.81mH.

Calculate The Current Sensing Resistor

After the primary inductance and transformer turn ratio is determined, the current sensing resistor, R_{ISNS} can be calculated.

The resistance for R_{ISNS} is governed by the output current and transformer turn ratio, the equation in below can be used.

$$R_{ISNS}= n\ x \left(\frac{V_{REF}}{I_{LED}}\right)$$

where V_{REF} is fixed to 0.14V internally.

Transformer turn ratio, $N_P : N_S$ is 3.8 : 1 and I_{LED} = 0.35A

$$R_{ISNS}=3.8\times\frac{0.14}{0.35}=1.52\,\Omega$$

In Figure 9, resistor R_{FILTER} is used to reduce the high frequency noise into ISNS pin. the typical value is 300 x R_{ISNS} .

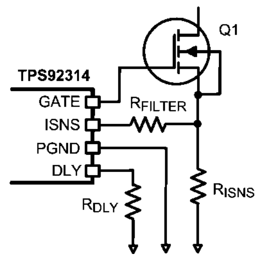


FIGURE 9. R_{ISNS} Resistor Interface

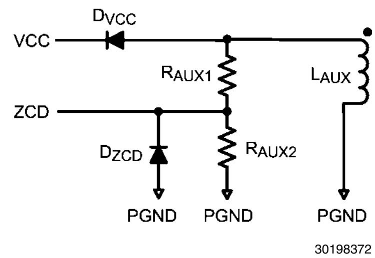


FIGURE 10. Auxiliary Winding Interface to ZCD

Auxiliary Winding Interface To ZCD

In Figure 10, R_{AUX1} and R_{AUX2} forms a resistor divider which sets the thresholds for over voltage protection of $V_{LED,}$ $V_{ZCD\text{-}OVP}$, and $V_{ZCD\text{-}PEAK}$. Before the calculation, we need to set the voltage of the auxiliary winding, V_{LAUX} at open circuit.

For example :

Assume the nominal forward voltage of LED stack (V_{LED}) is 21V.

To avoid false triggering ZCD_{OVP} voltage threshold at normal operation, select ZCD_{OVP} voltage at 1.3 times of the V_{LED} is typical in most applications. In case the transformer leakage is higher, the ZCD_{OVP} threshold can be set to 1.5 times of the V_{LED}.

In this design example, open circuit AUX winding OVP voltage threshold is set to 30V. Assume the current through the AUX winding is 0.4mA typical.

As a result, R_{AUX1} is 66kΩ and R_{AUX2} is 12kΩ.

Auxiliary Winding V_{cc} Diode Selection

The VCC diode D_{VCC} provides the supply current to the converter, low temperature coefficient , low reverse leakage and ultra fast diode is recommended.

Compensation Capacitor And Delay Timer Resistor Selection

To achieve PFC function with a constant on time flyback converter, a low frequency response loop is required. In most applications, a 4.7µF C_{COMP} capacitor is suitable for compensation.

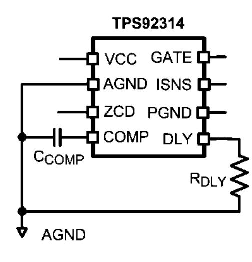


FIGURE 11. Compensation and DLY Timer connection

The resistor R_{DLY} connecting the DLY pin to ground is used to set the delay time between the ZCD trigger to power MOSFET turn on. The delay time required can be calculated with the parasitic capacitance at the drain of MOSFET to ground and primary inductance of the transformer. Equation in below can be used to find the delay time and Figure 6 in previous page can help to find the resistance once the delay time is calculated

$$t_{DLY} = \frac{\pi\sqrt{L_P C_{DS}}}{2}$$

For example, using a transformer with primary inductance L_P = 1mH, and power MOSFET drain to ground capacitor C_{DS}=37pF, the t_{DLY} can be calculated by the upper equation. As a result, t_{DLY}=302ns and R_{DLY} is 6.31kΩ. The delay time may need to change according to the primary inductance of the transformer. The typical level of output current will shift if inappropriate delay time is chosen.

Output Flywheel Diode Selection

To increase the overall efficiency of the system, a low forward voltage schottky diode with appropriate rating should be used.

Primary Side Snubber Design

The leakage inductance can induce a high voltage spike when power MOSFET is turned off. Figure 12 illustrate the operation waveform. A voltage clamp circuit is required to protect the power MOSFET. The voltage of snubber clamp (V_{SN}) must be higher than the sum of over shoot voltage (V_{OS}), LED open load voltage multiplied by the transformer turn ratio (n). In this examples, the V_{OS} is 50V and LED maximum voltage, $V_{LED(MAX)}$ is 30V, transformer turn ratio is 3.8. The snubber voltage required can be calculated with following equations.

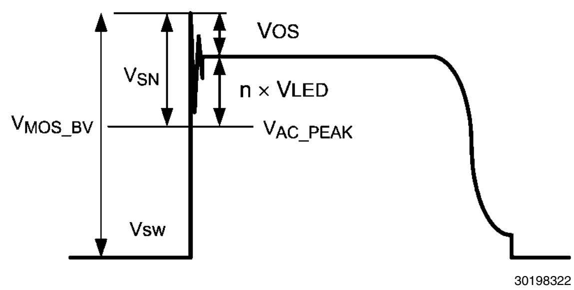


FIGURE 12. Snubber Waveform

$$V_{SN} > V_{OS} + V_{LED(MAX)} \times n$$

where n is the turn ratio of the transformer.

$$V_{SN} > 50V + 30V \times 3.8 = 164V$$

At the same time, sum of the snubber clamp voltage and V_{AC} peak voltage (V_{AC_PEAK}) must be smaller than the MOSFET breakdown voltage (V_{MOS_BV}). By re-arranging terms, equation in below can be used.

$$V_{SN} < V_{MOS\_BV} - V_{AC}\sqrt{2}$$

$$V_{SN} < 800 - 132 \times \sqrt{2} = 614V$$

In here, snubber clamp voltage, V_{SN} = 250V is recommended.

Output Capacitor

The capacitance of the output capacitor is determined by the equivalent series resistance (ESR) of the LED, R_{LED} and the ripple current allowed for the application. The equation in below can be used to calculate the required capacitance.

$$C_{OUT} = \frac{\sqrt{\left(2\frac{I_{LED}}{\Delta I_{LED}}\right)^2 - 1}}{4 \times \pi \times f_{AC} R_{LED}}$$

Assume the ESR of the LED stack contains 7 LEDs and is 2.6Ω, AC line frequency f_{AC} is 60Hz.

In this example, LED current I_{LED} is 350mA and output ripple current is 30% of I_{LED}:

$$C_{OUT} = \frac{\sqrt{\left(\frac{2x0.35}{0.3x0.35}\right)^2 - 1}}{4x\pi x60x7x2.6}$$

Then, C_{OUT} = 480µF.

In here, a 470µF output capacitor with 10µF ceramic capacitor in parallel is suggested.

PCB Layout Considerations

The performance of any switching power supplies depend as much upon the layout of the PCB as the component selection. Good layout practices are important when constructing the PCB. The layout must be as neat and compact as possible, and all external components must be as close as possible to their associated pins. High current return paths and signal return paths must be separated and connect together at single ground point. All high current connections must be as short and direct as possible with thick traces. The drain voltage of the MOSFET should be connected close to the transformer pin with short and thick trace to reduce potential electromagnetic interference. For off-line applications, one more consideration is the safety requirements. The clearance and creepage to high voltage traces must be complied to all applicable safety regulations.

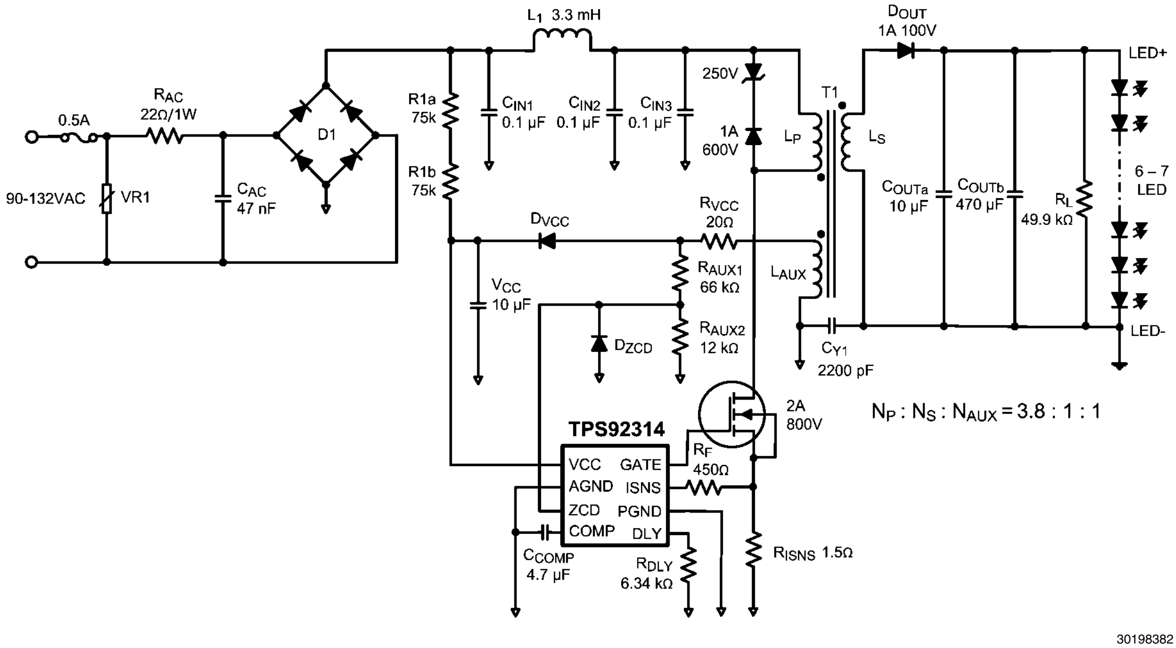


FIGURE 13. Isolated topology schematic

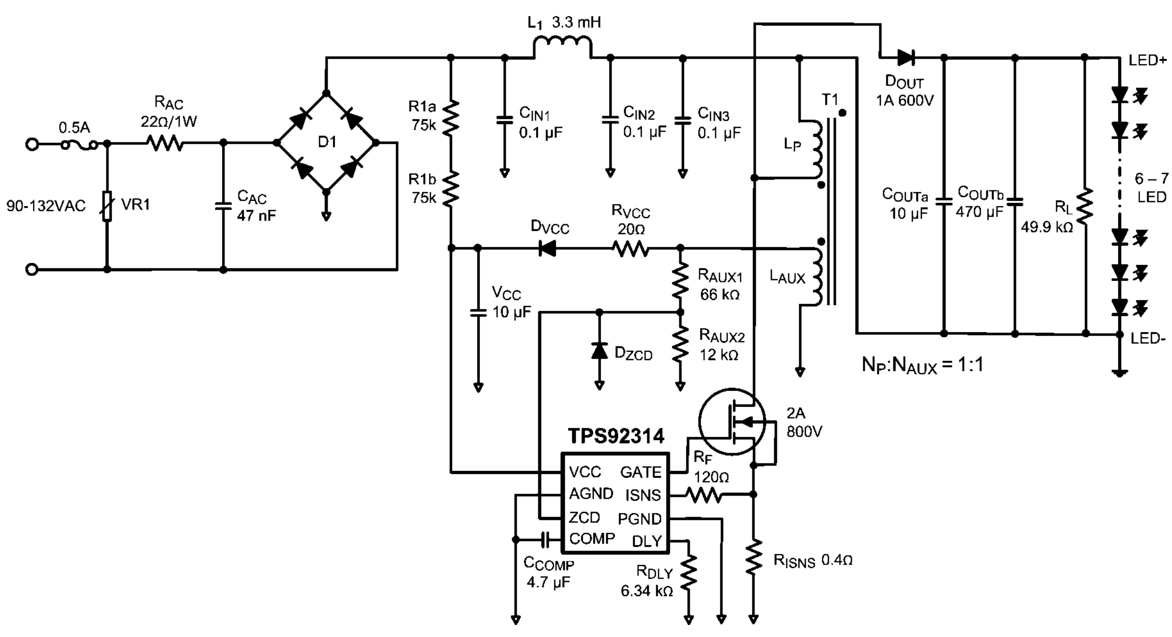
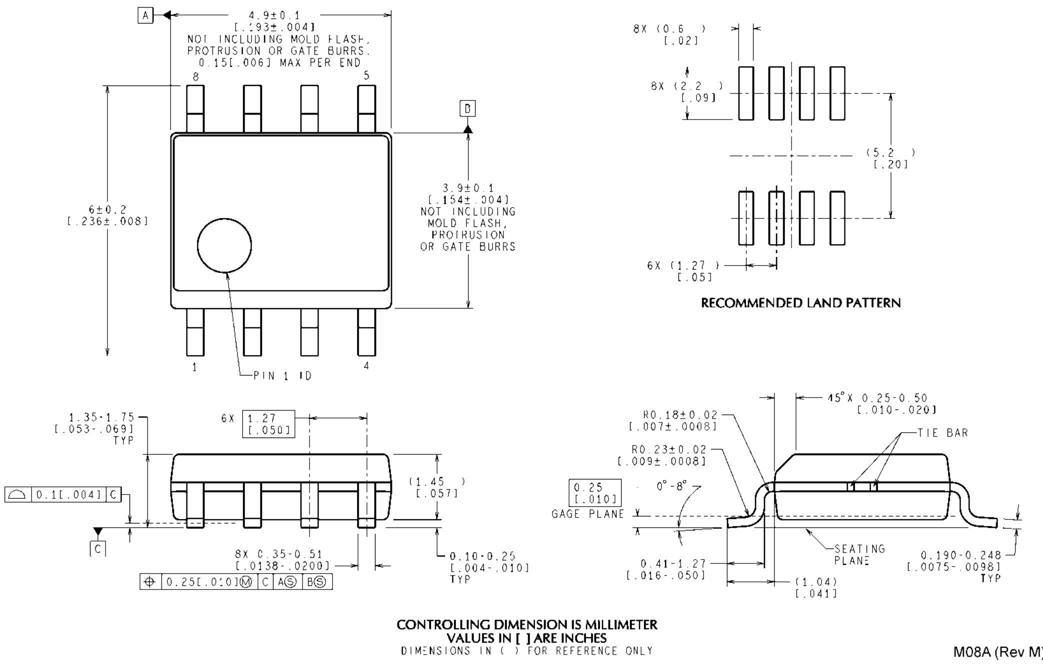


FIGURE 14. Non-isolated topology schematic

Physical Dimensions inches (millimeters) unless otherwise noted



SOIC-8 Pin Package (mm)
For Ordering, Refer to Ordering Information Table
NS Package Number M08A

Notes