74LVX257

LOW VOLTAGE QUAD 2 CHANNEL MULTIPLEXER (3-STATE)

- HIGH SPEED: t_{PD} = 5.8 ns (TYP.) at V_{CC} = 3.3V
- INPUT VOLTAGE LEVEL: V_{IL} = 0.8V, V_{IH} = 2V at V_{CC} = 3V
- LOW POWER DISSIPATION: I_{CC} = 4 µA (MAX.) at T_A = 25 °C
- LOW NOISE: V_{OLP} = 0.3 V (TYP.) at V_{CC} = 3.3V
- SYMMETRICAL OUTPUT IMPEDANCE: $|I_{OH}| = I_{OL}$ = 4 mA (MIN)
- BALANCED PROPAGATION DELAYS: $t_{PLH} \cong t_{PHL}$
- OPERATING VOLTAGE RANGE: V_{CC} (OPR) = 2V to 3.6V (1.2V Data Retention)
- PIN AND FUNCTION COMPATIBLE WITH 74 SERIES 257
- IMPROVED LATCH-UP IMMUNITY
- POWER DOWN PROTECTION ON INPUTS

M
(Micro Package)

T
(TSSOP Package)

ORDER CODES :

74LVX257M 74LVX257T

DESCRIPTION

The 74LVX257 is an advanced high-speed CMOS QUAD 2 CHANNEL MULTIPLEXER (3-STATE) fabricated with sub-micron silicon gate and double-layer metal wiring C^2MOS technology.

It has similar high speed performance of equivalent Bipolar Schottky TTL combined with true CMOS low power dissipation.

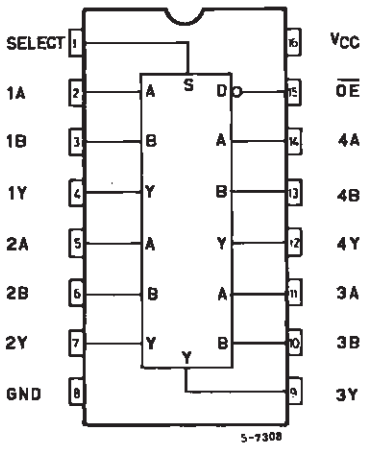
It is composed of four independent 2 channel multiplexers with common SELECT and ENABLE INPUT. The 74LVX257 is a non inverting multiplexer.

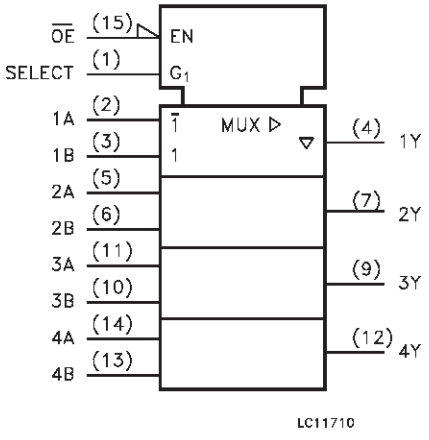
When the ENABLE INPUT is held "High", all outputs become high impedance state. If SELECT INPUT is held "Low", "A" data is selected, when SELECT INPUT is "High", "B" data is chosen.

Power down protection is provided on all inputs and 0 to 7V can be accepted on inputs with no regard to the supply voltage. This device can be used to interface 5V to 3V.

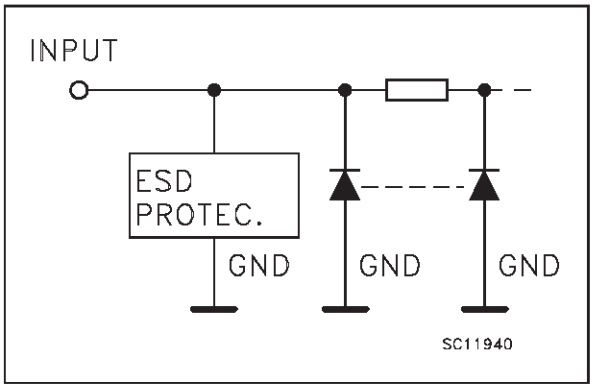
All inputs and outputs are equipped with protection circuits against static discharge, giving them 2KV ESD immunity and transient excess voltage.

PIN CONNECTION AND IEC LOGIC SYMBOLS





INPUT EQUIVALENT CIRCUIT



PIN DESCRIPTION

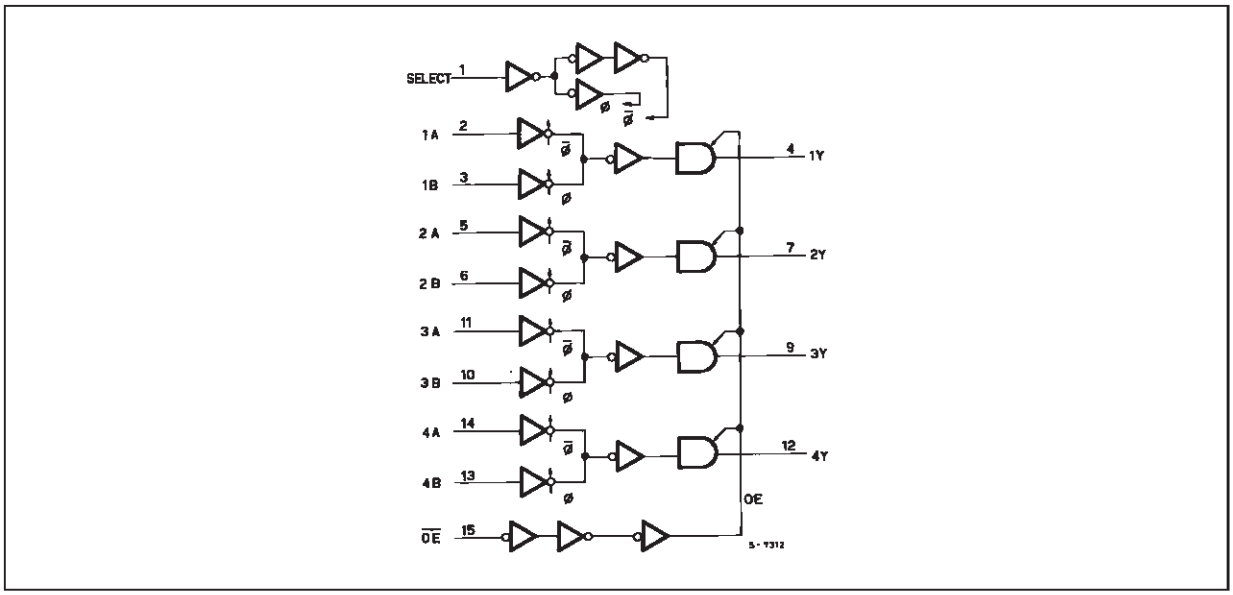
PIN No	SYMBOL	NAME AND FUNCTION
1	SELECT	Common Data Select Input
2, 5, 14, 11	1A to 4A	Data Inputs From Source A
3, 6, 13, 10	1B to 4B	Data Inputs from Source B
4, 7, 12, 9	1Y to 4Y	3 State Multiplexer Outputs
15	$\overline{OE}$	3 State Output Enable Input (Active LOW)
8	GND	Ground (0V)
16	V_{CC}	Positive Supply Voltage

TRUTH TABLE

INPUTS				OUTPUTS
$\overline{OE}$	SELECT	A	B	Y
H	X	X	X	Z
L	L	L	X	L
L	L	H	X	H
L	H	X	L	L
L	H	X	H	H

X = DON'T CARE Z = HIGH IMPEDANCE

LOGIC DIAGRAM



This logic diagram has not be used to estimate propagation delays

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7.0	V
V_I	DC Input Voltage	-0.5 to +7.0	V
V_O	DC Output Voltage	-0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	- 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Current	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage (note 1)	2 to 3.6	V
V_I	Input Voltage	0 to 5.5	V
V_O	Output Voltage	0 to V_{CC}	V
T_{op}	Operating Temperature:	-40 to +85	°C
dt/dv	Input Rise and Fall Time (V_{CC} = 3V) (note 2)	0 to 100	ns/V

1) Truth Table guaranteed: 1.2V to 3.6V
2) V_{IN} from 0.8V to 2V

DC SPECIFICATIONS

Symbol	Parameter	Test Conditions			Value					Unit
		V_{CC} (V)			T_A = 25 °C			-40 to 85 °C		
					Min.	Typ.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0			1.5			1.5		V
		3.0			2.0			2.0		
		3.6			2.4			2.4		
V_{IL}	Low Level Input Voltage	2.0					0.5		0.5	V
		3.0					0.8		0.8	
		3.6					0.8		0.8	
V_{OH}	High Level Output Voltage	2.0	V_I(*) = V_{IH} or V_{IL}	I_O=-50 µA	1.9	2.0		1.9		V
		3.0		I_O=-50 µA	2.9	3.0		2.9		
		3.0		I_O=-4 mA	2.58			2.48		
V_{OL}	Low Level Output Voltage	2.0	V_I(*) = V_{IH} or V_{IL}	I_O=50 µA		0.0	0.1		0.1	V
		3.0		I_O=50 µA		0.0	0.1		0.1	
		3.0		I_O=4 mA			0.36		0.44	
I_I	Input Leakage Current	3.6	V_I = 5.5V or GND				±0.1		±1	µA
I_{OZ}	3 State Output Leakage Current	3.6	V_I = V_{IH} or V_{IL} V_O = V_{CC} or GND				±0.25		±2.5	µA
I_{CC}	Quiescent Supply Current	3.6	V_I = V_{CC} or GND				4		40	µA

(*) All outputs loaded.

DYNAMIC SWITCHING CHARACTERISTICS

Symbol	Parameter	Test Conditions		Value					Unit
		V_{CC} (V)		T_A = 25 °C			-40 to 85 °C		
				Min.	Typ.	Max.	Min.	Max.	
V_{OLP}	Dynamic Low Voltage Quiet Output (note 1, 2)	3.3	C_L = 50 pF		0.3	0.5			V
V_{OLV}				-0.5	-0.3				
V_{IHD}	Dynamic High Voltage Input (note 1, 3)	3.3				2			
V_{ILD}	Dynamic Low Voltage Input (note 1, 3)	3.3		0.8					

1) Worst case package

2) Max number of outputs defined as (n). Data inputs are driven 0V to 3.3V, (n -1) outputs switching and one output at GND

3) max number of data inputs (n) switching. (n-1) switching 0V to 3.3V. Inputs under test switching: 3.3V to threshold (V_{ILD}), 0V to threshold (V_{IHD}). f=1MHz

AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 3$ ns)

Symbol	Parameter	Test Condition			Value					Unit
		V_{CC} (V)	C_L (pF)		T_A = 25 °C			-40 to 85 °C		
					Min.	Typ.	Max.	Min.	Max.	
t_{PLH} t_{PHL}	Propagation Delay Time A, B to Y	2.7	15				13.0	1.0	15.4	ns
		2.7	50				18.0	1.0	20.3	
		3.3(*)	15			5.8	9.3	1.0	11.0	
		3.3(*)	50			8.3	12.8	1.0	14.5	
t_{PLH} t_{PHL}	Propagation Delay Time SELECT to Y	2.7	15				15.4	1.0	18.2	ns
		2.7	50				20.3	1.0	23.1	
		3.3(*)	15			7.0	11.0	1.0	13.0	
		3.3(*)	50			9.5	14.5	1.0	16.5	
t_{PZL} t_{PZH}	Output Enable Time	2.7	15	R_L = 1 KΩ			14.7	1.0	17.5	ns
		2.7	50				19.6	1.0	22.4	
		3.3(*)	15			6.7	10.5	1.0	12.5	
		3.3(*)	50			9.2	14.0	1.0	16.0	
t_{PLZ} t_{PHZ}	Output Disable Time	2.7	50	R_L = 1 KΩ			16.8	1.0	18.9	ns
		3.3(*)	50			8.6	12.0	1.0	13.5	
t_{OSLH} t_{OSHL}	Output to Output Skew Time (note 1, 2)	2.7	50				1.5		1.5	ns
		3.3(*)	50				1.5		1.5	

1) Skew is defined as the absolute value of the difference between the actual propagation delay for any two outputs of the same device switching in the same direction, either HIGH or LOW

2) Parameter guaranteed by design

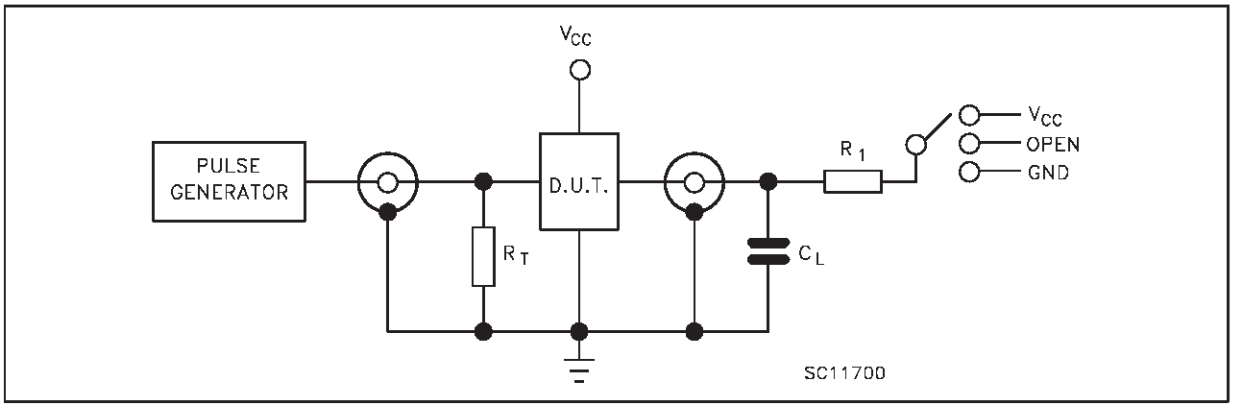
(*) Voltage range is 3.3V ± 0.3V

CAPACITIVE CHARACTERISTICS

Symbol	Parameter	Test Conditions	Value					Unit
			T_A = 25 °C			-40 to 85 °C		
			Min.	Typ.	Max.	Min.	Max.	
C_{IN}	Input Capacitance			4	10		10	pF
C_{OUT}	Output Capacitance			6				pF
C_{PD}	Power Dissipation Capacitance (note 1)			23				pF

1) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operating current can be obtained by the following equation. $I_{CC}(opr) = C_{PD} \bullet V_{CC} \bullet f_{IN} + I_{CC}/4$ (per Channel)

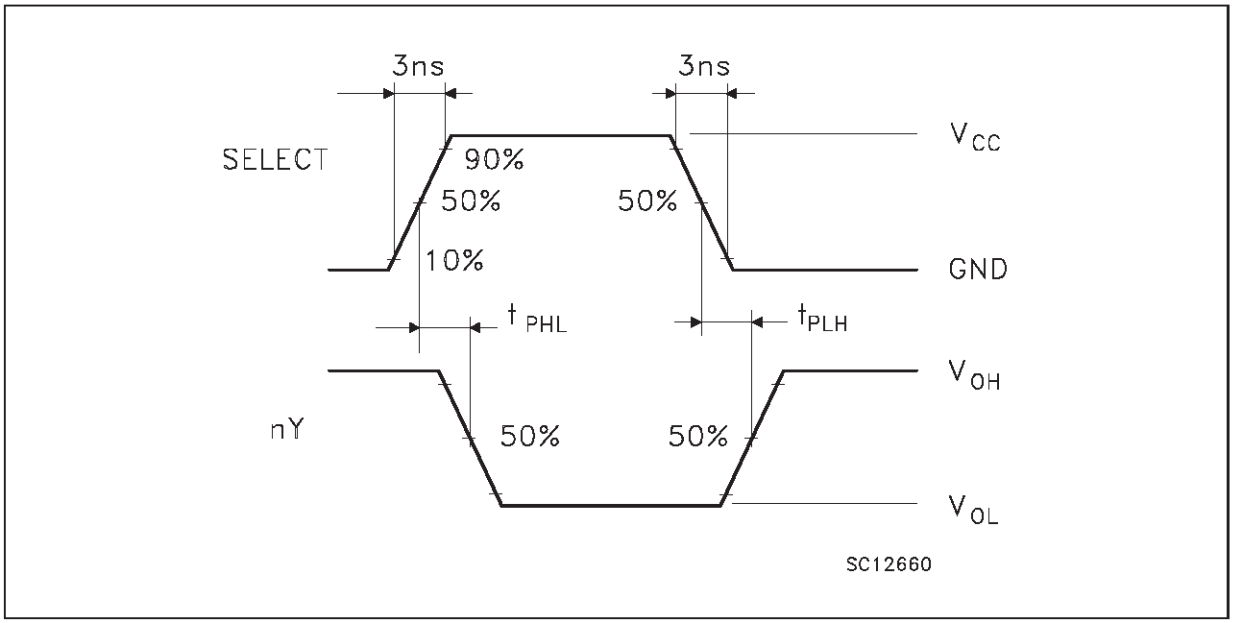
TEST CIRCUIT



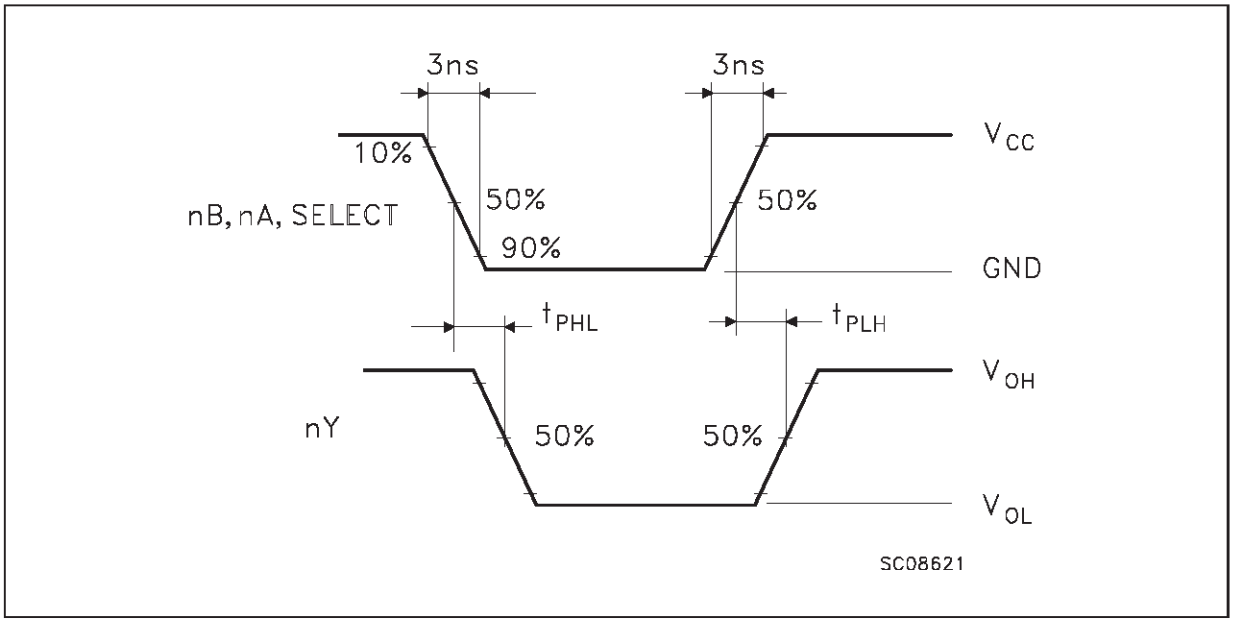
TEST	SWITCH
t_{PLH}, t_{PHL}	Open
t_{PZL}, t_{PLZ}	V_{CC}
t_{PZH}, t_{PHZ}	GND

C_L = 15/50 pF or equivalent (includes jig and probe capacitance)
$R_L = R_1$ = 1KΩ or equivalent
$R_T = Z_{OUT}$ of pulse generator (typically 50Ω)

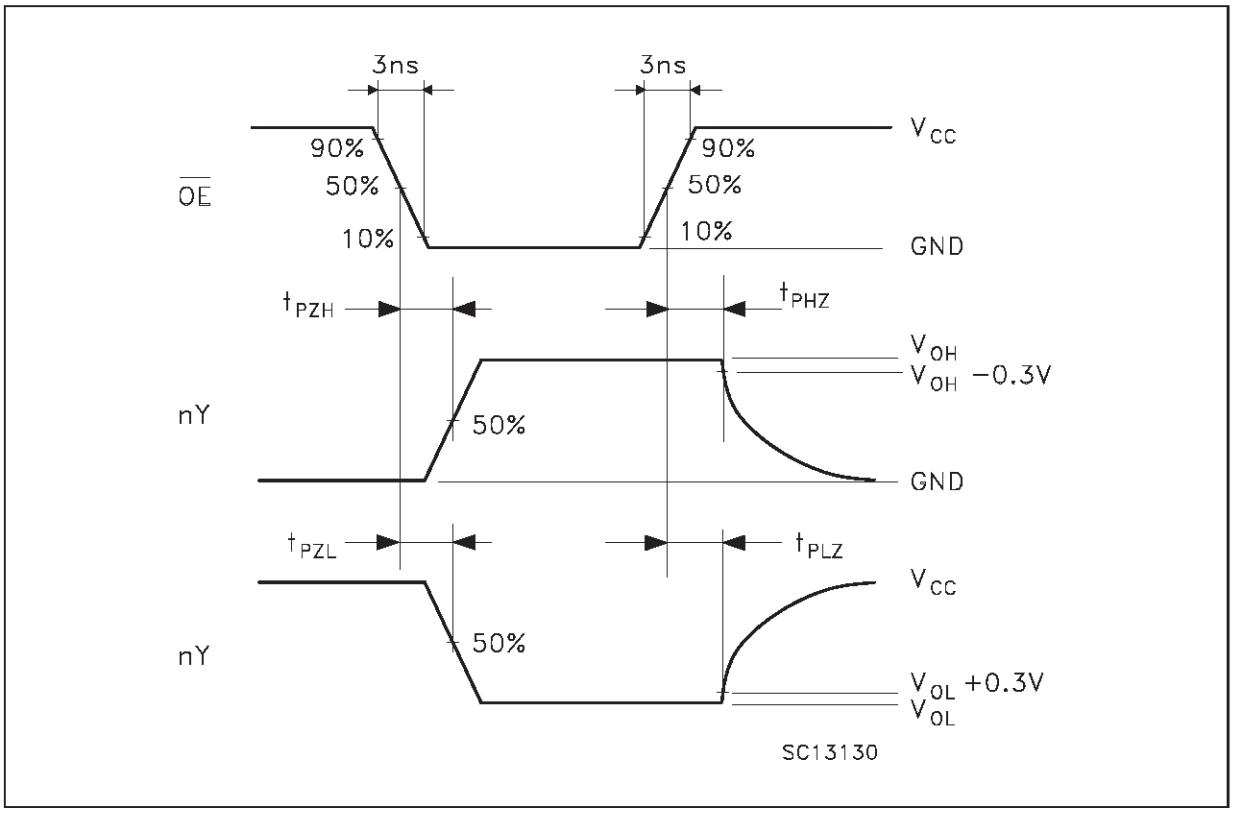
WAVEFORM 1: PROPAGATION DELAYS FOR INVERTING CONDITIONS (f=1MHz; 50% duty cycle)



WAVEFORM 2: PROPAGATION DELAYS FOR NON-INVERTING CONDITIONS (f=1MHz; 50% duty cycle)

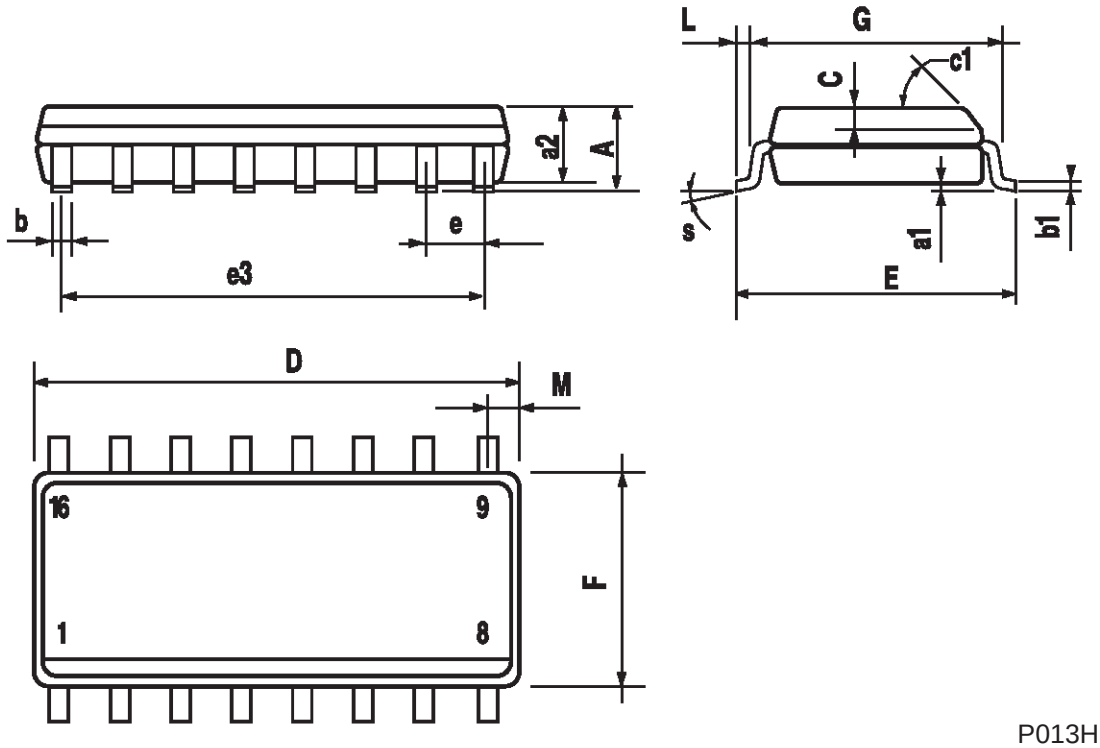


WAVEFORM 3: OUTPUT ENABLE AND DISABLE TIME (f=1MHz; 50% duty cycle)



SO-16 MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.75			0.068
a1	0.1		0.2	0.004		0.007
a2			1.65			0.064
b	0.35		0.46	0.013		0.018
b1	0.19		0.25	0.007		0.010
C		0.5			0.019	
c1	45 (typ.)					
D	9.8		10	0.385		0.393
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		8.89			0.350	
F	3.8		4.0	0.149		0.157
G	4.6		5.3	0.181		0.208
L	0.5		1.27	0.019		0.050
M			0.62			0.024
S	8 (max.)					



P013H

TSSOP16 MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.1			0.433
A1	0.05	0.10	0.15	0.002	0.004	0.006
A2	0.85	0.9	0.95	0.335	0.354	0.374
b	0.19		0.30	0.0075		0.0118
c	0.09		0.20	0.0035		0.0079
D	4.9	5	5.1	0.193	0.197	0.201
E	6.25	6.4	6.5	0.246	0.252	0.256
E1	4.3	4.4	4.48	0.169	0.173	0.176
e		0.65 BSC			0.0256 BSC	
K	0^o	4^o	8^o	0^o	4^o	8^o
L	0.50	0.60	0.70	0.020	0.024	0.028