National Semiconductor

74F113
Dual JK Negative Edge-Triggered Flip-Flop

General Description

The 'F113 offers individual J, K, Set and Clock inputs. When the clock goes HIGH the inputs are enabled and data may be entered. The logic level of the J and K inputs may be changed when the clock pulse is HIGH and the flip-flop will perform according to the Truth Table as long as minimum setup and hold times are observed. Input data is transferred to the outputs on the falling edge of the clock pulse.

Asynchronous input:
LOW input to $\overline{S}_D$ sets Q to HIGH level
Set is independent of clock

Features

- Guaranteed 4000V minimum ESD protection

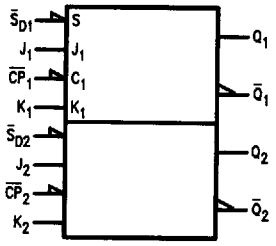
Ordering Code: See Section 11

Commercial	Package Number	Package Description
74F113PC	N14A	14-Lead (0.300" Wide) Molded Dual-In-Line
74F113SC (Note 1)	M14A	14-Lead (0.150" Wide) Molded Small Outline, JEDEC
74F113SJ (Note 1)	M14D	14-Lead (0.300" Wide) Molded Small Outline, EIAJ

Note 1: Devices also available in 13" reel. Use suffix = SCX and SJX.

Logic Symbols

IEEE/IEC



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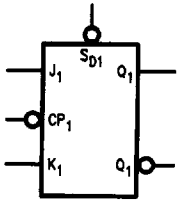

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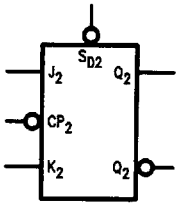

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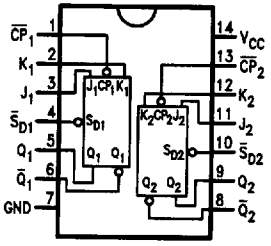
Connection Diagram

Pin Assignment for SOIC and DIP



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Unit Loading/Fan Out: See Section 2 for U.L. Definitions

Pin Names	Description	74F	
		U.L. HIGH/LOW	Input I_{IH}/I_{IL} Output I_{OH}/I_{OL}
J_1, J_2, K_1, K_2	Data Inputs	1.0/1.0	20 μA/−0.6 mA
$\overline{CP}_1, \overline{CP}_2$	Clock Pulse Inputs (Acitve Falling Edge)	1.0/4.0	20 μA/−2.4 mA
$\overline{S}_{D1}, \overline{S}_{D2}$	Direct Set Inputs (Active LOW)	1.0/5.0	20 μA/−3.0 mA
$Q_1, Q_2, \overline{Q}_1, \overline{Q}_2$	Outputs	50/33.3	−1 mA/20 mA

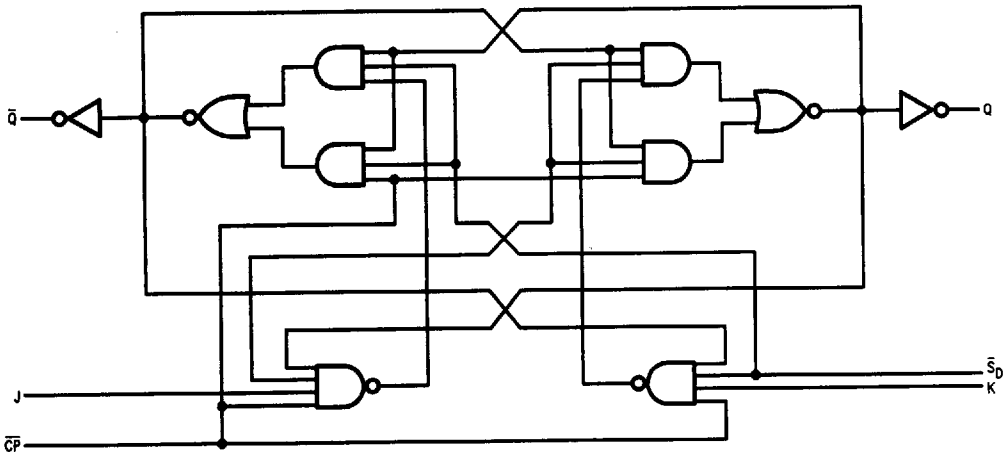
Truth Table

Inputs				Outputs	
$\overline{S}_D$	$\overline{CP}$	J	K	Q	$\overline{Q}$
L	X	X	X	H	L
H	⌐	h	h	$\overline{Q}_0$	Q_0
H	⌐	l	h	L	H
H	⌐	h	l	H	L
H	⌐	l	l	Q_0	$\overline{Q}_0$

H(h) = HIGH Voltage Level
L(l) = LOW Voltage level
⌐ = HIGH-to-LOW Clock Transition
X = Immaterial
Q_0 ($\overline{Q}_0$) = Before HIGH-to-LOW Transition of Clock

Lower case letters indicate the state of the referenced input or output prior to the HIGH-to-LOW clock transition.

Logic Diagram (One Half Shown)



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Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	−55°C to +175°C
Plastic	−55°C to +150°C
V_{CC} Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 2)	−0.5V to +7.0V
Input Current (Note 2)	−30 mA to +5.0 mA
Voltage Applied to Output in HIGH State (with V_{CC} = 0V)	
Standard Output	−0.5V to V_{CC}
TRI-STATE® Output	−0.5V to +5.5V
Current Applied to Output in LOW State (Max)	twice the rated I_{OL} (mA)

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

Recommended Operating Conditions

Free Air Ambient Temperature	
Commercial	0°C to +70°C
Supply Voltage	
Commercial	+4.5V to +5.5V

DC Electrical Characteristics

Symbol	Parameter		74F Min	74F Typ	74F Max	Units	V_{CC}	Conditions
V_{IH}	Input HIGH Voltage		2.0			V		Recognized as a HIGH Signal
V_{IL}	Input LOW Voltage				0.8	V		Recognized as a LOW Signal
V_{CD}	Input Clamp Diode Voltage				−1.2	V	Min	I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	74F 10% V_{CC}	2.5			V	Min	I_{OH} = −1 mA
		74F 5% V_{CC}	2.7					I_{OH} = −1 mA
V_{OL}	Output LOW Voltage	74F 10% V_{CC}			0.5	V	Min	I_{OL} = 20 mA
I_{IH}	Input HIGH Current	74F			5.0	μA	Max	V_{IN} = 2.7V
I_{BVI}	Input HIGH Current Breakdown Test	74F			7.0	μA	Max	V_{IN} = 7.0V
I_{CEX}	Output HIGH Leakage Current	74F			50	μA	Max	V_{OUT} = V_{CC}
V_{ID}	Input Leakage Test	74F	4.75			V	0.0	I_{ID} = 1.9 μA All Other Pins Grounded
I_{OD}	Output Leakage Circuit Current	74F			3.75	μA	0.0	V_{IOD} = 150 mV All Other Pins Grounded
I_{IL}	Input LOW Current				−0.6 −2.4 −3.0	mA	Max	V_{IN} = 0.5V (J_n, K_n) V_{IN} = 0.5V ($\overline{CP}_n$) V_{IN} = 0.5V ($\overline{S}_{Dn}$)
I_{OZH}	Output Leakage Current				50	μA	Max	V_{OUT} = 2.7V
I_{OZL}	Output Leakage Current				−50	μA	Max	V_{OUT} = 0.5V
I_{OS}	Output Short-Circuit Current		−60		−150	mA	Max	V_{OUT} = 0V
I_{CC}	Power Supply Current			12	19	mA	Max	

AC Electrical Characteristics: See Section 2 for Waveforms and Load Configurations

Symbol	Parameter	74F $T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50\ pF$			74F $T_A, V_{CC} = Com$ $C_L = 50\ pF$		Units	Fig. No.
		Min	Typ	Max	Min	Max		
f_{max}	Maximum Clock Frequency	85	105		80		MHz	2-1
t_{PLH} t_{PHL}	Propagation Delay $\overline{CP}_n$ to Q_n or $\overline{Q}_n$	2.0 2.0	4.0 4.0	6.0 6.0	2.0 2.0	7.0 7.0	ns	2-3
t_{PLH} t_{PHL}	Propagation Delay $\overline{S}_{Dn}$ to Q_n or $\overline{Q}_n$	2.0 2.0	4.5 4.5	6.5 6.5	2.0 2.0	7.5 7.5	ns	2-3

AC Operating Requirements: See Section 2 for Waveforms

Symbol	Parameter	74F $T_A = +25°C$ $V_{CC} = +5.0V$		74F $T_A, V_{CC} = Com$		Units	Fig. No.
		Min	Max	Min	Max		
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW J_n or K_n to $\overline{CP}_n$	4.0 3.0		5.0 3.5		ns	2-6
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW J_n or K_n to $\overline{CP}_n$	0 0		0 0			
$t_w(H)$ $t_w(L)$	$\overline{CP}_n$ Pulse Width HIGH or LOW	4.5 4.5		5.0 5.0		ns	2-4
$t_w(L)$	$\overline{S}_{Dn}$ Pulse Width, LOW	4.5		5.0		ns	2-4
t_{rec}	$\overline{S}_{Dn}$ to $\overline{CP}_n$ Recovery Time	4.0		5.0		ns	2-6