R&E INTERNATIONAL, INC.

CMOS STROBED HEX INVERTER/BUFFER

FEATURES

- 3-State Outputs with Separate Disable Control
- Common Input Inhibit Line
- TTL Output Drive Guaranteed Over Temperature Range
- Output Impedance < 200 Ω @ 5Vdc Guaranteed Over Temperature Range

DESCRIPTION

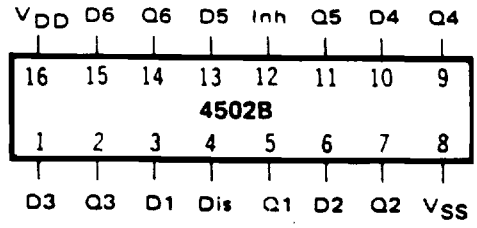
The 4502B is a Strobed Hex Inverter/Buffer with a common Data Input Inhibit Control and a common Output Disable Control. The 3-state output allows common bus configurations.

TRUTH TABLE

D_n	Inhibit	Disable	Q_n
0	0	0	1
1	0	0	0
X	1	0	0
X	X	1	High Impedance

X = Don't Care

CONNECTION DIAGRAM
(all packages)

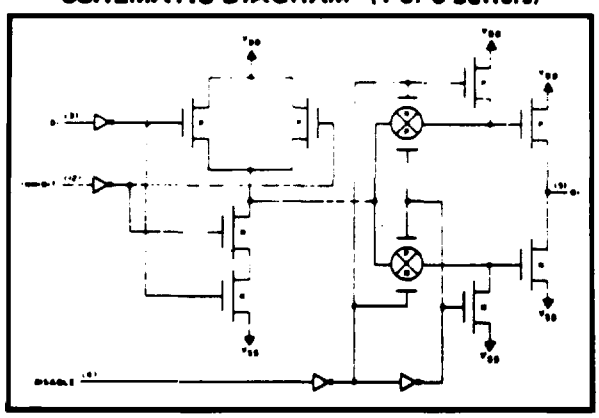


RECOMMENDED OPERATING CONDITIONS

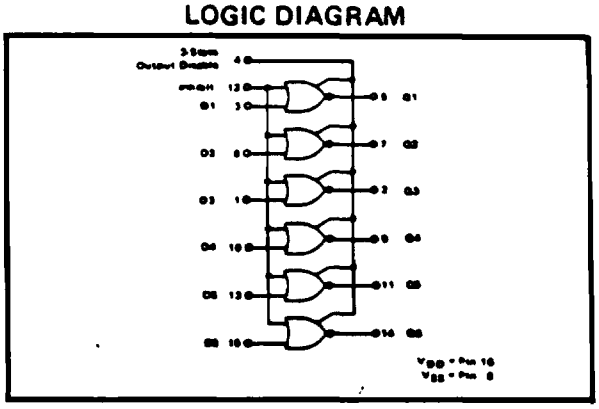
For maximum reliability:

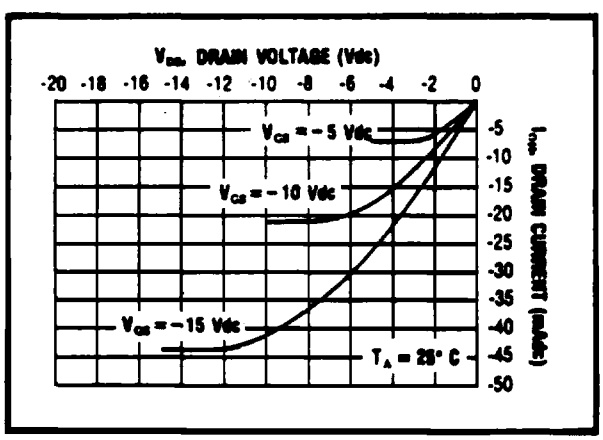
DC Supply Voltage	$V_{DD} - V_{SS}$	3 to 15	Vdc
Operating Temperature	T_A		
C		-55 to +125	°C
E		-40 to +85	°C

SCHEMATIC DIAGRAM (1 of 6 buffers)

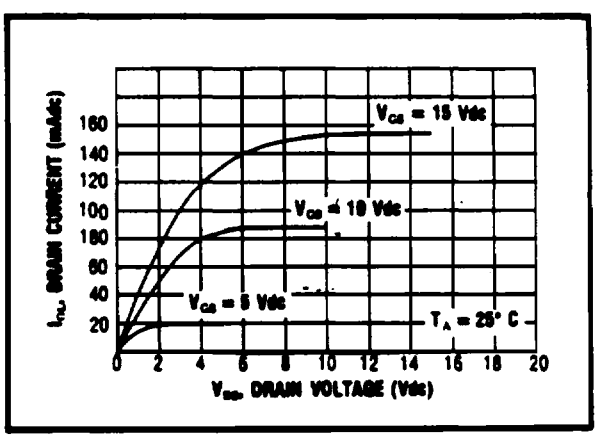


LOGIC DIAGRAM





Typical P-Channel
Source Current Characteristics



Typical N-Channel
Sink Current Characteristics

ELECTRICAL CHARACTERISTICS

STATIC CHARACTERISTICS [1]

PARAMETER		V_{DD} (Vdc)	CONDITIONS	T_{LOW} [2]		+25°C			T_{HIGH} [2]		Units
				Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
QUIESCENT DEVICE CURRENT	I_{DD}	5	$V_{IN} = V_{SS}$ or V_{DD}	–	1.0	–	0.005	1.0	–	30	μAdc
		10	All valid input	–	2.0	–	0.01	2.0	–	60	
		15	combinations	–	4.0	–	0.02	4.0	–	120	
OUTPUT LOW (SINK) CURRENT	I_{OL}	5	$V_{OL} = 0.4V$	3.5	–	2.8	5.7	–	2.0	–	mAdc
		10	$V_{OL} = 0.5V$	7.8	–	6.3	12.5	–	4.4	–	
		15	$V_{OL} = 1.5V$	29	–	24.0	49	–	16	–	
			$V_{IN} = V_{SS}$ or V_{DD}								
3-STATE OUTPUT LEAKAGE CURRENT	I_{ZL}	15		–	±0.1	–	$\pm 10^{-4}$	±0.1	–	±1.0	μAdc

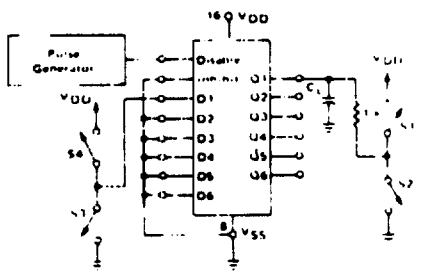
NOTES: [1] Remaining Static Electrical Characteristics are listed under "40008 Series Family Specifications".
[2] T_{LOW} = -55°C for C
= -40°C for E
T_{HIGH} = +125°C for C
= + 85°C for E

DYNAMIC CHARACTERISTICS (C_L = 50pF, T_A = 25°C)

PARAMETER		V_{DD} (Vdc)	Min.	Typ.	Max.	Units
PROPAGATION DELAY TIME From Data Inputs	t_{PLH}	5	–	125	250	ns
		10	–	60	120	
		15	–	45	90	
	t_{PHL}	5	–	100	200	ns
		10	–	50	100	
		15	–	40	80	
From Disable	t_{PHZ}, t_{PLZ} t_{PZH}, t_{PZL}	5	–	65	130	ns
		10	–	30	60	
		15	–	25	50	
OUTPUT TRANSITION TIME	t_{TLH}	5	–	100	200	ns
		10	–	50	100	
		15	–	40	80	
	t_{THL}	5	–	60	120	ns
		10	–	30	60	
		15	–	20	40	

Switch Positions for 3 State Test

Test	S1	S2	S3	S4
t_{PHZ}	Open	Closed	Closed	Open
t_{PLZ}	Closed	Open	Open	Closed
t_{PZL}	Closed	Open	Open	Closed
t_{PZH}	Open	Closed	Closed	Open



3-State AC Test Circuit and Waveforms (t_{PHZ}, t_{PZH}, t_{PLZ}, t_{PZL})