P54/74FCT827AT/BT/CT
P54/74FCT828AT/BT/CT
BUFFERS

FEATURES

- **Function, Pinout and Drive Compatible with the FCT, F and AM29827/828 Logic**
- **FCT-C speed at 4.4ns max. (Com'l) FCT-A speed at 5.0ns max. (Com'l)**
- **Reduced V_{OH} (typically = 3.3V) versions of Equivalent FCT functions**
- **Edge-rate Control Circuitry for Significantly Improved Noise Characteristics**
- **ESD protection exceeds 2000V**
- **Power-off disable feature**
- **Matched Rise and Fall times**
- **Fully Compatible with TTL Input and Output Logic Levels**
- **64 mA Sink Current (Com'l), 32 mA (Mil) 15 mA Source Current (Com'l), 12 mA (Mil)**
- **Manufactured in 0.7 micron PACE Technology™**

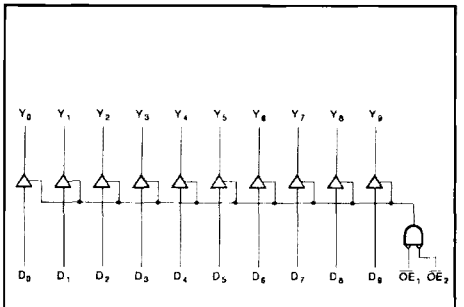
DESCRIPTION

The 'FCT827T and 'FCT828T 10-bit bus drivers provide high-performance bus interface buffering for wide data/address paths or buses carrying parity. The 10-bit buffers have NOR-ed output enables for maximum control flexibility. The 'FCT827T and 'FCT828T family of devices are designed for high-capacitance load drive capability, while providing low-capacitance bus loading at both inputs and outputs. All inputs have clamp diodes and all outputs are designed for' low-capacitance bus loading in the high impedance state. The 'FCT827T is non-inverting and the 'FCT828T is inverting.

The 'FCT827T and 'FCT828T is manufacturered using PACE Technology™ which is Performance Advanced CMOS Engineered to use 0.7 micron effective channel lengths giving 400 picoseconds loaded* internal gate delays. PACE Technology includes two-level metal and epitaxial substrates. In addition to very high performance and very high density, the technology features latch-up protection, single event upset protection, and is supported by a Class 1 environment volume production facility.

*For a fan-in/fan-out of 4, at 85°C junction temperature and 5.0V supply. For a fan-in/fan-out of 1, the internal gate delay is 200 picoseconds at room temperature and 5.0V

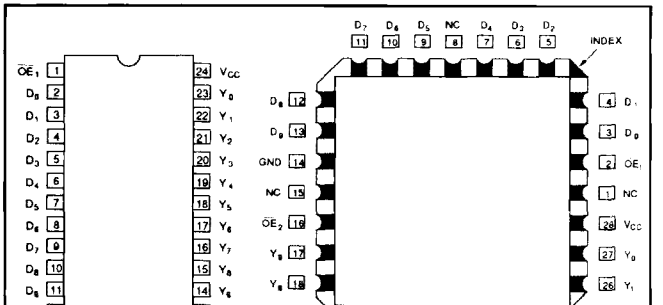
LOGIC BLOCK DIAGRAM



'FCT827T

1724 01

PIN CONFIGURATIONS



DIP (D4,P4)
SOIC (S4)

LCC (L5-1)

1724 02

ABSOLUTE MAXIMUM RATINGS[1,2]

Symbol	Parameter	Value	Unit
T_{STG}	Storage Temperature	–65 to +150	°C
T_A	Ambient Temperature Under Bias	–65 to +135	°C
V_{CC}	V_{CC} Potential to Ground	–0.5 to +7.0	V
P_T	Power Dissipation	0.5	W

1724 Tbl 01

Symbol	Parameter	Value	Unit
I_{OUTPUT}	Current Applied to Output	120	mA
V_{IN}	Input Voltage	–0.5 to +7.0	V
V_{OUT}	Voltage Applied to Output	–0.5 to +7.0	V

1724 Tbl 02

Notes:

1. Operation beyond the limits set forth in the above table may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.
2. Unused inputs must always be connected to an appropriate logic voltage level, preferably either V_{CC} or ground.

RECOMMENDED OPERATING CONDITIONS

Free Air Ambient Temperature	Min	Max
Military	–55°C	+125°C
Commercial	0°C	+70°C

1724 Tbl 03

Supply Voltage (V_{CC})	Min	Max
Military	+4.5V	+5.5V
Commercial	+4.75V	+5.25V

1724 Tbl 04

DC ELECTRICAL CHARACTERISTICS (Over recommended operating conditions)

Symbol	Parameter		Min	Typ[1]	Max	Units	V_{CC}	Conditions
V_{IH}	Input HIGH Voltage		2.0			V		
V_{IL}	Input LOW Voltage				0.8	V		
V_H	Hysteresis			0.2		V		All inputs
V_{IK}	Input Clamp Diode Voltage			–0.7	–1.2	V	MIN	I_{IN} = –18mA
V_{OH}	Output HIGH Voltage	Military	2.4	3.3		V	MIN	I_{OH} = –12mA
		Commercial	2.4	3.3		V	MIN	I_{OH} = –15mA
V_{OL}	Output LOW Voltage	Military		0.3	0.5	V	MIN	I_{OL} = 32mA
		Commercial		0.3	0.5	V	MIN	I_{OL} = 48mA
		Commercial		0.3	0.5	V	MIN	I_{OL} = 64mA
I_I	Input HIGH Current				20	µA	MAX	$V_{IN} = V_{CC}$
I_{IH}	Input HIGH Current				5	µA	MAX	V_{IN} = 2.7V
I_{IL}	Input LOW Current				–5	µA	MAX	V_{IN} = 0.5V
I_{OZH}	Off State I_{OUT} HIGH-Level Output Current				10	µA	MAX	V_{OUT} = 2.7V
I_{OZL}	Off State I_{OUT} LOW-Level Output Current				–10	µA	MAX	V_{OUT} = 0.5V
I_{OS}	Output Short Circuit Current[2]		–60	–120	–225	mA	MAX	V_{OUT} = 0.0V
I_{OFF}	Power-off Disable				100	µA	0V	V_{OUT} = 4.5V
C_{IN}	Input Capacitance[3]			6	10	pF	MAX	All inputs
C_{OUT}	Output Capacitance[3]			8	12	pF	MAX	All outputs
I_{CC}	Quiescent Power Supply Current			0.2	1.5	mA	MAX	$V_{IN} \leq 0.2V$, $V_{IN} \geq V_{CC}-0.2V$

1724 Tbl 05

Notes:

1. Typical limits are at V_{CC} = 5.0V, T_A = +25°C ambient.
2. Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high speed test apparatus and/or sample and hold techniques are preferable in order to minimize internal chip heating and more accurately reflect operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{os} tests should be performed last.
3. This parameter is guaranteed but not tested.

DC CHARACTERISTICS (Over recommended operating conditions unless otherwise specified.)

Symbol	Parameter	Typ[1]	Max	Units	Conditions
ΔI_{CC}	Quiescent Power Supply Current (TTL inputs)	0.5	2.0	mA	V_{CC} = MAX, V_{IN} = 3.4V[2], f_1 = 0, Outputs Open
I_{CCD}	Dynamic Power Supply Current[3]	0.15	0.25	mA/ mHz	V_{CC} = MAX, One Input Toggling, 50% Duty Cycle, Outputs Open, $\overline{OE}_1$ = $\overline{OE}_2$ = GND, $V_{IN} \le 0.2V$ or $V_{IN} \ge V_{CC} - 0.2V$
I_C	Total Power Supply Current[5]	1.7	4.0	mA	V_{CC} = MAX, 50% Duty Cycle, Outputs Open, One Bit Toggling at f_1 = 10MHz, $\overline{OE}_1$ = $\overline{OE}_2$ = GND, $V_{IN} \le 0.2V$ or $V_{IN} \ge V_{CC} - 0.2V$
		2.0	5.0	mA	V_{CC} = MAX, 50% Duty Cycle, Outputs Open, One Bit Toggling at f_1 = 10MHz, $\overline{OE}_1$ = $\overline{OE}_2$ = GND, V_{IN} = 3.4V or V_{IN} = GND
		3.2	6.5[4]	mA	V_{CC} = MAX, 50% Duty Cycle, Outputs Open, Eight Bits Toggling at f_1 = 2.5MHz, $\overline{OE}_1$ = $\overline{OE}_2$ = GND, $V_{IN} \le 0.2V$ or $V_{IN} \ge V_{CC} - 0.2V$
		5.2	14.5[4]	mA	V_{CC} = MAX, 50% Duty Cycle, Outputs Open, Eight Bits Toggling at f_1 = 2.5MHz, $\overline{OE}_1$ = $\overline{OE}_2$ = GND, V_{IN} = 3.4V or V_{IN} = GND

1724 Tbl 06

Notes:

1. Typical values are at V_{CC} = 5.0V, +25°C ambient.
2. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
3. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
4. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
5. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD}(f_0/2 + f_1 N_1)$
   I_{CC} = Quiescent Current with CMOS input levels
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_0 = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_1 = Input Frequency
   N_1 = Number of Inputs at f_1
   All currents are in milliamps and all frequencies are in megahertz.

FUNCTION TABLES

'FCT827T (Non-Inverting)

Inputs			Outputs	Function
$\overline{OE}_1$	$\overline{OE}_2$	D_i	Y_i	
L	L	L	L	Transparent
L	L	H	H	
H	X	X	Z	Three-State
X	H	X	Z	

1724 Tbl 07

Note:
H = High, L = Low, X = Don't Care, Z = High Impedance

'FCT828T (Inverting)

Inputs			Outputs	Function
$\overline{OE}_1$	$\overline{OE}_2$	D_i	Y_i	
L	L	L	H	Transparent
L	L	H	L	
H	X	X	Z	Three-State
X	H	X	Z	

1724 Tbl 08

Note:
H = High, L = Low, X = Don't Care, Z = High Impedance

7

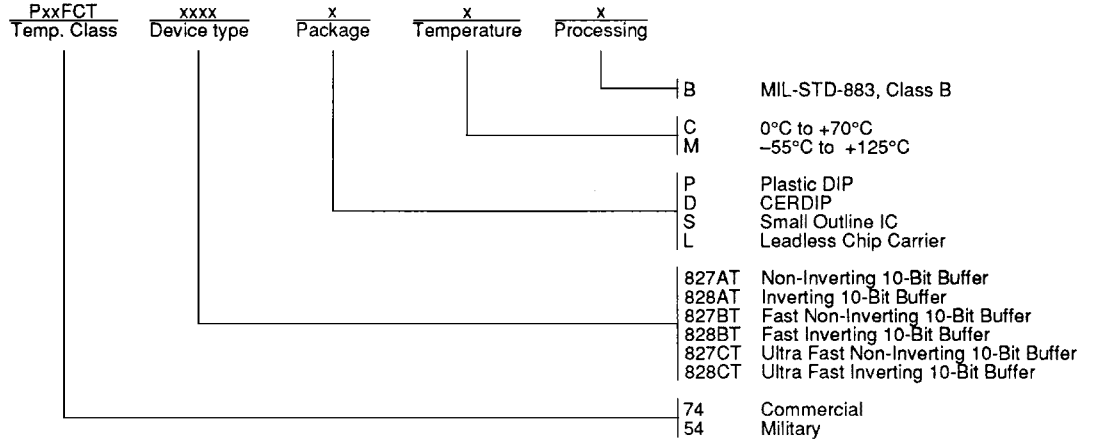
AC CHARACTERISTICS

Sym.	Parameter	Test Conditions	'FCT827AT/828AT				'FCT827BT/828BT				'FCT827CT/828CT				Units	Fig. No.
			MIL		COM'L		MIL		COM'L		MIL		COM'L			
			Min.[1]	Max.	Min.[1]	Max.	Min.[1]	Max.	Min.[1]	Max.	Min.[1]	Max.	Min.[1]	Max		
t_{PLH} t_{PHL}	Propagation Delay from D_1 to Y_1 'FCT827T	C_L = 50pF R_L = 500Ω	–	9.0	–	8.0	–	6.5	–	5.0	–	5.0	–	4.4	ns	1,3
t_{PLH} t_{PHL}	Propagation Delay from D_1 to Y_1 'FCT827T	C_L = 300pF[2] R_L = 500Ω	–	17.0	–	15.0	–	14.0	–	13.0	–	11.0	–	10.0	ns	1,3
t_{PLH} t_{PHL}	Propagation Delay from D_1 to Y_1 'FCT828T	C_L = 50pF R_L = 500Ω	–	10.0	–	9.0	–	6.5	–	5.5	–	5.0	–	4.4	ns	1,2
t_{PLH} t_{PHL}	Propagation Delay from D_1 to Y_1 'FCT828T	C_L = 300pF[2] R_L = 500Ω	–	16.0	–	14.0	–	14.0	–	13.0	–	11.0	–	10.0	ns	1,2
t_{PZH} t_{PZL}	Output Enable Time $\overline{OE}$ to Y_1	C_L = 50pF R_L = 500Ω	–	13.0	–	12.0	–	9.0	–	8.0	–	8.0	–	7.0	ns	1,7,8
t_{PZH} t_{PZL}	Output Enable Time $\overline{OE}$ to Y_1	C_L = 300pF[2] R_L = 500Ω	–	25.0	–	23.0	–	16.0	–	15.0	–	15.0	–	14.0	ns	1,7,8
t_{PHZ} t_{PHL}	Output Disable Time $\overline{OE}$ to Y_1	C_L = 5pF[2] R_L = 500Ω	–	9.0	–	9.0	–	7.0	–	6.0	–	6.7	–	5.7	ns	1,7,8
t_{PHZ} t_{PHL}	Output Disable Time $\overline{OE}$ to Y_1	C_L = 50p R_L = 500Ω	–	10.0	–	10.0	–	8.0	–	7.0	–	7.0	–	6.0	ns	1,7,8

1724 Tbl 09

Notes:
1. Minimum limits are guaranteed but not tested on Propagation Delays.
2. These parameters are guaranteed but not tested.

ORDERING INFORMATION



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