

SN54F114, SN74F114 DUAL J-K NEGATIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET, COMMON CLEAR, AND COMMON CLOCK

D2932, MARCH 1987—REVISED JANUARY 1989

- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

description

These devices contain two independent J-K negative-edge-triggered flip-flops. A low level at the Preset or Clear inputs sets or resets the outputs regardless of the levels of the other inputs. When Preset and Clear are inactive (high), data at the J and K inputs meeting the setup time requirements are transferred to the outputs on the negative-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the fall time of the clock pulse. Following the hold time interval, data at the J and K inputs may be changed without affecting the levels at the outputs. These versatile flip-flops can perform as toggle flip-flops by tying J and K high.

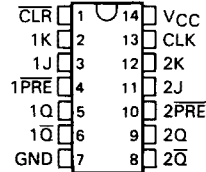
The SN54F114 is characterized for operation over the full military temperature range of -55°C to 125°C. The SN74F114 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE

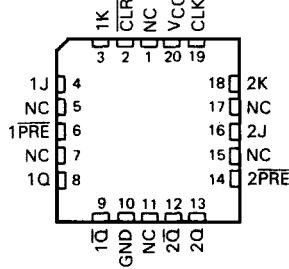
INPUTS			OUTPUTS			
PRE	CLR	CLK	J	K	Q	\bar{Q}
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H [†]	H [†]
H	H	↓	L	L	Q ₀	\bar{Q}_0
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	TOGGLE	TOGGLE
H	H	H	X	X	Q ₀	\bar{Q}_0

[†]The output levels in this configuration are not guaranteed to meet the minimum levels for V_{OH}. Furthermore, this configuration is nonstable; that is, it will not persist when either Preset or Clear returns to its inactive (high) level.

SN54F114 . . . J PACKAGE
SN74F114 . . . D OR N PACKAGE
(TOP VIEW)

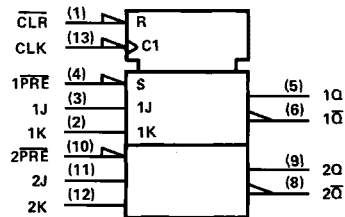


SN54F114 . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

logic symbol[†]



[†]This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for D, J, and N packages.

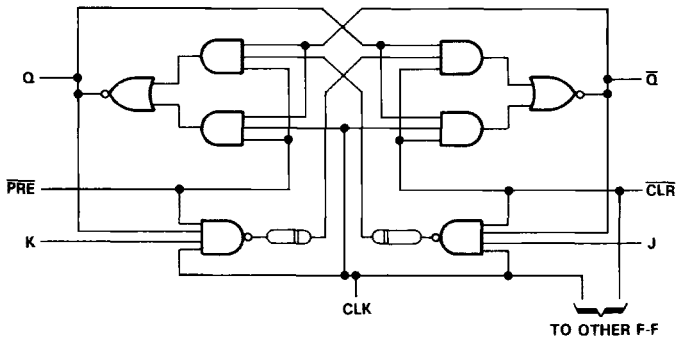
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Data Sheets

UNLESS OTHERWISE NOTED this document contains PRODUCTION DATA information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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WITH PRESET, COMMON CLEAR, AND COMMON CLOCK

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC}	-0.5 V to 7 V
Input voltage [†]	-1.2 V to 7 V
Input current	-30 mA to 5 mA
Voltage applied to any output in the high state	-0.5 V to V_{CC}
Current into any output in the low state	40 mA
Operating free-air temperature range: SN54F114	-55 °C to 125 °C
SN74F114	0 °C to 70 °C
Storage temperature range	-65 °C to 150 °C

[†]The input voltage ratings may be exceeded provided the input current ratings are observed.

recommended operating conditions

	SN54F114			SN74F114			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC} Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH} High-level input voltage	2			2			V
V_{IL} Low-level input voltage			0.8			0.8	V
I_{IK} Input clamp current			-18			-18	mA
I_{OH} High-level output current			-1			-1	mA
I_{OL} Low-level output current			20			20	mA
T_A Operating free-air temperature	-55		125	0		70	°C

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	SN54F114		SN74F114		UNIT		
		MIN	TYP [†]	MAX	MIN		TYP [†]	MAX
V _{IJK}	V _{CC} = 4.5 V, I _I = -18 mA			-1.2		-1.2	V	
V _{OH}	V _{CC} = 4.5 V, I _{OH} = -1 mA	2.5	3.4		2.5	3.4	V	
	V _{CC} = 4.75 V, I _{OH} = -1 mA				2.7			
V _{OL}	V _{CC} = 4.5 V, I _{OL} = 20 mA		0.3	0.5		0.3	0.5	V
I _I	V _{CC} = 5.5 V, V _I = 7 V			0.1		0.1	mA	
I _{IH}	V _{CC} = 5.5 V, V _I = 2.7 V			20		20	μA	
I _{IL}	V _{CC} = 5.5 V, V _I = 0.5 V	J or K		-0.6		-0.6	mA	
		PRE or CLR		-3		-3		
		CLK		-2.4		-2.4		
I _{OS} [‡]	V _{CC} = 5.5 V, V _O = 0	-60		-150	-60		-150	mA
I _{CC}	V _{CC} = 5.5 V, See Note 1		12	19		12	19	mA

timing requirements

		V _{CC} = 5 V, T _A = 25°C		V _{CC} = 4.5 V to 5.5 V, T _A = MIN to MAX [§]				UNIT
		'F114		SN54F114		SN74F114		
		MIN	MAX	MIN	MAX	MIN	MAX	
f _{clock}	Clock frequency	0	100			0	90	MHz
t _{su}	Setup time before CLK↓	Data high	4			5		ns
		Data low	3			3.5		
t _h	Hold time after CLK↓	Data high	0			0		ns
		or low						
t _w	Pulse duration	CLK high or low	4.5			5		ns
t _w	Pulse duration	PRE or CLR low	4.5			5		ns
t _{rec}	Recovery time	PRE or CLR to CLK	4			5		ns

switching characteristics (see Note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 5 V, C _L = 50 pF, R _L = 500 Ω, T _A = 25°C			V _{CC} = 4.5 V to 5.5 V, C _L = 50 pF, R _L = 500 Ω, T _A = MIN to MAX [§]				UNIT
			'F114			SN54F114		SN74F114		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _{max}			100	125			90		MHz	
t _{PLH}	CLK	Q or Q̄	2.2	4.6	6.5			2.2	7.5	ns
t _{PHL}			2.2	5.1	7.5			2.2	8.5	
t _{PLH}	PRE or CLR	Q or Q̄	2.2	4.1	6.5			2.2	7.5	ns
t _{PHL}			2.2	4.1	6.5			2.2	7.5	

[†] All typical values are at V_{CC} = 5 V, T_A = 25°C.

[‡] Not more than one output should be shorted at a time and the duration of the short circuit should not exceed one second.

[§] For conditions shown as MIN or MAX, use the appropriate value specified under Recommended Operating Conditions.

NOTES: 1. I_{CC} is measured with all outputs open, the Q and Q̄ outputs alternately at high level and at the time of measurement, the clock is grounded.

2. Load circuits and waveforms are shown in Section 1.

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Data Sheets

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Data Sheets