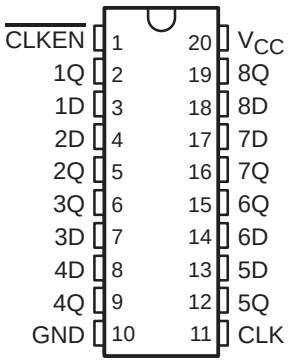
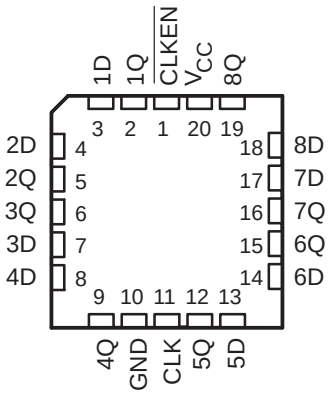
- **State-of-the-Art *EPIC*-II*B*™ BiCMOS Design Significantly Reduces Power Dissipation**
- **Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17**
- **Typical V_{OLP} (Output Ground Bounce) < 1 V at V_{CC} = 5 V, T_A = 25°C**
- **High-Drive Outputs (–32-mA I_{OH}, 64-mA I_{OL})**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages, Ceramic Chip Carriers (FK), Plastic (N) and Ceramic (J) DIPs, and Ceramic Flat (W) Package**

SN54ABT377 . . . J OR W PACKAGE
SN74ABT377A . . . DB, DW, N, OR PW PACKAGE
(TOP VIEW)



SN54ABT377 . . . FK PACKAGE
(TOP VIEW)



description

These 8-bit positive-edge-triggered D-type flip-flops with a clock (CLK) input are particularly suitable for implementing buffer and storage registers, shift registers, and pattern generators.

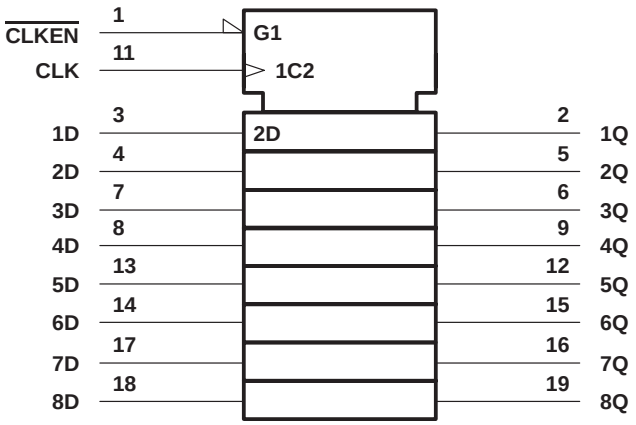
Data (D) input information that meets the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse if the common clock-enable ($\overline{CLKEN}$) input is low. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the buffered clock (CLK) input is at either the high or low level, the D-input signal has no effect at the output. The circuits are designed to prevent false clocking by transitions at $\overline{CLKEN}$.

The SN54ABT377 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74ABT377A is characterized for operation from –40°C to 85°C.

FUNCTION TABLE
(each flip-flop)

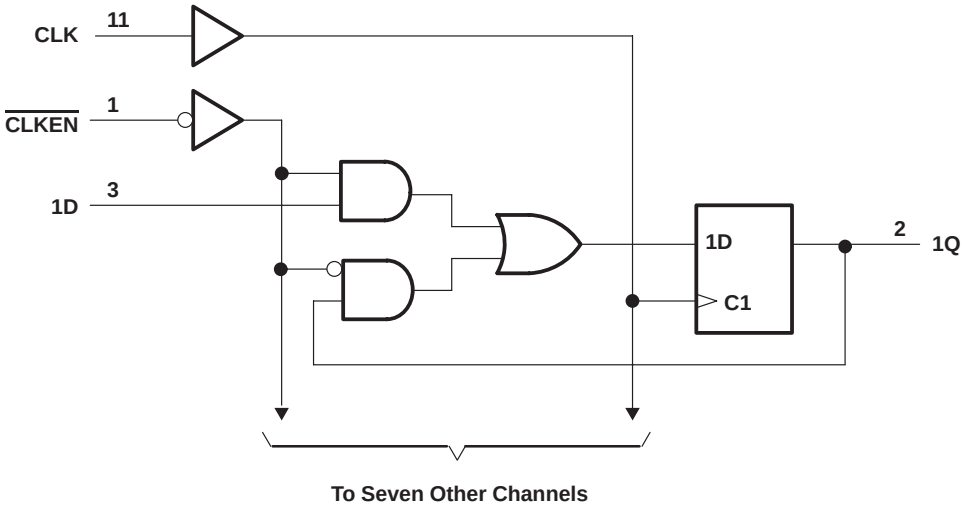
INPUTS			OUTPUT
$\overline{CLKEN}$	CLK	D	Q
H	X	X	Q_0
L	↑	H	H
L	↑	L	L
X	H or L	X	Q_0

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . –0.5 V to 7 V
Input voltage range, V_I (see Note 1) . . . . . –0.5 V to 7 V
Voltage range applied to any output in the high or power-off state, V_O . . . . . –0.5 V to 5.5 V
Current into any output in the low state, I_O: SN54ABT377 . . . . . 96 mA
SN74ABT377A . . . . . 128 mA
Input clamp current, I_{IK} (V_I < 0) . . . . . –18 mA
Output clamp current, I_{OK} (V_O < 0) . . . . . –50 mA
Package thermal impedance, θ_{JA} (see Note 2): DB package . . . . . 115°C/W
DW package . . . . . 97°C/W
N package . . . . . 67°C/W
PW package . . . . . 128°C/W
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The package thermal impedance is calculated in accordance with EIA/JEDEC Std JESD51, except for through-hole packages, which use a trace length of zero.

recommended operating conditions (see Note 3)

			SN54ABT377		SN74ABT377A		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I	Input voltage		0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current			–24		–32	mA
I_{OL}	Low-level output current			48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		5		5	ns/V
T_A	Operating free-air temperature		–55	125	–40	85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			T_A = 25°C			SN54ABT377		SN74ABT377A		UNIT
				MIN	TYP†	MAX	MIN	MAX	MIN	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = –18 mA				–1.2		–1.2		–1.2	V
V_{OH}	V_{CC} = 4.5 V,	I_{OH} = –3 mA		2.5			2.5		2.5		V
	V_{CC} = 5 V,	I_{OH} = –3 mA		3			3		3		
	V_{CC} = 4.5 V	I_{OH} = –24 mA		2			2				
		I_{OH} = –32 mA		2*					2		
V_{OL}	V_{CC} = 4.5 V	I_{OL} = 48 mA				0.55		0.55			V
		I_{OL} = 64 mA				0.55*				0.55	
V_{hys}					100						mV
I_I	V_{CC} = 5.5 V,	V_I = V_{CC} or GND				±1		±1		±1	µA
I_{off}	V_{CC} = 0,	V_I or V_O ≤ 4.5 V				±100				±100	µA
I_{CEX}	V_{CC} = 5.5 V,	V_O = 5.5 V	Outputs high			50		50		50	µA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.5 V		–50	–100	–180	–50	–180	–50	–180	mA
I_{CC}	V_{CC} = 5.5 V, I_O = 0, V_I = V_{CC} or GND		Outputs high		1	250		250		250	µA
			Outputs low		24	30		30		30	mA
ΔI_{CC}§	V_{CC} = 5.5 V, One input at 3.4 V, Other inputs at V_{CC} or GND					1.5		1.5		1.5	mA
C_i	V_I = 2.5 V or 0.5 V				3.5						pF

* On products compliant to MIL-PRF-38535, this parameter does not apply.
† All typical values are at V_{CC} = 5 V.
‡ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
§ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

			SN54ABT377				UNIT
			V_{CC} = 5 V, T_A = 25°C		MIN	MAX	
			MIN	MAX			
f_{clock}	Clock frequency		0	150	0	150	MHz
t_w	Pulse duration	CLK high or low	3.3		3.3		ns
t_{su}	Setup time before CLK↑	Data high or low	2		2.5		ns
		$\overline{\text{CLKEN}}$ high or low	3		3		
t_h	Hold time after CLK↑	Data high or low	1.8¶		1.8¶		ns
		$\overline{\text{CLKEN}}$ high or low	1.8¶		1.8¶		

¶ This data sheet limit may vary among suppliers.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

			SN74ABT377A				UNIT
			V_{CC} = 5 V, T_A = 25°C		MIN	MAX	
			MIN	MAX			
f_{clock}	Clock frequency		0	150	0	150	MHz
t_w	Pulse duration	CLK high or low	3.3		3.3		ns
t_{su}	Setup time before CLK↑	Data high or low	2		2.5		ns
		$\overline{\text{CLKEN}}$ high or low	3		3		
t_h	Hold time after CLK↑	Data high or low	1.8†		1.8†		ns
		$\overline{\text{CLKEN}}$ high or low	1.2†		1.2†		

† This data sheet limit may vary among suppliers.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figure 1)

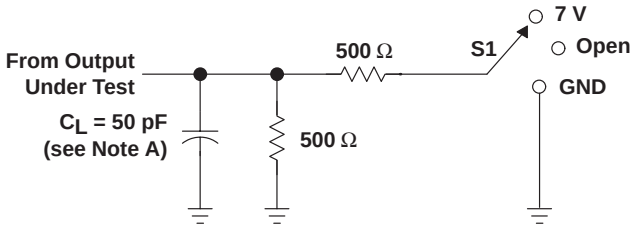
PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54ABT377					UNIT
			V_{CC} = 5 V, T_A = 25°C			MIN	MAX	
			MIN	TYP	MAX			
f_{max}			150			150		MHz
t_{PLH}	CLK	Q	2.2	4.5	6	2.2	7	ns
t_{PHL}			3.1	5.3	6.8	2	7.6	

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN74ABT377A					UNIT
			V_{CC} = 5 V, T_A = 25°C			MIN	MAX	
			MIN	TYP	MAX			
f_{max}			150			150		MHz
t_{PLH}	CLK	Q	2.2	4.5	6	2.2	6.5	ns
t_{PHL}			2.6†	5.3	6.8	2.6†	7.3	

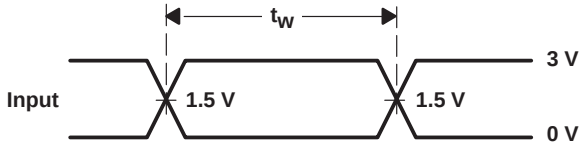
† This data sheet limit may vary among suppliers.

PARAMETER MEASUREMENT INFORMATION

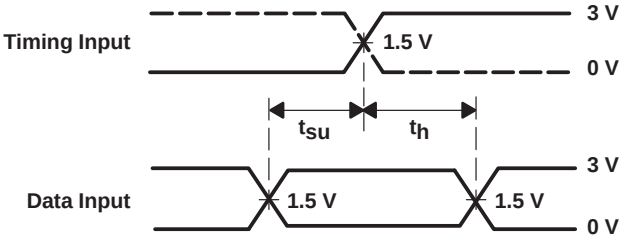


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open

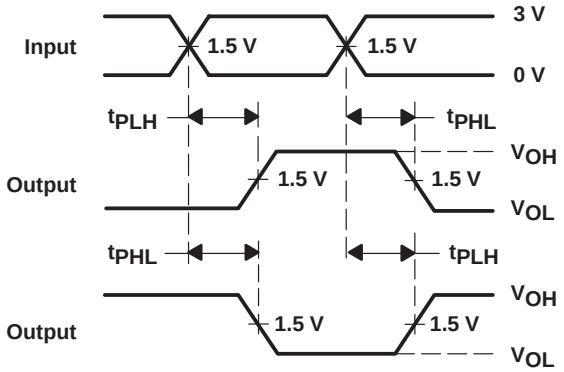
LOAD CIRCUIT



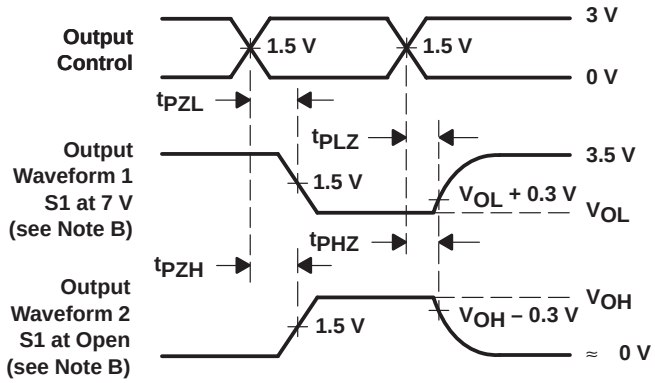
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

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PRODUCT FOLDER | PRODUCT INFO: FEATURES | DESCRIPTION | DATASHEETS | PRICING/AVAILABILITY/PKG | SAMPLES | APPLICATION NOTES | USER GUIDES | MORE LITERATURE

PRODUCT SUPPORT: TRAINING

SN74ABT377A, Octal Edge-Triggered D-Type Flip-Flops With Clock Enable

DEVICE STATUS: **ACTIVE**

PARAMETER NAME	SN74ABT377A
Voltage Nodes (V)	5
Vcc range (V)	4.5 to 5.5
Input Level	TTL
Output Level	TTL
Output Drive (mA)	-32/64
Output	2S
No. of Bits	8
Static Current	15.2
th (ns)	1.8
tpd max (ns)	7.3
tsu (ns)	3

FEATURES

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- State-of-the-Art EPIC-IIB™ BiCMOS Design Significantly Reduces Power Dissipation
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- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
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EPIC-IIB is a trademark of Texas Instruments Incorporated.

DESCRIPTION

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These 8-bit positive-edge-triggered D-type flip-flops with a clock (CLK) input are particularly suitable for implementing buffer and storage registers, shift registers, and pattern generators.

Data (D) input information that meets the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse if the common clock-enable ($\overline{CLKEN}$) input is low. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the buffered clock (CLK) input is at either the high or low level, the D-input signal has no effect at the output. The circuits are designed to prevent false clocking by transitions at $\overline{CLKEN}$.

The SN54ABT377 is characterized for operation over the full military temperature range of -55°C to 125°C. The SN74ABT377A is characterized for operation from -40°C to 85°C.

Product Folder: SN74ABT377A, Octal Edge-Triggered D-Type Flip-Flops With Clock Enable

TECHNICAL DOCUMENTS

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DATASHEET

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Full datasheet in Acrobat PDF: sn74abt377a.pdf (108 KB,Rev.E) (Updated: 01/01/1997)

APPLICATION NOTES

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View Application Notes for Digital Logic

- Advanced BiCMOS Technology (ABT) Logic Characterization Information (Rev. B) (SCBA008B - Updated: 06/01/1997)
- Advanced BiCMOS Technology (ABT) Logic Enables Optimal System Design (Rev. A) (SCBA001A - Updated: 03/01/1997)
- Bus-Interface Devices With Output-Damping Resistors Or Reduced-Drive Outputs (Rev. A) (SCBA012A - Updated: 08/01/1997)
- Designing With Logic (Rev. C) (SDYA009C - Updated: 06/01/1997)
- Evaluation of Nickel/Palladium/Gold-Finished Surface-Mount Integrated Circuits (SZZA026 - Updated: 06/20/2001)
- Family of Curves Demonstrating Output Skews for Advanced BiCMOS Devices (Rev. A) (SCBA006A - Updated: 12/01/1996)
- Implications of Slow or Floating CMOS Inputs (Rev. C) (SCBA004C - Updated: 02/01/1998)
- Input and Output Characteristics of Digital Integrated Circuits (SDYA010 - Updated: 10/01/1996)
- Live Insertion (SDYA012 - Updated: 10/01/1996)
- Power-Up 3-State (PU3S) Circuits in TI Standard Logic Devices (SZZA033 - Updated: 05/10/2002)
- Quad Flatpack No-Lead Logic Packages (Rev. C) (SCBA017C - Updated: 11/22/2002)
- TI IBIS File Creation, Validation, and Distribution Processes (SZZA034 - Updated: 08/29/2002)
- Understanding Advanced Bus-Interface Products Design Guide (SCAA029, 253 KB - Updated: 05/01/1996)
- Understanding and Interpreting Texas Instruments Standard-Logic Products Data Sh (Rev. A) (SZZA036A - Updated: 02/27/2003)

MORE LITERATURE

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- Enhanced Plastic Portfolio Brochure (SGZB004, 387 KB - Updated: 08/19/2002)
- Logic Reference Guide (SCYB004, 1032 KB - Updated: 10/23/2001)
- MicroStar Junior BGA Design Summary (SCET004, 167 KB - Updated: 07/28/2000)
- Military Brief (SGYN138, 803 KB - Updated: 10/10/2000)
- Overview of IEEE Std 91-1984, Explanation of Logic Symbols Training Booklet (Rev. A) (SDYZ001A, 138 KB - Updated: 07/01/1996)
- Palladium Lead Finish User's Manual (SDYV001, 2041 KB - Updated: 11/01/1996)
- QML Class V Space Products Military Brief (Rev. A) (SGZN001A, 257 KB - Updated: 10/07/2002)

USER GUIDES

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- LOGIC Pocket Data Book (SCYD013, 4837 KB - Updated: 12/05/2002)

SAMPLES

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ORDERABLE DEVICE	PACKAGE INDUSTRY (TI)	PINS	TEMP (°C)	STATUS	PRODUCT CONTENT	SAMPLES
SN74ABT377ADBR	SSOP (DB)	20	-40 TO 85	ACTIVE	View Product Content	Request Samples
SN74ABT377ADW	SOIC (DW)	20	-40 TO 85	ACTIVE	View Product Content	Request Samples
SN74ABT377ADWR	SOIC (DW)	20	-40 TO 85	ACTIVE	View Product Content	Request Samples
SN74ABT377AN	PDIP (N)	20	-40 TO 85	ACTIVE	View Product Content	Request Samples
SN74ABT377APWR	TSSOP (PW)	20	-40 TO 85	ACTIVE	View Product Content	Request Samples

PRICING/AVAILABILITY/PKG

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Product Folder: SN74ABT377A, Octal Edge-Triggered D-Type Flip-Flops With Clock Enable

DEVICE INFORMATION (Updated Daily)							TI INVENTORY STATUS (As Of 09:00 AM GMT, 17 Apr 2003)			REPORTED DISTRIBUTOR INVENTORY (As Of 09:00 AM GMT, 17 Apr 2003)		
ORDERABLE DEVICE	STATUS	PACKAGE TYPE | PINS	TEMP (°C)	PRODUCT CONTENT	BUDGETARY PRICING QTY | $US	STD PACK QTY	IN STOCK	IN PROGRESS QTY | DATE	LEAD TIME	DISTRIBUTOR COMPANY | REGION	IN STOCK	PURCHASE
SN74ABT377ADBLE	OBSOLETE	SSOP (DB) | 20	-40 TO 85	View Contents	1KU |		0*		Call**	None Reported View Distributors		
SN74ABT377ADBR	ACTIVE	SSOP (DB) | 20	-40 TO 85	View Contents	1KU | 0.26	2000	0*	>10k | 08 May	4 WKS	Avnet | Americas	>1k	BUY NOW
										DigiKey | Americas	>1k	BUY NOW
SN74ABT377ADW	ACTIVE	SOIC (DW) | 20	-40 TO 85	View Contents	1KU | 0.26	25	225*	>10k | 12 May	4 WKS	Avnet | Americas	>1k	BUY NOW
										EBV Electronik | Europe	800	BUY NOW
										DigiKey | Americas	106	BUY NOW
										Avnet-SILICA | Europe	75	BUY NOW
SN74ABT377ADWR	ACTIVE	SOIC (DW) | 20	-40 TO 85	View Contents	1KU | 0.26	2000	2163*	>10k | 01 May	4 WKS	DigiKey | Americas	>1k	BUY NOW
SN74ABT377AN	ACTIVE	PDIP (N) | 20	-40 TO 85	View Contents	1KU | 0.26	20	0*	460 | 30 Apr	4 WKS	DigiKey | Americas	>1k	BUY NOW
										Insight | Americas	940	BUY NOW
										Avnet-SILICA | Europe	660	BUY NOW
SN74ABT377ANSR	ACTIVE	SOP (NS) | 20		View Contents	1KU | 0.75	2000	0*	>10k | 12 May	4 WKS	None Reported View Distributors		
SN74ABT377APW	ACTIVE	TSSOP (PW) | 20	-40 TO 85	View Contents	1KU | 0.48	70	0*	>10k | 08 May	4 WKS	None Reported View Distributors		
SN74ABT377APWLE	OBSOLETE	TSSOP (PW) | 20	-40 TO 85	View Contents	1KU |		0*		Call**	None Reported View Distributors		
SN74ABT377APWR	ACTIVE	TSSOP (PW) | 20	-40 TO 85	View Contents	1KU | 0.26	2000	0*	1424 | 21 Apr	4 WKS	DigiKey | Americas	642	BUY NOW
								>10k | 08 May				

Table Data Updated on: 4/17/2003

SN54ABT377, Octal Edge-Triggered D-type Flip-Flops With Clock Enable

DEVICE STATUS: **ACTIVE**

PARAMETER NAME	SN54ABT377
Voltage Nodes (V)	5

FEATURES

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DESCRIPTION

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APPLICATION NOTES

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Product Folder: SN54ABT377, Octal Edge-Triggered D-type Flip-Flops With Clock Enable

- Advanced BiCMOS Technology (ABT) Logic Enables Optimal System Design (Rev. A) (SCBA001A - Updated: 03/01/1997)
- Bus-Interface Devices With Output-Damping Resistors Or Reduced-Drive Outputs (Rev. A) (SCBA012A - Updated: 08/01/1997)
- Designing With Logic (Rev. C) (SDYA009C - Updated: 06/01/1997)
- Evaluation of Nickel/Palladium/Gold-Finished Surface-Mount Integrated Circuits (SZZA026 - Updated: 06/20/2001)
- Family of Curves Demonstrating Output Skews for Advanced BiCMOS Devices (Rev. A) (SCBA006A - Updated: 12/01/1996)
- Implications of Slow or Floating CMOS Inputs (Rev. C) (SCBA004C - Updated: 02/01/1998)
- Input and Output Characteristics of Digital Integrated Circuits (SDYA010 - Updated: 10/01/1996)
- Live Insertion (SDYA012 - Updated: 10/01/1996)
- Power-Up 3-State (PU3S) Circuits in TI Standard Logic Devices (SZZA033 - Updated: 05/10/2002)
- Quad Flatpack No-Lead Logic Packages (Rev. C) (SCBA017C - Updated: 11/22/2002)
- TI IBIS File Creation, Validation, and Distribution Processes (SZZA034 - Updated: 08/29/2002)
- Understanding Advanced Bus-Interface Products Design Guide (SCAA029, 253 KB - Updated: 05/01/1996)
- Understanding and Interpreting Texas Instruments Standard-Logic Products Data Sh (Rev. A) (SZZA036A - Updated: 02/27/2003)

MORE LITERATURE

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- Enhanced Plastic Portfolio Brochure (SGZB004, 387 KB - Updated: 08/19/2002)
- Logic Reference Guide (SCYB004, 1032 KB - Updated: 10/23/2001)
- MicroStar Junior BGA Design Summary (SCET004, 167 KB - Updated: 07/28/2000)
- Military Brief (SGYN138, 803 KB - Updated: 10/10/2000)
- Overview of IEEE Std 91-1984, Explanation of Logic Symbols Training Booklet (Rev. A) (SDYZ001A, 138 KB - Updated: 07/01/1996)
- Palladium Lead Finish User's Manual (SDYV001, 2041 KB - Updated: 11/01/1996)
- QML Class V Space Products Military Brief (Rev. A) (SGZN001A, 257 KB - Updated: 10/07/2002)

USER GUIDES

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- LOGIC Pocket Data Book (SCYD013, 4837 KB - Updated: 12/05/2002)

PRICING/AVAILABILITY/PKG

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DEVICE INFORMATION
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TI INVENTORY STATUS
As Of 09:00 AM GMT, 17 Apr 2003

REPORTED DISTRIBUTOR INVENTORY
As Of 09:00 AM GMT, 17 Apr 2003

ORDERABLE DEVICE	STATUS	PACKAGE TYPE | PINS	TEMP (°C)	DSCC NUMBER	PRODUCT CONTENT	BUDGETARY PRICING QTY | $US	STD PACK QTY	IN STOCK	IN PROGRESS QTY | DATE	LEAD TIME	DISTRIBUTOR COMPANY | REGION	IN STOCK	PURCHASE
5962-9314801Q2A	ACTIVE	LCCC (FK) | 20	-55 TO 125		View Contents	1KU | 8.08	1	68*	3942 | 20 May	8 WKS	Avnet | Americas	2	BUY NOW
									>10k | 27 May				
5962-9314801QRA	ACTIVE	CDIP (J) | 20	-55 TO 125		View Contents	1KU | 4.86	1	16*	>10k | 20 May	8 WKS	Avnet | Americas	1	BUY NOW
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SNJ54ABT377FK	ACTIVE	LCCC (FK) | 20	-55 TO 125	5962-9314801Q2A	View Contents	1KU | 8.08	1	0*	3889 | 20 May	8 WKS	None Reported View Distributors		
									>10k | 27 May				
SNJ54ABT377J	ACTIVE	CDIP (J) | 20	-55 TO 125	5962-9314801QRA	View Contents	1KU | 4.86	1	0*	>10k | 20 May	8 WKS	None Reported View Distributors		
SNJ54ABT377W	ACTIVE	CFP (W) | 20	-55 TO 125	5962-9314801QSA	View Contents	1KU | 8.58	1	0*	>10k | 20 May	8 WKS	None Reported View Distributors		

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