3.3V CMOS 16-BIT EDGE-TRIGGERED D-TYPE FLIP-FLOP WITH 3-STATE OUTPUTS, 5 VOLT TOLERANT I/O

IDT74LVC16374A

FEATURES:

- Typical $t_{SK(0)}$ (Output Skew) < 250ps
- ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
- 0.635mm pitch SSOP, 0.50mm pitch TSSOP and 0.40mm pitch TVSOP packages
- Extended commercial range of -40°C to +85°C
- V_{CC} = 3.3V ±0.3V, Normal Range
- V_{CC} = 2.7V to 3.6V, Extended Range
- CMOS power levels (0.4µW typ. static)
- All inputs, outputs and I/O are 5 Volt tolerant
- Supports hot insertion

Drive Features for LVC16374A:

- High Output Drivers: ±24mA
- Reduced system switching noise

APPLICATIONS:

- 5V and 3.3V mixed voltage systems
- Data communication and telecommunication systems

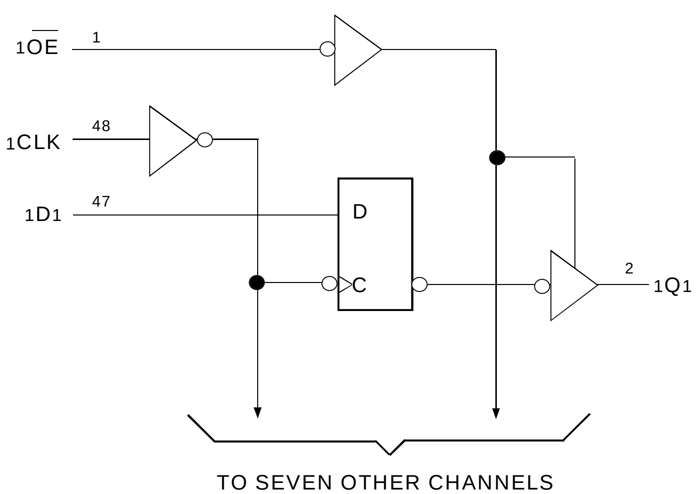
DESCRIPTION:

The LVC16374A 16-bit edge-triggered D-type flip-flop is built using advanced dual metal CMOS technology. This high-speed, low-power register is ideal for use as a buffer register for data synchronization and storage. The Output Enable ($\overline{OE}$) and clock (CLK) controls are organized to operate this device as two 8-bit registers or one 16-bit register with common clock. Flow-through organization of signal pins simplifies layout. All inputs are designed with hysteresis for improved noise margin.

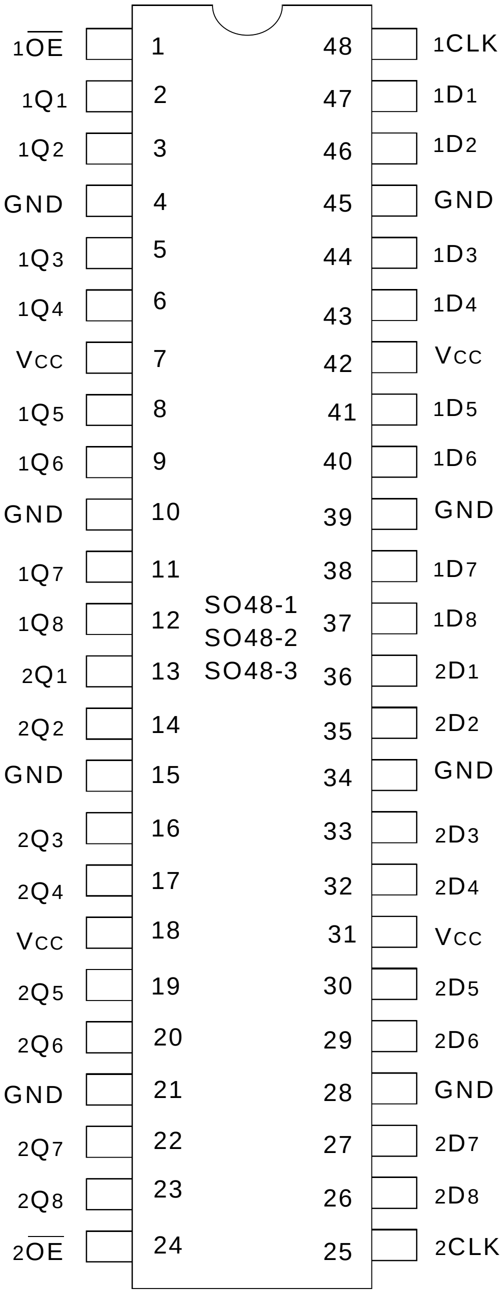
All pins of the LVC16374A can be driven from either 3.3V or 5V devices. This feature allows the use of this device as a translator in a mixed 3.3V/5V supply system.

The LVC16374A has been designed with a ±24mA output driver. This driver is capable of driving a moderate to heavy load while maintaining speed performance.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



SSOP/ TSSOP/ TVSOP
TOP VIEW

PIN DESCRIPTION

Pin Names	Description
xDx	Data Inputs
xCLK	Clock Inputs
xQx	3-State Outputs
x$\overline{OE}$	3-State Output Enable Inputs (Active LOW)

ABSOLUTE MAXIMUM RATINGS (1)

Symbol	Description	Max.	Unit
V_{TERM}	Terminal Voltage with Respect to GND	– 0.5 to +6.5	V
T_{STG}	Storage Temperature	– 65 to +150	°C
I_{OUT}	DC Output Current	– 50 to +50	mA
I_{IK} I_{OK}	Continuous Clamp Current, $V_I < 0$ or $V_O < 0$	– 50	mA
I_{CC} I_{SS}	Continuous Current through each V_{CC} or GND	±100	mA

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NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	4.5	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	6.5	8	pF
$C_{I/O}$	I/O Port Capacitance	V_{IN} = 0V	6.5	8	pF

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NOTE:

1. As applicable to the device type.

FUNCTION TABLE (each flip-flop) (1)

Inputs			Outputs
xDx	xCLK	x$\overline{OE}$	xQx
X	L	H	Z
X	H	H	Z
L	↑	L	L
H	↑	L	H
L	H	L	Q_0
H	L	L	Q_0

NOTE:

1. H = HIGH Voltage Level
   L = LOW Voltage Level
   X = Don't Care
   Z = High-Impedance
   ↑ = LOW-to-HIGH Transition
   Q_0 = Output level of Q before the indicated steady-stte input conditions were established.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Operating Condition: $T_A = -40^{\circ}C$ to $+85^{\circ}C$

Symbol	Parameter	Test Conditions		Min.	Typ.(1)	Max.	Unit
V_{IH}	Input HIGH Voltage Level	V_{CC} = 2.3V to 2.7V		1.7	—	—	V
		V_{CC} = 2.7V to 3.6V		2	—	—	
V_{IL}	Input LOW Voltage Level	V_{CC} = 2.3V to 2.7V		—	—	0.7	V
		V_{CC} = 2.7V to 3.6V		—	—	0.8	
I_{IH} I_{IL}	Input Leakage Current	V_{CC} = 3.6V	V_I = 0 to 5.5V	—	—	±5	µA
I_{OZH} I_{OZL}	High Impedance Output Current (3-State Output pins)	V_{CC} = 3.6V	V_O = 0 to 5.5V	—	—	±10	µA
I_{OFF}	Input/Output Power Off Leakage	V_{CC} = 0V, V_{IN} or $V_O \leq 5.5V$		—	—	±50	µA
V_{IK}	Clamp Diode Voltage	V_{CC} = 2.3V, I_{IN} = – 18mA		—	– 0.7	– 1.2	V
V_H	Input Hysteresis	V_{CC} = 3.3V		—	100	—	mV
I_{CCL} I_{CCH} I_{CCZ}	Quiescent Power Supply Current	V_{CC} = 3.6V	V_{IN} = GND or V_{CC}	—	—	10	µA
			$3.6 \leq V_{IN} \leq 5.5V$(2)	—	—	10	
ΔI_{CC}	Quiescent Power Supply Current Variation	One input at V_{CC} - 0.6V other inputs at V_{CC} or GND		—	—	500	µA

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NOTES:
1. Typical values are at V_{CC} = 3.3V, +25°C ambient.
2. This applies in the disabled state only.

OUTPUT DRIVE CHARACTERISTICS

Symbol	Parameter	Test Conditions(1)		Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = 2.3V to 3.6V	I_{OH} = – 0.1mA	V_{CC} – 0.2	—	V
		V_{CC} = 2.3V	I_{OH} = – 6mA	2	—	
		V_{CC} = 2.3V	I_{OH} = – 12mA	1.7	—	
		V_{CC} = 2.7V		2.2	—	
		V_{CC} = 3.0V		2.4	—	
		V_{CC} = 3.0V	I_{OH} = – 24mA	2.2	—	
V_{OL}	Output LOW Voltage	V_{CC} = 2.3V to 3.6V	I_{OL} = 0.1mA	—	0.2	V
		V_{CC} = 2.3V	I_{OL} = 6mA	—	0.4	
			I_{OL} = 12mA	—	0.7	
		V_{CC} = 2.7V	I_{OL} = 12mA	—	0.4	
		V_{CC} = 3.0V	I_{OL} = 24mA	—	0.55	

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NOTE:
1. V_{IH} and V_{IL} must be within the min. or max. range shown in the DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE table for the appropriate V_{CC} range. T_A = – 40°C to +85°C.

OPERATING CHARACTERISTICS, V_{CC} = 3.3V ± 0.3V, T_A = 25°C

Symbol	Parameter	Test Conditions	Typical	Unit
C_{PD}	Power Dissipation Capacitance per Flip-Flop Outputs enabled	C_L = 0pF, f = 10Mhz	58	pF
C_{PD}	Power Dissipation Capacitance per Flip-Flop Outputs disabled		24	pF

SWITCHING CHARACTERISTICS OVER OPERATING RANGE (1)

		VCC = 2.7V		VCC = 3.3V±0.3V		
Symbol	Parameter	Min.	Max.	Min.	Max.	Unit
f_{MAX}		150	—	150	—	MHz
t_{PLH} t_{PHL}	Propagation Delay xCLK to xQx	—	4.9	1.5	4.5	ns
t_{PZH} t_{PZL}	Output Enable Time x$\overline{OE}$ to xQx	—	5.3	1.5	4.6	ns
t_{PHZ} t_{PLZ}	Output Disable Time x$\overline{OE}$ to xQx	—	6.1	1.5	5.5	ns
t_{SU}	Set-up Time HIGH or LOW, xDx to xCLK	1.9	—	1.9	—	ns
t_H	Hold Time HIGH or LOW, xDx after xCLK	1.1	—	1.1	—	ns
t_W	xCLK Pulse Width HIGH or LOW	3.3	—	3.3	—	ns
$t_{SK}(o)$	Output Skew (2)	—	—	—	500	ps

NOTES:
1. See test circuits and waveforms. T_A = – 40°C to + 85°C.
2. Skew between any two outputs of the same package and switching in the same direction.

TEST CIRCUITS AND WAVEFORMS:

TEST CONDITIONS

Symbol	VCC(1)= 3.3V ±0.3V	VCC(1) = 2.7V	VCC(2)= 2.5V ±0.2V	Unit
VLOAD	6	6	2 x Vcc	V
VIH	2.7	2.7	Vcc	V
VT	1.5	1.5	Vcc / 2	V
VLZ	300	300	150	mV
VHZ	300	300	150	mV
CL	50	50	30	pF

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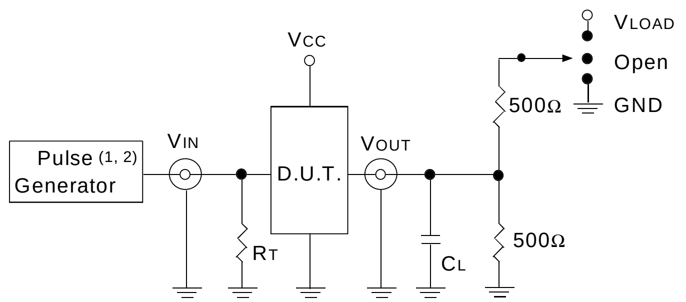
TEST CIRCUITS FOR ALL OUTPUTS



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DEFINITIONS:

CL = Load capacitance: includes jig and probe capacitance.
RT = Termination resistance: should be equal to ZOUT of the Pulse Generator.

NOTES:

1. Pulse Generator for All Pulses: Rate ≤ 10MHz; tF ≤ 2.5ns; tR ≤ 2.5ns.
2. Pulse Generator for All Pulses: Rate ≤ 10MHz; tF ≤ 2ns; tR ≤ 2ns.

SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	VLOAD
Disable High Enable High	GND
All Other tests	Open

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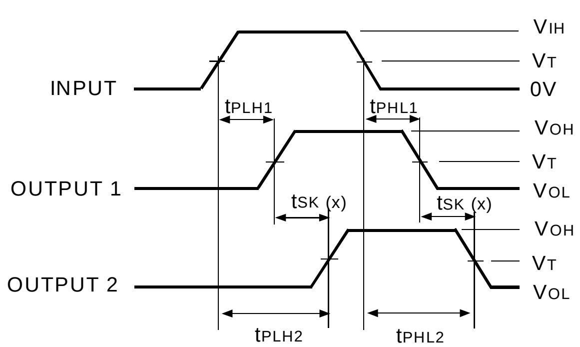
OUTPUT SKEW - tsk (x)



$t_{SK(x)} = |t_{PLH2} - t_{PLH1}|$ or $|t_{PHL2} - t_{PHL1}|$

NOTES:

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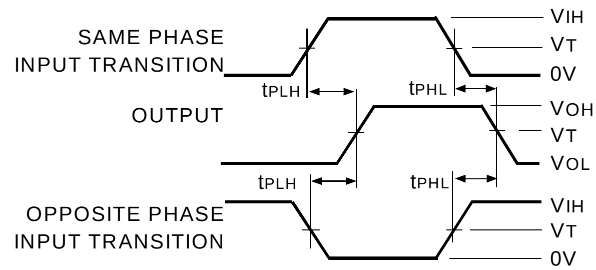
1. For tSK(o) OUTPUT1 and OUTPUT2 are any two outputs.
2. For tSK(b) OUTPUT1 and OUTPUT2 are in the same bank.

PROPAGATION DELAY



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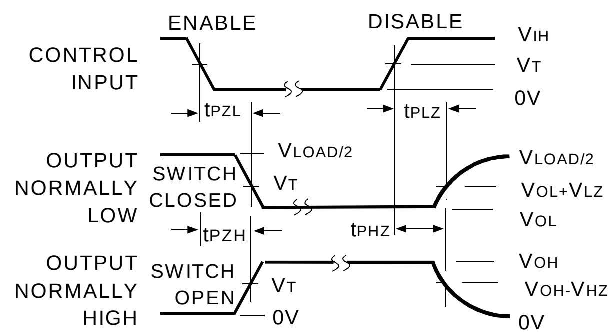
ENABLE AND DISABLE TIMES



NOTE:

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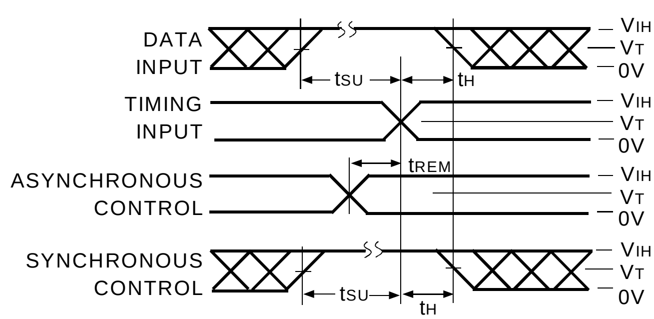
1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.

SET-UP, HOLD, AND RELEASE TIMES



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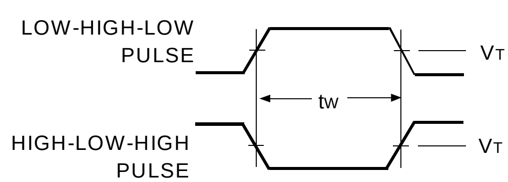
PULSE WIDTH



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ORDERING INFORMATION

IDT	XX	LVC	X	XX	XXXX	XX
	Temp. Range		Bus-Hold	Family	Device Type	Package

Field	Code	Description
Package	PV	Shrink Small Outline Package (SO48-1)
	PA	Thin Shrink Small Outline Package (SO48-2)
	PF	Thin Very Small Outline Package (SO48-3)
Device Type	374A	16-Bit Edge-Triggered D-Type Flip-Flop with 3-State Outputs, 5 volt Tolerant I/O
Family	16	Double-Density with Resistors, ±24mA
Bus-Hold	Blank	No Bus-hold
Temp. Range	74	-40°C to +85°C

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