QUAD 2-INPUT MULTIPLEXER; INVERTING

FEATURES
- Inverting data path
- Output capability: standard
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT158 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT158 are quad 2-input multiplexers which select 4 bits of data from two sources and are controlled by a common data select input (S). The four outputs present the selected data in the inverted form. The enable input ($\overline{E}$) is active LOW.

When $\overline{E}$ is HIGH, all the outputs ($1\overline{Y}$ to $4\overline{Y}$) are forced HIGH regardless of all other input conditions.

Moving the data from two groups of registers to four common output buses is a common use of the "158". The state of S determines the particular register from which the data comes. It can also be used as a function generator.

The device is useful for implementing highly irregular logic by generating any four of the 16 different functions of two variables with one variable common.

The "158" is the logic implementation of a 4-pole, 2-position switch, where the position of the switch is determined by the logic levels applied to S.

The logic equations for the output are:

$1\overline{Y} = \overline{E}.(1I_1.S + 1I_0.\overline{S})$

$2\overline{Y} = \overline{E}.(2I_1.S + 2I_0.\overline{S})$

$3\overline{Y} = \overline{E}.(3I_1.S + 3I_0.\overline{S})$

$4\overline{Y} = \overline{E}.(4I_1.S + 4I_0.\overline{S})$

The "158" is identical to the "157" but has inverting outputs.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
$t_{PHL}/$ t_{PLH}	propagation delay nI_0, nI_1 to $n\overline{Y}$ $\overline{E}$ to $n\overline{Y}$ S to $n\overline{Y}$	C_L = 15 pF V_{CC} = 5 V	12 14 14	13 16 16	ns ns ns
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per multiplexer	notes 1 and 2	40	40	pF

GND = 0 V; T_{amb} = 25 °C; t_r = t_f = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):

$P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:

f_i = input frequency in MHz C_L = output load capacitance in pF
f_o = output frequency in MHz V_{CC} = supply voltage in V
$\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs

2. For HC the condition is V_I = GND to V_{CC}
For HCT the condition is V_I = GND to V_{CC} − 1.5 V

PACKAGE OUTLINES

SEE PACKAGE INFORMATION SECTION

PIN DESCRIPTION

| PIN NO.	SYMBOL	NAME AND FUNCTION
1	S	common data select input
2, 5, 11, 14	$1I_0$ to $4I_0$	data inputs from source 0
3, 6, 10, 13	$1I_1$ to $4I_1$	data inputs from source 1
4, 7, 9, 12	$1\overline{Y}$ to $4\overline{Y}$	multiplexer outputs
8	GND	ground (0 V)
15	$\overline{E}$	enable input (active LOW)
16	V_{CC}	positive supply voltage
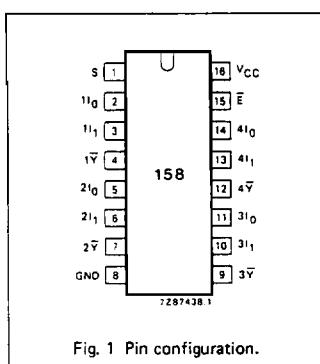
Fig. 1 Pin configuration.
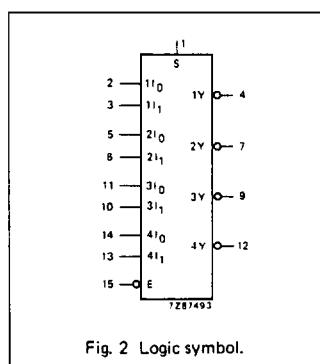
Fig. 2 Logic symbol.

Fig. 3 IEC logic symbol.

Fig. 4 Functional diagram.
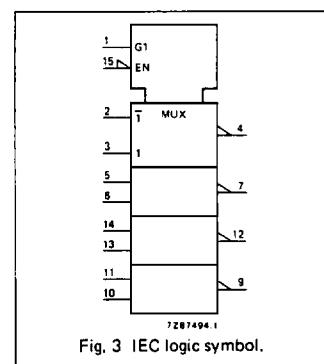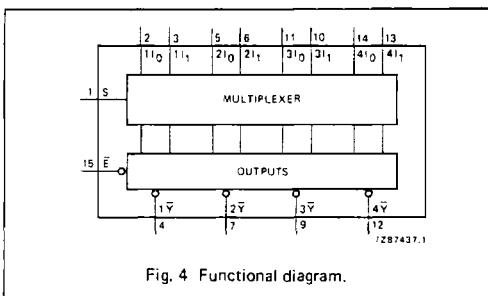
FUNCTION TABLE

INPUTS				OUTPUT
$\overline{E}$	S	nI_0	nI_1	$n\overline{Y}$
H	X	X	X	H
L	L	L	X	H
L	L	H	X	L
L	H	X	L	H
L	H	X	H	L

H = HIGH voltage level
L = LOW voltage level
X = don't care

Fig. 5 Logic diagram.
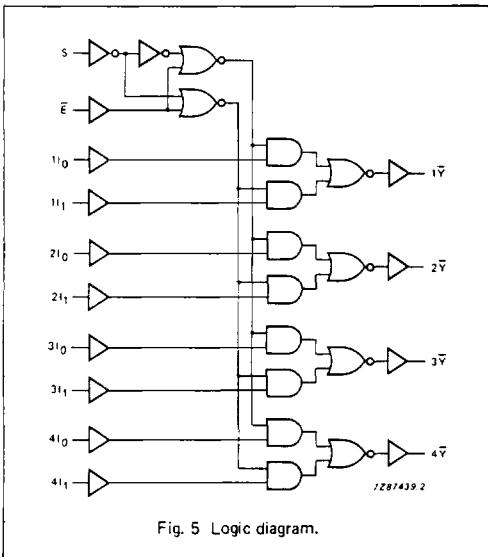
DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard
I_{CC} category: MSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C) 74HC							UNIT	V_{CC} V	TEST CONDITIONS WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
$t_{PHL}/$ t_{PLH}	propagation delay nI_0, nI_1 to $n\overline{Y}$		41 15 12	125 25 21		155 31 26		190 38 32	ns	2.0 4.5 6.0	Fig. 7
$t_{PHL}/$ t_{PLH}	propagation delay $\overline{E}$ to $n\overline{Y}$		47 17 14	145 29 25		180 36 31		220 44 38	ns	2.0 4.5 6.0	Fig. 6
$t_{PHL}/$ t_{PLH}	propagation delay S to $n\overline{Y}$		47 17 14	145 29 25		180 36 31		220 44 38	ns	2.0 4.5 6.0	Fig. 7
$t_{THL}/$ t_{TLH}	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Figs 6 and 7

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard
I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications.
To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
nI_0	0.40
nI_1	0.40
S	2.80
$\overline{E}$	0.60

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f = 6$ ns; $C_L = 50$ pF

SYMBOL	PARAMETER	T_{amb} (°C) 74HCT							UNIT	TEST CONDITIONS	
		+25			−40 to +85		−40 to +125			V_{CC} V	WAVEFORMS
		min.	typ.	max.	min.	max.	min.	max.			
$t_{PHL}/$ t_{PLH}	propagation delay nI_0, nI_1 to $n\overline{Y}$		16	30		38		45	ns	4.5	Fig. 7
$t_{PHL}/$ t_{PLH}	propagation delay $\overline{E}$ to $n\overline{Y}$		19	35		44		53	ns	4.5	Fig. 6
$t_{PHL}/$ t_{PLH}	propagation delay S to $n\overline{Y}$		19	35		44		53	ns	4.5	Fig. 7
$t_{THL}/$ t_{TLH}	output transition time		7	15		19		22	ns	4.5	Figs 6 and 7

AC WAVEFORMS
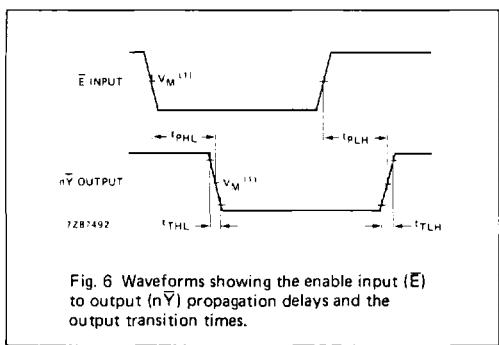
Fig. 6 Waveforms showing the enable input ($\overline{E}$) to output (n$\overline{Y}$) propagation delays and the output transition times.
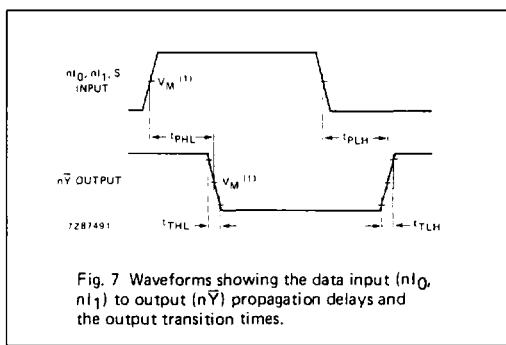
Fig. 7 Waveforms showing the data input (nI$_0$, nI$_1$) to output (n$\overline{Y}$) propagation delays and the output transition times.

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
  HCT: V_M = 1.3 V; V_I = GND to 3 V.