Signetics

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Status	Product Specification
FAST Products	

FAST 74F5074
Flip-Flop/ Clock Driver

Synchronizing Dual D-Type Flip-Flop
With Metastable Immune Characteristics

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F5074	120 MHz	20mA

FEATURES

- **Metastable Immune Characteristics**
- **Propagation delay skew and output to output skew guaranteed less than 1.5ns**
- **High source current (I_{OH} = 15mA) ideal for clock driver applications**
- **Pinout compatible with 74F74**
- **See 74F50728 for Synchronizing Cascaded D-Type Flip-Flop**
- **See 74F50729 for Synchronizing Dual D-Type Flip-Flop with Edge-Triggered Set and Reset**
- **See 74F50109 for Synchronizing Dual J-$\overline{K}$ Positive Edge-Triggered Flip-Flops**

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
14-Pin Plastic DIP	N74F5074N
14-Pin Plastic SO	N74F5074D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D_0, D_1	Data inputs	1.0/0.417	20µA/250µA
CP_0, CP_1	Clock inputs (active rising edge)	1.0/0.033	20µA/20µA
$\overline{S}_{D0}$, $\overline{S}_{D1}$	Set inputs (active Low)	1.0/0.033	20µA/20µA
$\overline{R}_{D0}$, $\overline{R}_{D1}$	Reset inputs (active Low)	1.0/0.033	20µA/20µA
Q_0, Q_1, $\overline{Q}_0$, $\overline{Q}_1$	Data outputs	750/33	15mA/20mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

DESCRIPTION

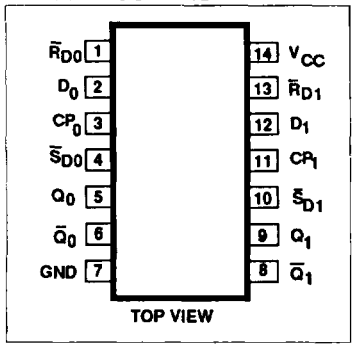
The 74F5074 is a dual positive edge-triggered D-type flip-flop featuring individual Data, Clock, Set and Reset inputs; also true and complementary outputs.

Set ($\overline{S}_{Dn}$) and Reset ($\overline{R}_{Dn}$) are asynchronous active-Low inputs and operate independently of the Clock (CP_n) input. Data must be stable just one setup time prior to the Low-to-High transition of the clock for guaranteed propagation delays.

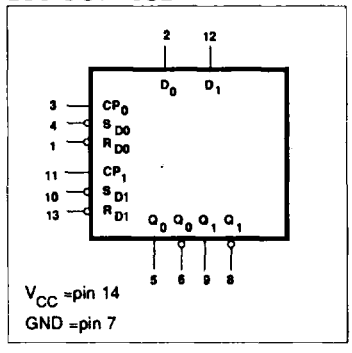
Clock triggering occurs at a voltage level and is not directly related to the transition time of the positive-going pulse. Following the hold time interval, data at the D_n input may be changed without affecting the levels of the output.

The 74F5074 is designed so that the outputs can never display a metastable state due to setup and hold time violations. If setup and hold times are violated the propagation delays may be extended beyond the specifications but the outputs will not glitch or display a metastable state. Typical metastability parameters for the 74F5074 are: $\tau \cong 135ps$ and $T_o \cong 9.8 \times 10^6$ sec where τ represents a function of the rate at which a latch in a metastable state resolves that condition and T_o represents a function of the measurement of the propensity of a latch to enter a metastable state.

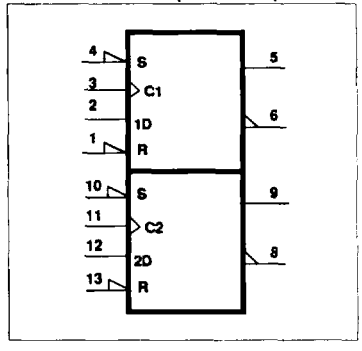
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL(IEEE/IEC)



Metastable Immune Characteristics

Signetics uses the term 'metastable immune' to describe characteristics of some of the products in its FAST family. Specifically the 74F50XXX family presently consists of 4 products which display metastable immune characteristics. This term means that the outputs will not glitch or display an output anomaly under any circumstances including setup and hold time violations. This claim is easily verified on the 74F5074.

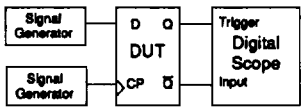


Fig. 1—Test Set up

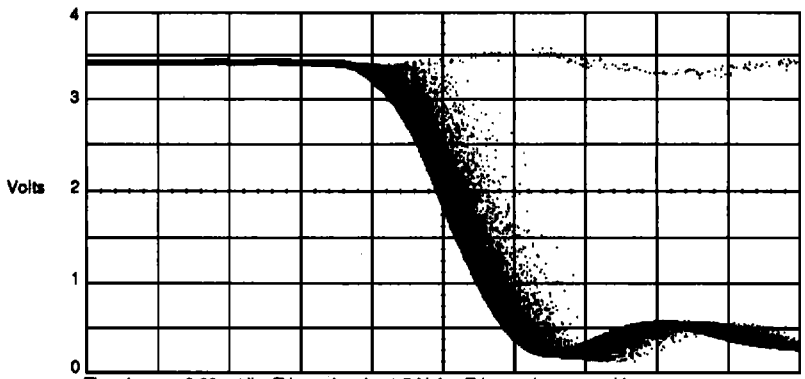
By running two independent signal generators (see Fig. 1) at nearly the same frequency (in this case 10 MHz clock and 10.02 MHz data) the device-under-test can often be driven into a metastable state. If the Q output is then used to trigger a digital scope set to infinite persistence the $\overline{Q}$ output will build a waveform. An experiment was run by continuously operating the devices in the region where metastability will occur.

When the device-under-test is a 74F74 (which was not designed with metastable immune characteristics) the waveform will appear as in Fig. 2.

Fig. 2 shows clearly that the $\overline{Q}$ output can vary in time with respect to the Q trigger point. This also implies that the Q or $\overline{Q}$ output waveshapes may be distorted. This can be verified on an analog scope with a charge plate CRT. Perhaps of even greater interest are the dots running along the 3.5 volt line in the upper right hand quadrant. These show that the $\overline{Q}$ output did not change state even though the Q output glitched to at least 1.5 volts, the trigger point of the scope.

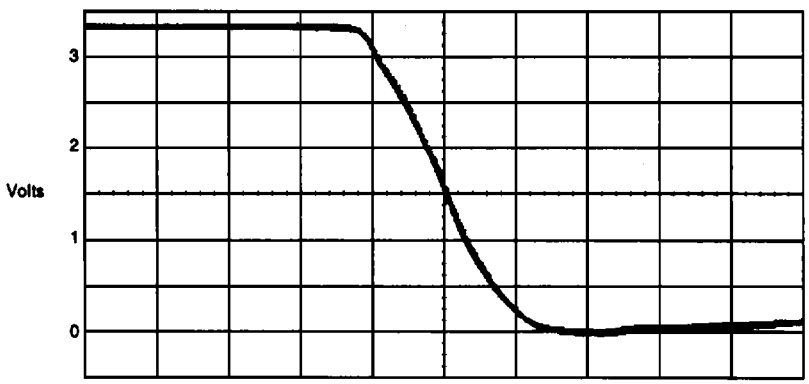
When the device-under-test is a metastable immune part, such as the 74F5074, the waveform will appear as in Fig. 3. The 74F5074 $\overline{Q}$ output will not vary with respect to the Q trigger point even when the part is driven into a metastable state. Any tendency towards internal metastability is resolved by Signetics

COMPARISON OF METASTABLE IMMUNE AND NON-IMMUNE CHARACTERISTICS



Time base = 2.00ns/div Trigger level = 1.5 Volts Trigger slope = positive

Fig. 2—74F74 $\overline{Q}$ output triggered by Q output, setup and hold times violated



Time base = 2.00ns/div Trigger level = 1.5 Volts Trigger slope = positive

Fig. 3—74F5074 $\overline{Q}$ output triggered by Q output, setup and hold times violated

patented circuitry. If a metastable event occurs within the flop the only outward manifestation of the event will be an increased Clock-to-Q/$\overline{Q}$ propagation delay. This propagation delay is, of course, a function of the metastability characteristics of the part defined by τ and T_o.

The metastability characteristics of the 74F5074 and related part types represent state-of-the art in TTL technology.
After determining the T_o and τ of the flop, calculating the mean time between failures (MTBF) is simple. Suppose a designer wants to use the F5074 for synchronizing asynchronous data that is arriving at 10MHz (as measured by a frequency counter), has a clock frequency of 50MHz , and has decided that he would like to sample the output of the F5074 10 nanoseconds after the clock edge.
He simply plugs his numbers into the equation below:

$$MTBF = e^{(t'/\tau)} / T_o f_C f_I$$

In this formula, f_C is the frequency of the clock, f_I is the average input event frequency, and t' is the time after the clock pulse that the output is sampled (t'>h, h being the normal propagation delay). In this situation the f_I will be twice the data frequency or 20MHz because input events consist of both low and high data transitions. Multiplying f_I by f_C gives an answer of 10^{15} Hz^2. From Fig. 4 it is clear that the MTBF is greater than 10^{10} seconds. Using the above formula the actual MTBF is 1.51×10^{10} seconds or about 480 years.

MEAN TIME BETWEEN FAILURES (MTBF) versus t'

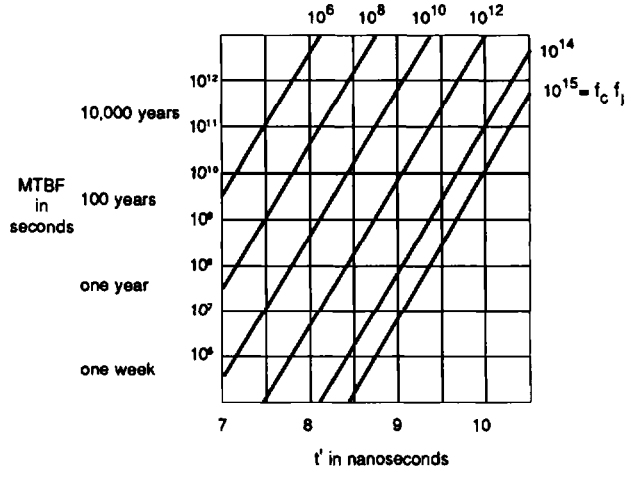
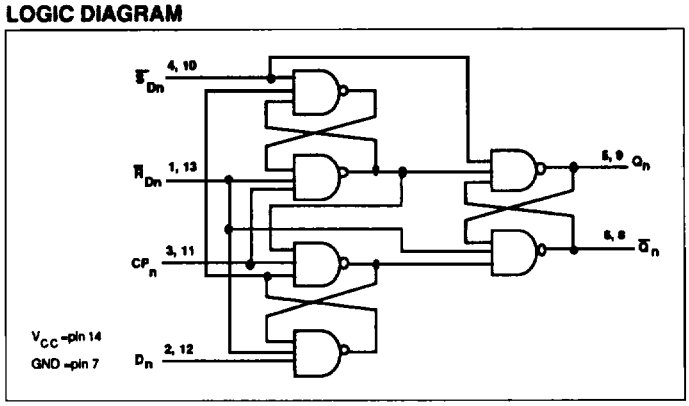


Fig. 4 MTBF versus t' for 74F5074 at τ = 135ps and T_o=9.8x 10^6 sec

Typical values for τ and T_e at various V_{CC}s and Temperatures

	0°C		25°C		70°C	
	τ	T_e	τ	T_e	τ	T_e
5.5 V	125 ps	1.0×10^9 sec	138ps	5.4×10^8sec	160 ps	1.7×10^5sec
5.0 V	115ps	1.3×10^{10} sec	135 ps	9.8×10^6sec	167ps	3.9×10^4sec
4.5 V	115 ps	3.4×10^{13}sec	132ps	5.1×10^8sec	175 ps	7.3×10^4sec

LOGIC DIAGRAM



FUNCTION TABLE

INPUTS				OUTPUTS		OPERATING MODE
$\overline{S}_{Dn}$	$\overline{R}_{Dn}$	CP_n	D_n	Q_n	$\overline{Q}_n$	
L	H	X	X	H	L	Asynchronous Set
H	L	X	X	L	H	Asynchronous Reset
L	L	X	X	H	H	Undetermined*
H	H	↑	h	H	L	Load "1"
H	H	↑	l	L	H	Load "0"
H	H	↥	X	NC	NC	Hold

H = High voltage level
h = High voltage level one setup time prior to Low-to-High clock transition
L = Low voltage level
l = Low voltage level one setup time prior to Low-to-High clock transition
NC =No change from the previous setup
X = Don't care

↥ = Low-to-High clock transition
↧ = Not a Low-to-High clock transition
* = This setup is unstable and will change when either Set or Reset return to the High level.

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				0.8	V
I_{IK}	Input clamp current				-18	mA
I_{OH}	High-level output current	V_{CC}±10%			-12	mA
		V_{CC}±5%			-15	mA
I_{OL}	Low-level output current				20	mA
T_A	Operating free-air temperature range		0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS[1]			LIMITS			UNIT
					Min	Typ[2]	Max	
V_{OH}	High-level output voltage	V_{CC} =MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = -12mA	±10%V_{CC}	2.5			V
				±5%V_{CC}	2.7	3.4		V
			I_{OH} = -15mA	±5%V_{CC}	2.0			V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} =MAX	±10%V_{CC}		0.30	0.50	V
				±5%V_{CC}		0.30	0.50	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}				-0.73	-1.2	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7.0V					100	µA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7V					20	µA
I_{IL}	Low-level input current $\frac{D_n}{CP_n, \overline{S}_{Dn}, \overline{R}_{Dn}}$	V_{CC} = MAX, V_I = 0.5V					-250	µA
							-20	µA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX			-60		-150	mA
I_{CC}	Supply current[4] (total)	V_{CC} = MAX				20	30	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
4. Measure I_{CC} with the clock input grounded and all outputs open, then with Q and $\overline{Q}$ outputs High in turn.

AC ELECTRICAL CHARACTERISTICS

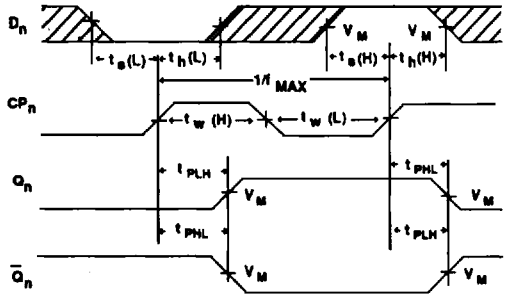
SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	105	120		85		MHz
t_{PLH} t_{PHL}	Propagation delay CP_n to Q_n or $\overline{Q}_n$	Waveform 1	2.0 2.0	3.9 3.9	6.0 6.0	1.5 2.0	6.5 6.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{S}_{Dn}$, $\overline{R}_{Dn}$ to Q_n or $\overline{Q}_n$	Waveform 2	3.0 3.0	4.5 5.0	7.5 7.5	2.5 2.5	8.0 8.0	ns
t_{PS}	Propagation delay Skew[1,3]	Waveform 4			1.0		1.0	ns
t_{OS}	Output to output Skew[2,3]	Waveform 4			1.5		1.5	ns

NOTE:
1. $|t_{PLH}$ actual - t_{PHL} actual $|$ for any output.
2. $|t_{PN}$ actual - t_{PM} actual $|$ for any output compared to any other output where N and M are either LH or HL.
3. Skew times are valid only under same test conditions (temperature, V_{CC}, loading, etc.,).

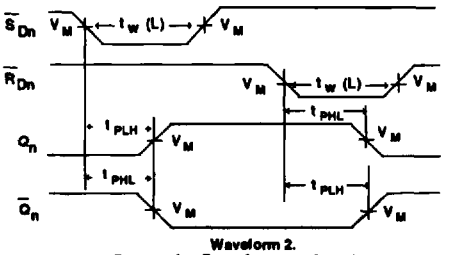
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low D_n to CP_n	Waveform 1	1.5 1.5			2.0 2.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low D_n to CP_n	Waveform 1	1.0 1.0			1.5 1.5		ns
$t_w(H)$ $t_w(L)$	CP Pulse width, High or Low	Waveform 1	3.0 4.0			3.0 4.5		ns
$t_w(L)$	$\overline{S}_{Dn}$ or $\overline{R}_{Dn}$ Pulse width, Low	Waveform 2	3.0			4.0		ns
t_{REC}	Recovery time $\overline{S}_{Dn}$ or $\overline{R}_{Dn}$ to CP_n	Waveform 3	3.0			3.5		ns

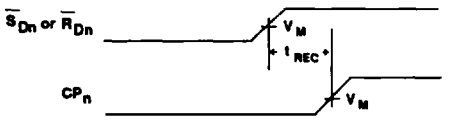
AC WAVEFORMS



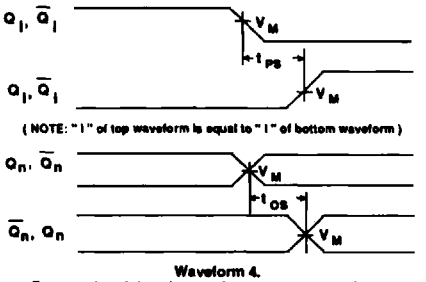
Waveform 1. Propagation Delay For data to output, data setup time and hold times, and clock width



Waveform 2.
Propagation Delay for set and reset to output, set and reset pulse width



Waveform 3.
Recovery time for set or reset to clock

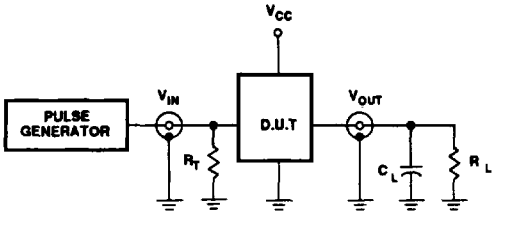


(NOTE: " i " of top waveform is equal to " i " of bottom waveform)

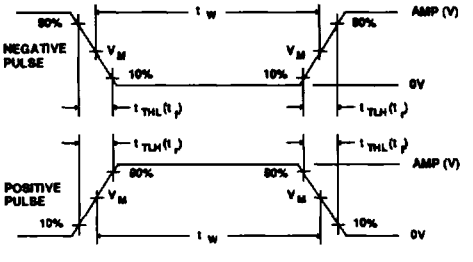
Waveform 4.
Propagation delay skew and output to output skew

NOTE: For all waveforms, V_M = 1.5V.
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For Totem-Pole Outputs



V_M = 1.5V
Input Pulse Definition

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns