



# High-Speed CMOS 8-Bit Bus Interface Register Transceivers

QS54/74FCT646T  
QS54/74FCT2646T

## FEATURES/BENEFITS

- Pin and function compatible to the 74F646, 74FCT646 and 74FCT646T
- Industrial temperature  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$
- CMOS power levels:  $<7.5\text{mW}$  static
- Available in DIP, SOIC, QSOP, ZIP, HQSOP
- Undershoot clamp diodes on all inputs
- TTL-compatible input and output levels
- Ground bounce controlled outputs
- Reduced output swing of 0-3.5V
- Military product compliant to MIL-STD-883, Class B

### FCT-T 646T

- JEDEC-FCT spec compatible
- Std., A, C, and D speed grades with  $4.8\text{ns}$   $t_{PD}$  for D
- $I_{OL} = 64\text{mA}$  Ind.,  $48\text{mA}$  Mil.

### FCT-T 2646T

- Built-in  $25\Omega$  series resistor outputs reduce reflection and other system noise
- A and C speed grades with  $5.4\text{ns}$   $t_{PD}$  for C
- $I_{OL} = 12\text{mA}$  Ind.

## DESCRIPTION

The QSFCT646T and QSFCT2646T are 8-bit high-speed CMOS TTL-compatible registered bus transceivers with three-state outputs that are ideal for driving high capacitance loads such as memory and address buses. The 2646 device is a  $25\Omega$  resistor output version useful for driving transmission lines and reducing system noise. The 2646 series parts can replace the 646 series to reduce noise in an existing design. All inputs have clamp diodes for undershoot noise suppression. All outputs have ground bounce suppression (see QSI Application Note AN-001), and outputs will not load an active bus when  $V_{CC}$  is removed from the device.

Figure 1. Functional Block Diagram

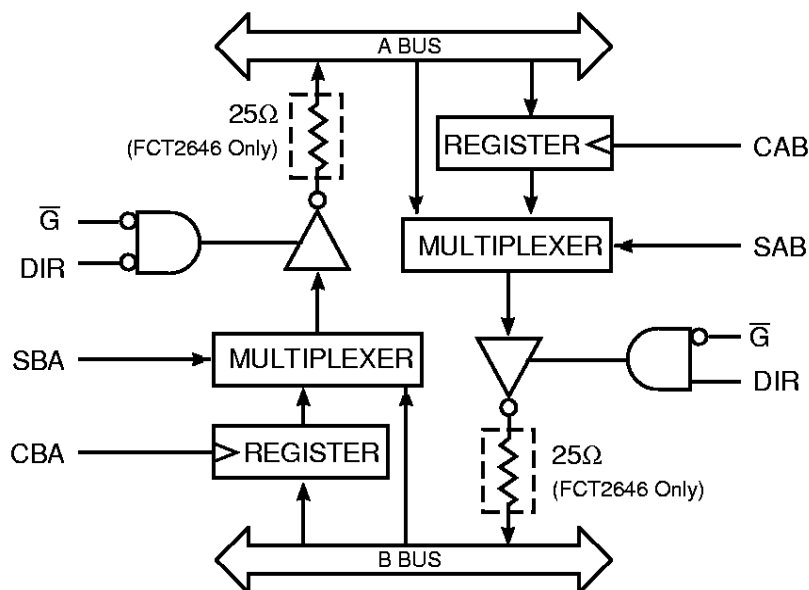


Figure 2. Pin Configurations (All Pins Top View)

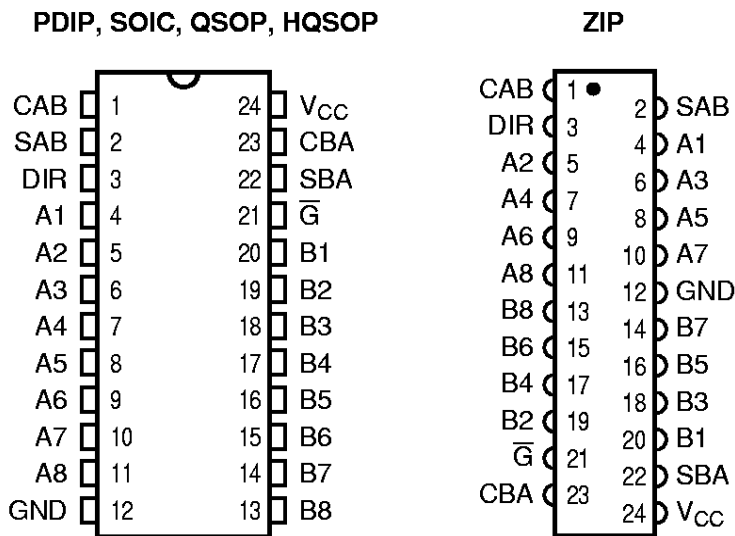


Table 1. Pin Description

Name	I/O	Description
A8-A1	I/O	A Bus
B8-B1	I/O	B Bus
CAB	I	Clock A to Register
CBA	I	Clock B to Register
SAB	I	A Bus or Reg to B
SBA	I	B Bus or Reg to A
DIR	I	Direction, A → B or B → A
$\bar{G}$	I	Output Enable

Table 2. Function Table

Inputs						Outputs		Function
$\bar{G}$	DIR	CAB	CBA	SAB	SBA	A8-A1	B8-B1	
H	—	—	—	—	—	Hi-Z	Hi-Z	Disabled
L	L	—	—	—	—	A	Hi-Z	Output A
L	H	—	—	—	—	Hi-Z	B	Output B
—	—	↑	—	—	—	—	—	Load A Register
—	—	—	↑	—	—	—	—	Load B Register
—	—	—	—	L	—	—	—	A Bus → B Bus
—	—	—	—	H	—	—	—	A Reg → B Bus
—	—	—	—	—	L	—	—	B Bus → A Bus
—	—	—	—	—	H	—	—	B Reg → A Bus

**Table 3. Absolute Maximum Ratings**

Supply Voltage to Ground.....	-0.5V to 7.0V
DC Output Voltage $V_{OUT}$ .....	-0.5V to 7.0V
DC Input Voltage $V_{IN}$ .....	-0.5V to 7.0V
AC Input Voltage (for a pulse width $\leq 20$ ns) .....	-3.0V
DC Input Diode Current with $V_{IN} < 0$ .....	-20mA
DC Output Diode Current with $V_{OUT} < 0$ .....	-50mA
DC Output Current Max. Sink Current/Pin .....	120mA
Maximum Power Dissipation.....	0.5 watts
$T_{STG}$ Storage Temperature.....	-65° to 150°C

**Note:** Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to QSI devices that result in functional or reliability type failures.

**Table 4. Capacitance<sup>(1)</sup>**

$T_A = 25^\circ\text{C}$ ,  $f = 1\text{MHz}$ ,  $V_{IN} = 0\text{V}$ ,  $V_{OUT} = 0\text{V}$

Pins <sup>(2)</sup>	SOIC	QSOP	PDIP	ZIP	Unit
1-11, 13-23	8	8	9	10	pF

**Notes:**

1. Capacitance is characterized but not tested.
2. Pin reference for 24-pin package.

**Table 5. Power Supply Characteristics**

Symbol	Parameter	Test Conditions <sup>(1)</sup>	Min	Max	Unit
$I_{CC}$	Quiescent Power Supply Current	$V_{CC} = \text{Max.}$ , freq = 0 $0\text{V} \leq V_{IN} \leq 0.2\text{V}$ or $V_{CC} - 0.2\text{V} \leq V_{IN} \leq V_{CC}$	—	1.5	mA
$\Delta I_{CC}$	Supply Current per Input @ TTL HIGH	$V_{CC} = \text{Max.}$ , $V_{IN} = 3.4\text{V}$ , freq = 0 <sup>(2)</sup>	—	2.0	mA
$Q_{CCD}$	Supply Current per Input per MHz	$V_{CC} = \text{Max.}$ , Outputs Open and Enabled One Bit Toggling @ 50% Duty Cycle Other Inputs at GND or $V_{CC}$ <sup>(3,4)</sup>	—	0.25	mA/ MHz

**Notes:**

1. For conditions shown as Min. or Max., use the appropriate values specified under DC specifications.
2. Per TTL driven input ( $V_{IN} = 3.4\text{V}$ ).
3. For flip-flops,  $Q_{CCD}$  is measured by switching one of the data input pins so that the output changes every clock cycle. This is a measurement of device power consumption only and does not include power to drive load capacitance or tester capacitance. This parameter is guaranteed by design but not tested.
4.  $I_C$  can be computed using the above parameters as explained in the Technical Overview section.

**QS54/74FCT646T, 2646T**

**Table 6. DC Electrical Characteristics Over Operating Range**

Industrial  $T_A = -40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ ,  $V_{CC} = 5.0\text{V} \pm 5\%$

Military  $T_A = -55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ ,  $V_{CC} = 5.0\text{V} \pm 10\%$

Symbol	Parameter	Test Conditions	Min	Typ <sup>(1)</sup>	Max	Unit
$V_{IH}$	Input HIGH Voltage	Logic HIGH for All Inputs	2.0	—	—	V
$V_{IL}$	Input LOW Voltage	Logic LOW for All Inputs	—	—	0.8	V
$\Delta V_T$	Input Hysteresis	$V_{TLH} - V_{THL}$ for All Inputs	—	0.2	—	V
$ I_{IH} $ $ I_{IL} $	Input Current Input HIGH or LOW	$V_{CC} = \text{Max.}, 0 \leq V_{IN} < V_{CC}$	—	—	5	$\mu\text{A}$
$ I_{OZ} $	Off-State Output Current (Hi-Z)	$V_{CC} = \text{Max.}, 0 \leq V_{IN} \leq V_{CC}$	—	—	5	$\mu\text{A}$
$I_{OS}$	Short Circuit Current (FCT646)	$V_{CC} = \text{Max.}, V_{OUT} = \text{GND}^{(2,3)}$	-60	—	—	mA
$I_{OR}$	Current Drive (FCT2646)	$V_{CC} = \text{Max.}, V_{OUT} = 2.0\text{V}^{(3)}$	50	—	—	mA
$V_{IC}$	Input Clamp Voltage	$V_{CC} = \text{Min.}, I_{IN} = -18\text{mA}, T_A = 25^{\circ}\text{C}^{(3)}$	—	-0.7	-1.2	V
$V_{OH}$	Output HIGH Voltage	$V_{CC} = \text{Min.}$ $I_{OH} = -12\text{mA}$ (MIL) $I_{OH} = -15\text{mA}$ (IND)	2.4 2.4	— —	— —	V
$V_{OL}$	Output LOW Voltage (FCT646)	$V_{CC} = \text{Min.}$ $I_{OL} = 48\text{mA}$ (MIL) $I_{OL} = 64\text{mA}$ (IND)	— —	— —	0.55 0.55	V
$V_{OL}$	Output LOW Voltage (FCT2646- 25 $\Omega$ )	$V_{CC} = \text{Min.}$ $I_{OL} = 12\text{mA}$ (MIL) $I_{OL} = 12\text{mA}$ (IND)	— —	— —	0.50 0.50	V
$R_{OUT}$	Output Resistance (FCT2646- 25 $\Omega$ )	$V_{CC} = \text{Min.}$ $I_{OL} = 12\text{mA}$ (MIL) $I_{OL} = 12\text{mA}$ (IND)	— 20	25 28	— 40	$\Omega$

**Notes:**

1. Typical values indicate  $V_{CC} = 5.0\text{V}$  and  $T_A = 25^{\circ}\text{C}$ .
2. Not more than one output should be shorted and the duration is  $\leq 1$  second.
3. These parameters are guaranteed by design but not tested.

## QS54/74FCT646T, 2646T

**Table 7. Switching Characteristics Over Operating Range**

Industrial  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$ ,  $V_{CC} = 5.0\text{V} \pm 5\%$

Military  $T_A = -55^\circ\text{C}$  to  $125^\circ\text{C}$ ,  $V_{CC} = 5.0\text{V} \pm 10\%$

$C_{LOAD} = 50\text{pF}$ ,  $R_{LOAD} = 500\Omega$  unless otherwise noted.

Symbol	Description <sup>(1)</sup>		646		646A 2646A		646C 2646C		646D		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	
$t_{PHLB}$	Bus to Bus	Ind	2.0	9.0	2.0	6.3	1.5	5.4	1.5	4.8	ns
$t_{PLHB}$	Delay, 646	Mil	2.0	11	2.0	7.7	1.5	6.0	—	—	
$t_{PHLB}$	Bus to Bus	Ind	2.0	9.0	2.0	6.3	1.5	5.4	1.5	4.8	ns
$t_{PLHB}$	Delay, 2646	Mil	2.0	11	2.0	7.7	1.5	6.0	—	—	
$t_{PZH}$	Output Enable	Ind	2.0	14	2.0	9.8	1.5	7.8	1.5	7.3	ns
$t_{PZL}$	Time, 646	Mil	2.0	15	2.0	10.5	1.5	8.9	—	—	
$t_{PZH}$	Output Enable	Ind	2.0	14	2.0	9.8	1.5	7.8	1.5	7.3	ns
$t_{PZL}$	Time, 2646	Mil	2.0	15	2.0	10.5	1.5	8.9	—	—	
$t_{PHZ}$	Output Disable	Ind <sup>(2)</sup>	2.0	9.0	2.0	6.3	1.5	6.3	1.5	6.3	ns
$t_{PLZ}$	Time	Mil <sup>(2)</sup>	2.0	11	2.0	7.7	1.5	7.7	—	—	
$t_{PHLC}$	Clock to Bus	Ind	2.0	9.0	2.0	6.3	1.5	5.7	1.5	5.2	ns
$t_{PLHC}$	Delay, 646	Mil	2.0	10	2.0	7.0	1.5	6.3	—	—	
$t_{PHLC}$	Clock to Bus	Ind	2.0	9.0	2.0	6.3	1.5	5.7	1.5	5.2	ns
$t_{PLHC}$	Delay, 2646	Mil	2.0	10	2.0	7.0	1.5	6.3	—	—	
$t_{PHLS}$	SBA/SAB to Bus	Ind	2.0	11	2.0	7.7	1.5	6.2	1.5	5.8	ns
$t_{PLHS}$	Delay, 646	Mil	2.0	12	2.0	8.4	1.5	7.0	—	—	
$t_{PHLS}$	SBA/SAB to Bus	Ind	2.0	11	2.0	7.7	1.5	6.2	1.5	5.8	ns
$t_{PLHS}$	Delay, 2646	Mil	2.0	12	2.0	8.4	1.5	7.0	—	—	
$t_S$	Data Setup Time	Ind	4.0	—	2.0	—	2.0	—	2.0	—	ns
		Mil	4.5	—	2.0	—	2.0	—	—	—	
$t_H$	Data Hold Time	Ind	2.0	—	1.5	—	1.5	—	1.5	—	ns
		Mil	2.0	—	1.5	—	1.5	—	—	—	
$t_{PWH}$	Clock Pulse Width	Ind <sup>(2)</sup>	6.0	—	5.0	—	5.0	—	5.0	—	ns
$t_{PWL}$	HIGH or LOW	Mil <sup>(2)</sup>	6.0	—	5.0	—	5.0	—	—	—	

**Notes:**

1. Minimums guaranteed but not tested for all parameters except  $t_S$  and  $t_H$ .
2. This parameter is guaranteed by design but not tested.
3. See Test Circuit and Waveforms.