

FEATURES/BENEFITS

- 5V tolerant inputs and outputs
- Industry standard pinouts
- Bus Hold feature holds last active state during 3-state operation
- 10 μ A I_{CCQ} quiescent power supply current
- Hot insertable
- 2.0V–3.6V V_{CC} supply operation
- \pm 24mA balanced output drive
- Meets or exceeds JEDEC Standard 36 specifications
- t_{PD} = 5.0ns
- Input hysteresis for noise immunity
- Multiple power and ground pins for low noise
- Operating temperature range: –40°C to 85°C
- Latch-up performance exceeds 500mA
- ESD performance:
 - Human body model > 2000V
 - Machine model > 200V
- Packages available:
 - 56-pin TSSOP
 - 56-pin SSOP

DESCRIPTION

The LCX16H646 is a 16-bit bus registered transceiver with three-state outputs that is ideal for driving address and data buses. The LCX16H646 is organized for transmission of data between A bus and B bus either directly or from the internal storage registers. The QS74LCX16H646 provides Bus Hold circuitry on the data inputs to retain the last active state during 3-state operation, eliminating the need for pull-up resistors. The 3.3V LCXPlus family features low power, low switching noise, and fast switching speeds for low power portable applications as well as high-end advanced workstation applications. 5V tolerant inputs and outputs allow this LCXPlus product to be used in mixed 5V and 3.3V applications. Easy board layout is facilitated by the use of flow-through pinouts and byte enable controls provide architectural flexibility for systems designers. To accommodate hot-plug or live insertion applications, this product is designed not to load an active bus when V_{CC} is removed.

Figure 1. Functional Block Diagram

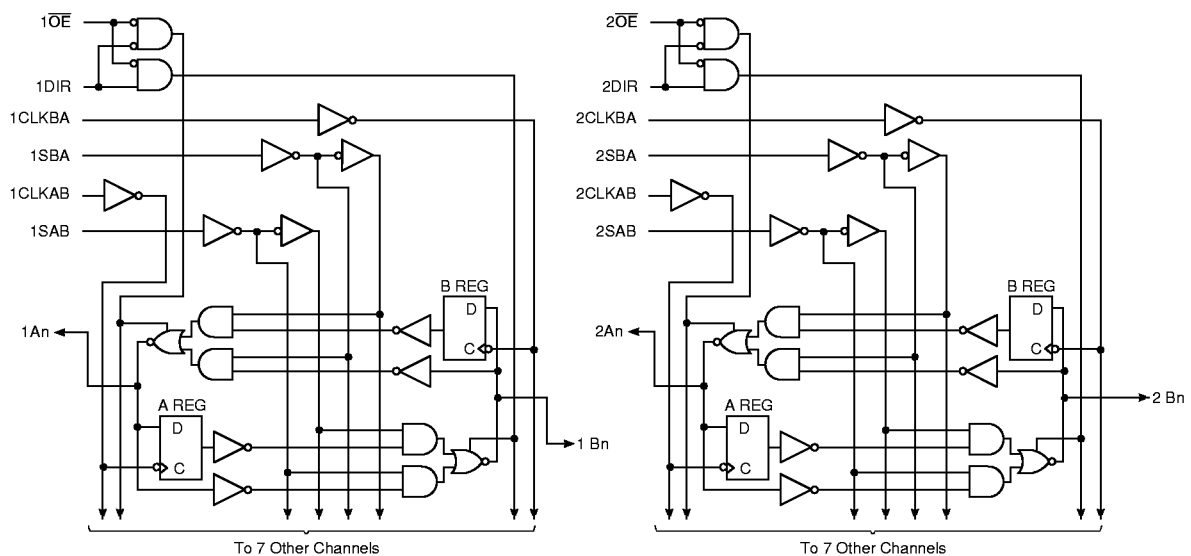


Figure 2. Pin Configuration
(All Pins Top View)
SSOP, TSSOP

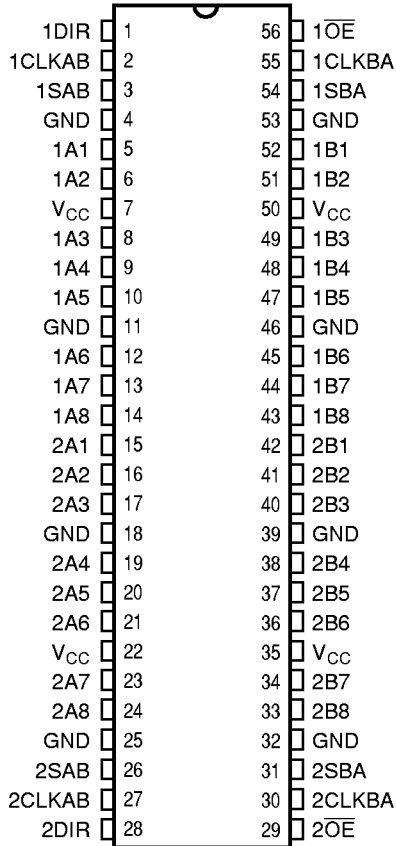


Table 1. Pin Description

Name	Description
xAx	Data Register A Inputs Data Register B Outputs (Bus Hold Inputs)
xBx	Data Register B Inputs Data Register A Outputs (Bus Hold Inputs)
xCLKAB, xCLKBA	Clock Inputs
xSAB, xSBA	Output Source Select Inputs
xDIR, xOE	Output Enable Inputs

Table 2. Function Table

Inputs						Data I/O ⁽¹⁾		Operation or Function
xOE	xDIR	xCLKAB	xCLKBA	xSAB	xSBA	xAx	xBx	
H	X	H or L	H or L	X	X	Input	Input	Isolation
H	X	↑	↑	X	X			Store A and B Data
L	L	X	X	X	L	Output	Input	Real Time B Data to A Bus
L	L	X	H or L	X	H			Stored B Data to A Bus
L	H	X	X	L	X	Input	Output	Real Time A Data to B Bus
L	H	H or L	X	H	X			Stored A Data to B Bus

Notes:

- The data output functions may be enabled or disabled by various signals at the xOE or xDIR inputs. Data input functions are always enabled, i.e. data at the bus pins will be stored on every LOW-to-HIGH transition on the clock inputs.
- H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
↑ = LOW-to-HIGH Transition

Table 3. Capacitance

Symbol	Pins	Typ	Unit	Conditions
C _{IN}	Input Capacitance	7.0	pF	V _{IN} = 0V, V _{OUT} = 0V, f = 1MHz
C _{I/O}	I/O Capacitance	8.0	pF	V _{IN} = 0V, V _{OUT} = 0V, f = 1MHz
C _{PD}	Power Dissipation Capacitance	25	pF	V _{CC} = 3.3V, V _{IN} = 0 or V _{CC} f = 10MHz

Note: Capacitance is characterized but not production tested.

Table 4. Absolute Maximum Ratings

Supply Voltage to Ground	-0.5V to 7.0V
DC Output Voltage V _{OUT}	
Outputs HIGH-Z	-0.5V to 7.0V
Outputs Active	-0.5V to V _{CC} + 0.5V
DC Input Voltage V _{IN}	-0.5V to 7.0V
DC Input Diode Current with V _{IN} < 0	-50mA
DC Output Diode Current	
V _O < 0	-50mA
V _O > V _{CC}	50mA
DC Output Source/Sink Current (I _{OH} /I _{OL})	±50mA
DC Supply Current per Supply Pin	±100mA
DC Ground Current per Ground Pin	±100mA
T _{STG} Storage Temperature	-65° to 150°C

Note: Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to this device resulting in functional or reliability type failures.

Table 5. Recommended Operating Conditions

Symbol	Parameter	Min	Max	Unit	
V _{CC}	Supply Voltage, Operating	2.0	3.6	V	
	Supply Voltage, Data Retention Only	1.5	3.6		
V _{IN}	Input Voltage	0	5.5	V	
V _{OUT}	Output Voltage in Active State	0	V _{CC}	V	
	Output Voltage in "OFF" State	0	5.5		
I _{OH} /I _{OL}	Output Current	V _{CC} = 3.0–3.6V	—	±24	mA
		V _{CC} = 2.7V	—	±12	
Δt/Δv	Input Transition Slew Rate	—	10	ns/V	
T _A	Operating Free Air Temperature	-40	85	°C	

Table 6. DC Electrical Characteristics Over Operating Range

Industrial Temperature Range, $T_A = -40^{\circ}\text{C}$ to 85°C

Symbol	Parameter	Test Conditions ⁽¹⁾	Min	Typ ⁽²⁾	Max	Unit
V_{IH}	Input HIGH Voltage	Logic HIGH for All Inputs	2.0	—	—	V
V_{IL}	Input LOW Voltage	Logic LOW for All Inputs	—	—	0.8	V
V_{OH}	Output HIGH Voltage	$V_{CC} = 2.7\text{V}, I_{OH} = -100\mu\text{A}$ $V_{CC} = 2.7\text{V}, I_{OH} = -12\text{mA}$ $V_{CC} = 3.0\text{V}, I_{OH} = -18\text{mA}$ $V_{CC} = 3.0\text{V}, I_{OH} = -24\text{mA}$	$V_{CC} - 0.2$ 2.2 2.4 2.2	— — — —	— — — —	V
V_{OL}	Output Low Voltage	$V_{CC} = 2.7\text{V}, I_{OL} = 100\mu\text{A}$ $V_{CC} = 2.7\text{V}, I_{OL} = 12\text{mA}$ $V_{CC} = 3.0\text{V}, I_{OL} = 16\text{mA}$ $V_{CC} = 3.0\text{V}, I_{OL} = 24\text{mA}$	— — — —	— — — —	0.2 0.4 0.4 0.5	V
ΔV_T	Input Hysteresis ⁽³⁾	$V_{TLH} - V_{THL}$ for All Inputs	—	150	—	mV
I_I	Input Leakage Current	$V_I = 0\text{V}, V_I = 5.5\text{V}, V_{CC} = 3.6\text{V}$	—	—	± 1.0	μA
$ I_{BH} $	Input Current Inputs High or Low Bus Hold Inputs ^(3,4)	$V_{CC} = 3.6\text{V}, V_{IN} = 0\text{V}$ or $V_{IN} = V_{CC}$	—	—	50	μA
		$V_{CC} = 3.6\text{V}, 0.8\text{V} < V_{IN} < 2.0\text{V}$	—	—	500 ⁽⁵⁾	μA
I_{BHH}	Bus Hold Sustaining Current	$V_{CC} = 3.0\text{V}$	$V_{IN} = 2.0\text{V}$	—	—	μA
I_{BHL}	Bus Hold Inputs			$V_{IN} = 0.8\text{V}$	75	—
I_{OZ}	High-Z I/O Leakage ⁽³⁾	$V_O = 0\text{V}, V_O = 5.5\text{V},$ $V_I = V_{IH}$ or $V_{IL}, V_{CC} = 3.6\text{V}$	—	—	± 1.0	μA
I_{OS}	Short Circuit Current ^(3,6)	$V_{CC} = 3.6\text{V}, V_O = \text{GND}$	-60	—	-200	mA
I_{OFF}	Power Off Leakage	$V_{CC} = 0\text{V}, V_I$ or $V_O = 5.5\text{V}$	—	—	10	μA
V_{IK}	Input Clamp Voltage	$V_{CC} = 2.7\text{V}, I_{IN} = -18\text{mA}$	—	-0.7	-1.2	V

Notes:

1. For conditions shown as Min. or Max. use appropriate value specified under Recommended Operating Conditions for the applicable device type.
2. Typical values are at $V_{CC} = 3.3\text{V}$ and $T_A = 25^{\circ}\text{C}$.
3. These parameters are guaranteed by characterization, but not production tested.
4. Pins with Bus Hold are identified in the Pin Description.
5. An external driver must provide at least $|I_{BH}|$ during transition to guarantee that the Bus Hold input will change state.
6. Not more than one output should be tested at one time. Duration of test should not exceed one second.

Table 7. Power Supply Characteristics

Symbol	Parameter	Test Conditions ⁽¹⁾	Typ ⁽²⁾	Max	Unit	
I_{CC}	Quiescent Power Supply Current	$V_{CC} = 3.6V$, Freq = 0 $V_{IN} = GND$ or V_{CC}	0.1	10	μA	
ΔI_{CC}	Supply Current per Input @ TTL HIGH	$V_{CC} = 3.6V$ $V_{IN} = V_{CC} - 0.6V^{(3)}$	Control Inputs	2.0	30	μA
			Bus Hold Inputs	—	500	μA
I_{CCD}	Supply Current per Input per MHz ⁽⁴⁾	$V_{CC} = 3.6V$, Outputs Open One Bit Toggling @ 50% Duty Cycle $xDIR = x\overline{OE} = GND$	$V_{IN} = V_{CC}$ $V_{IN} = GND$	65	100	$\mu A/$ MHZ
I_C	Total Power Supply Current ⁽⁶⁾	$V_{CC} = 3.6V$, Outputs Open One Bit Toggling @ 50% Duty Cycle $f = 5MHz$, $f_{CP} = 10MHz$ (xCLKBA) $xDIR = x\overline{OE} = GND$,	$V_{IN} = V_{CC} - 0.6V$ $V_{IN} = GND$	0.5 ⁽⁵⁾	1.0 ⁽⁵⁾	mA
		$V_{CC} = 3.6V$, Outputs Open Sixteen Bits Toggling @ 50% Duty Cycle $f = 2.5MHz$, $f_{CP} = 10MHz$ (xCLKBA) $xDIR = x\overline{OE} = GND$	$V_{IN} = V_{CC} - 0.6V$ $V_{IN} = GND$	2.7 ⁽⁵⁾	8.0 ⁽⁵⁾	mA

Notes:

- For conditions shown as Min. or Max., use the appropriate values specified under Recommended Operating Conditions for applicable device type.
- Typical values are at $V_{CC} = 3.3V$, 25°C ambient.
- Per TTL driven input. All other inputs at V_{CC} or GND.
- This parameter is not directly testable, but is derived for use in total power supply calculations.
- Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed by design but not tested.
- $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
 $I_C = I_{CCQ} + \Delta I_{CC} D_H N_T + I_{CCD} f N_O$
 I_{CCQ} = Quiescent Current (I_{CCL} , I_{CCH} , and I_{CCZ}).
 ΔI_{CC} = Power Supply Current for a TTL-High Input ($V_{IN} = V_{CC} - 0.6V$).
 D_H = Duty Cycle for TTL High Inputs.
 N_T = Number of TTL High Inputs.
 I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL).
 f = Average Switching Frequency per Output.
 N_O = Number of Outputs Switching.

Table 8. Dynamic Switching Characteristics⁽¹⁾

Symbol	Parameter	Conditions	V_{CC} (V)	$T_A = 25^\circ C$	
				Typical	Units
V_{OLP}	Quiet Output Dynamic Peak V_{OL}	$C_L = 50pF$, $V_{IH} = 3.3V$, $V_{IL} = 0V$	3.3	0.8	V
V_{OLV}	Quiet Output Dynamic Valley V_{OL}	$C_L = 50pF$, $V_{IH} = 3.3V$, $V_{IL} = 0V$	3.3	0.8	V

Note:

- Characterized but not production tested.

Table 9. Switching Characteristics Over Operating Range

Industrial Temperature Range, $T_A = -40^{\circ}\text{C}$ to 85°C .

$C_{\text{LOAD}} = 50\text{pF}$, $R_{\text{LOAD}} = 500\Omega$ unless otherwise noted.

Symbol	Description ⁽²⁾	$V_{\text{CC}} = 3.3 \pm 0.3\text{V}$		$V_{\text{CC}} = 2.7\text{V}^{(2)}$		Unit
		Min	Max	Min	Max	
f_{MAX}	Clock Pulse Frequency ⁽²⁾	170	—	—	—	MHz
t_{PHL} t_{PLH}	Propagation Delay Bus to Bus	2.0	5.0	2.0	6.0	ns
t_{PZH} t_{PZL}	Output Enable Time xDIR or xOE to Bus	2.0	7.5	2.0	8.5	ns
t_{PHZ} t_{PLZ}	Output Disable Time ⁽²⁾ xDIR or xOE to Bus	2.0	6.0	2.0	7.0	ns
t_{PHL} t_{PLH}	Propagation Delay Clock to Bus	2.0	6.0	2.0	7.0	ns
t_{PHL} t_{PLH}	Propagation Delay xSAB or xSBA to Bus	2.0	6.0	2.0	7.0	ns
t_{SU}	Setup Time HIGH or LOW Bus to Clock	2.5	—	2.5	—	ns
t_{H}	Hold Time HIGH or LOW Bus to Clock	1.5	—	1.5	—	ns
t_{W}	Clock Pulse Width ⁽²⁾ LOW or HIGH	3.0	—	3.0	—	ns
$t_{\text{SK(O)}}$	Output Skew ⁽³⁾	—	0.5	—	—	ns

Notes:

1. Minimums guaranteed but not tested on propagation delays. See Test Circuit and Waveforms.
2. Guaranteed by characterization
3. Skew between any two outputs of the same package switching in the same direction.
This parameter is guaranteed by characterization but not production tested.

TEST CIRCUIT AND WAVEFORMS

Figure 3. Test Circuit

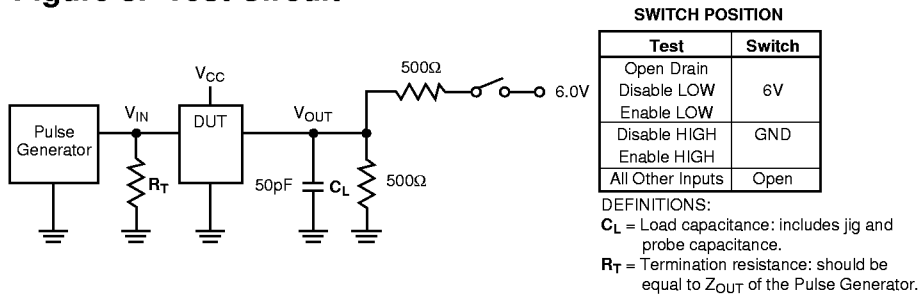


Figure 4. Setup, Hold, and Release Timing

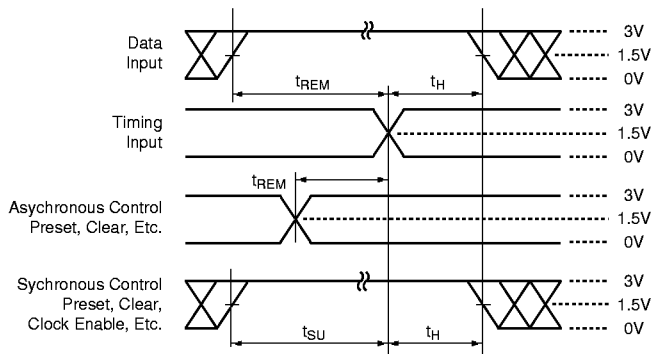


Figure 6. Pulse Width

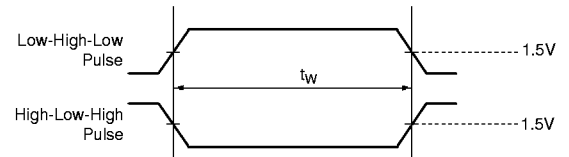


Figure 5. Enable and Disable Timing

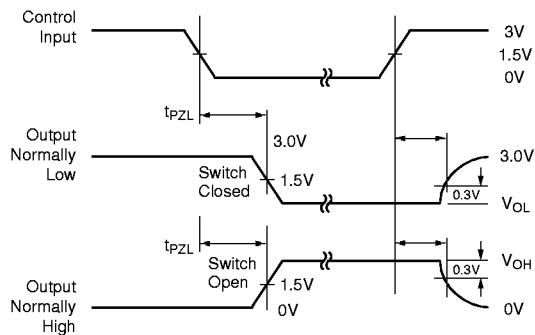
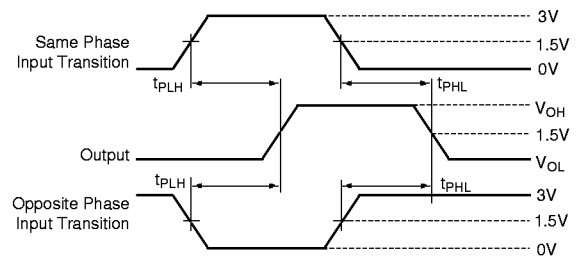


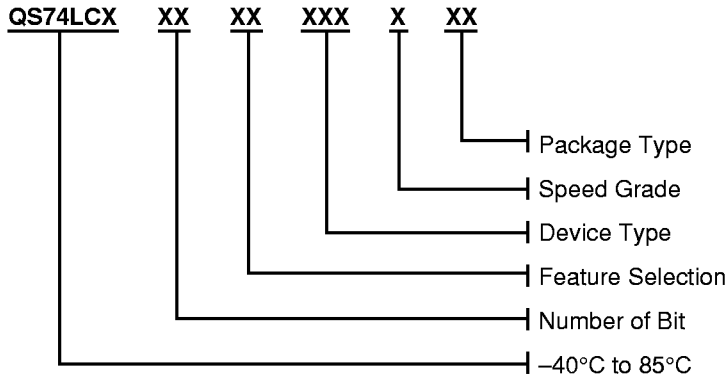
Figure 7. Propagation Delay



Notes:

1. Input Control Enable = LOW and Input Control Disable = HIGH.
2. Pulse Generator for All Pulses: Rate \leq 1.0MHz;
 $Z_{OUT} \leq 50\Omega$; $t_F, t_R \leq 2.5ns$.

ORDERING INFORMATION



Device Type:

646

Speed Grades:

Blank – Standard

Package Type:

PV – SSOP, 300 mil

PA – TSSOP, 240 mil

Feature Selection:

H – Bus Hold

Number of Bit:

16 – 16-Bit