High Speed CMOS Bus Interface 8-, 9-, and 10-Bit Latches

QS54/74FCT841T
QS54/74FCT843T
QS54/74FCT845T*

QS54/74FCT2841T
QS54/74FCT2843T*
QS54/74FCT2845T*

FEATURES/BENEFITS

- Pin and function compatible to the Am29841 /29843/29845 74FCT 841/843/845 and 74FCT841T/843T/845T
- CMOS power levels: <7.5 mW static
- Available in DIP, SOIC, QSOP, ZIP
- Undershoot Clamp diodes on all inputs
- TTL-compatible input and output levels
- Ground bounce controlled outputs
- Reduced output swing of 0-3.5V
- Military product compliant to MIL-STD-883

FCT-T 841T, 843T, 845T

- JEDEC-FCT spec compatible
- Fastest CMOS Logic family Available
- A, B, and C speed grades with 5.5 ns t_{PD} for C
- I_{OL} = 48 mA Com, 32 mA Mil

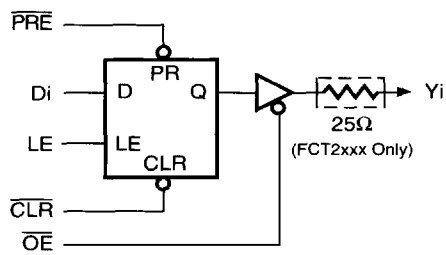
FCT-T 2841T, 2843T, 2845T

- Built-in 25Ω series resistor outputs reduce reflection and other system noise
- A, B, and C speed grades with 5.5 ns t_{PD} for C
- I_{OL} = 12 mA Com

DESCRIPTION

The QSFCT841T, 843T, and 845T are 10, 9, and 8-bit high-speed CMOS TTL-compatible buffered latches with three-state outputs that are ideal for driving high capacitance loads such as memory and address buses. The devices come in A, B, and C speed grades with 5.5 ns (Max.) t_{PLH}/t_{PLH} for the C grade. The 2841/3/5 devices are 25Ω resistor output versions useful for driving transmission lines and reducing system noise. The 284x eliminate the need for external series resistor in high speed systems and can replace the 84x series to reduce noise in an existing design. All inputs have clamp diodes for undershoot noise suppression. All outputs have ground bounce suppression see QSI Application Note AN-001), and outputs will not load an active bus when Vcc is removed from the device.

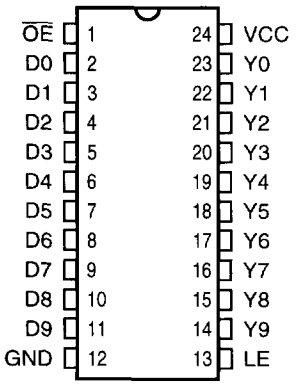
FUNCTIONAL BLOCK DIAGRAM



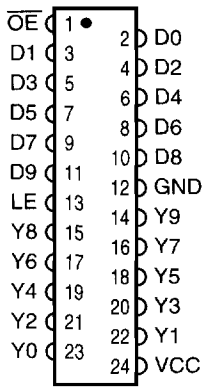
*Note: QS54/74FCT845T, 2843T, 2845T are not recommended for use in new designs

FCT841 PIN CONFIGURATIONS (All Pins Top View)

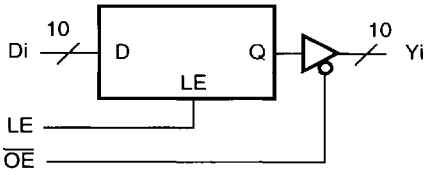
PDIP, SOIC, QSOP



ZIP



FCT841 LOGIC SYMBOL



PIN DESCRIPTION

Name	I/O	Description
Di	I	Data Inputs
Yi	O	Data Outputs - Three State
LE	I	Latch Enable
$\overline{OE}$	I	Output Enable

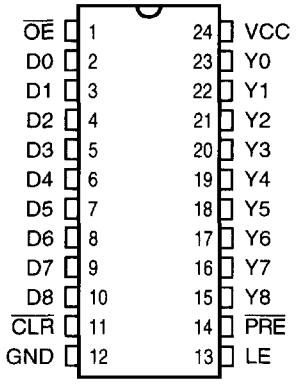
FUNCTION TABLES

QSFCT841, 2841

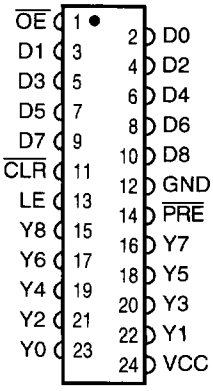
Inputs			Internal	Outputs	
$\overline{OE}$	LE	Di	Qi	Yi	Function
H	X	X	X	Z	Hi-Z
L	X	X	H	H	Output Enabled
L	X	X	L	L	Output Enabled
X	H	H	H	X	Transparent
X	H	L	L	X	Transparent
X	L	X	NC	X	Latched

FCT843 PIN CONFIGURATIONS (All Pins Top View)

PDIP, SOIC, QSOP



ZIP



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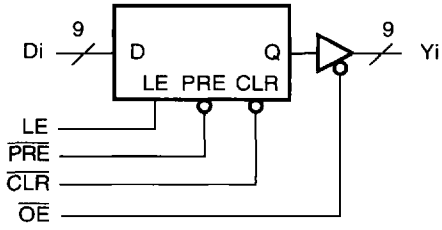
FCT843 LOGIC SYMBOL



PIN DESCRIPTION

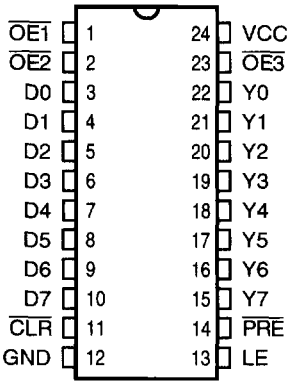
Name	I/O	Description
Di	I	Data Inputs
Yi	O	Data Outputs - Three State
$\overline{OE}$	I	Output Enable
LE	I	Latch Enable
$\overline{PRE}$	I	Preset
$\overline{CLR}$	I	Asynchronous Reset

FUNCTION TABLE
QSFCT843, 2843, 845, 2845

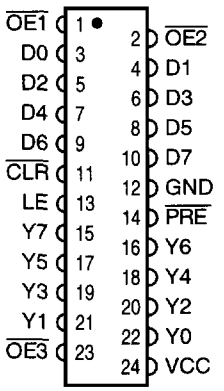
Inputs					Internal	Outputs	
$\overline{CLR}$	$\overline{PRE}$	$\overline{OE}$	LE	Di	Qi	Yi	Function
H	H	H	X	X	X	Z	Hi-Z
X	X	L	X	X	H	H	Output Enabled
X	X	L	X	X	L	L	Output Enabled
H	H	L	H	H	H	H	Transparent
H	H	L	H	L	L	L	Transparent
H	H	L	L	X	NC	NC	Latched
H	L	L	X	X	H	H	Preset
L	H	L	L	X	L	L	Clear
L	L	L	L	X	H	H	Preset

FCT845 PIN CONFIGURATIONS (All Pins Top View)

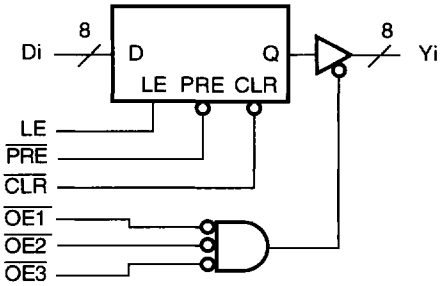
PDIP, SOIC, QSOP



ZIP



FCT845 LOGIC SYMBOL



PIN DESCRIPTION

Name	I/O	Description
Di	I	Data Inputs
Yi	O	Data Outputs - Three State
$\overline{OEi}$	I	Output Enable
LE	I	Latch Enable
$\overline{PRE}$	I	Preset
$\overline{CLR}$	I	Asynchronous Reset

ABSOLUTE MAXIMUM RATINGS

Supply Voltage to Ground	–0.5V to +7.0V
DC Output Voltage V_{OUT}	–0.5V to +7.0V
DC Input Voltage V_{IN}	–0.5V to +7.0V
AC Input Voltage (for a pulse width ≤ 20 ns)	–3.0V
DC Input Diode Current with V_{IN} < 0	–20 mA
DC Output Diode Current with V_{OUT} < 0	–50 mA
DC Output Current Max. Sink Current/Pin	120 mA
Maximum Power Dissipation	0.5 watts
T_{STG} Storage Temperature	–65° to +150°C

Note: Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to QSI devices that result in functional or reliability type failures.

CAPACITANCE

T_A = 25°C, f = 1 MHz, V_{IN} = 0V, V_{OUT} = 0V

Pins	SOIC	QSOP	PDIP	ZIP	Unit
1-11, 13, 14, 23	4	4	5	7	pF
15-22	6	6	7	9	pF

Note: Capacitance is characterized but not tested.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]	Min	Max	Unit
Icc	Quiescent Power Supply Current	Vcc = Max., freq = 0 0V ≤ V_{IN} ≤ 0.2V or Vcc-0.2V ≤ V_{IN} ≤ Vcc	—	1.5	mA
ΔIcc	Supply Current per Input @ TTL HIGH	Vcc = Max., V_{IN} = 3.4V, freq = 0[2]	—	2.0	mA
Q_{CCD}	Supply Current per Input per MHz	Vcc = Max., Outputs open and enabled One bit toggling @ 50% duty cycle Other inputs at GND or Vcc[3,4]	—	0.25	mA/ MHz

Notes:
1. For conditions shown as Min. or Max., use the appropriate values specified under DC specifications.
2. Per TTL driven input (V_{IN} = 3.4V).
3. For flip-flops, Q_{CCD} is measured by switching one of the data input pins so that the output changes every clock cycle. This is a measurement of device power consumption only and does not include power to drive load capacitance or tester capacitance. This parameter is guaranteed by design but not tested.
4. Ic can be computed using the above parameters as explained in the Technical Overview section.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Commercial T_A = 0°C to 70°C, V_{CC} = 5.0V ± 5% Military T_A = –55°C to 125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions	Min	Typ(1)	Max	Unit
V_{IH}	Input HIGH Voltage	Logic HIGH for All Inputs	2.0	—	—	V
V_{IL}	Input LOW Voltage	Logic LOW for All Inputs	—	—	0.8	V
ΔV_T	Input Hysteresis	$V_{TLH} - V_{THL}$ for All Inputs	—	0.2	—	V
$\lvert I_{IH} \rvert$ $\lvert I_{IL} \rvert$	Input Current Input HIGH or LOW	Vcc = Max., 0 ≤ V_{IN} < Vcc	—	—	5	µA
$\lvert I_{OZ} \rvert$	Off-State Output Current (Hi-Z)	Vcc = Max., 0 ≤ V_{IN} ≤ Vcc	—	—	5	µA
I_{OS}	Short Circuit Current (FCTXXX)	Vcc = Max., V_{OUT} = GND(2,3)	–60	—	—	mA
I_{OR}	Current Drive (FCT2XXX – 25Ω)	Vcc = Min., V_{OUT} = 2.0V(3)	50	—	—	mA
V_{IC}	Input Clamp Voltage	Vcc = Min., I_{IN} = –18 mA, T_A = 25°C(3)	—	–0.7	–1.2	V
V_{OH}	Output HIGH Voltage	Vcc = Min. I_{OH} = –12 mA (MIL) I_{OH} = –15 mA (COM)	2.4 2.4	— —	— —	V
V_{OL}	Output LOW Voltage (FCTXXX)	Vcc = Min. I_{OL} = 32 mA (MIL) I_{OL} = 48 mA (COM)	— —	— —	0.50 0.50	V
V_{OL}	Output LOW Voltage (FCT2XXX – 25Ω)	Vcc = Min. I_{OL} = 12 mA (MIL) I_{OL} = 12 mA (COM)	— —	— —	0.50 0.50	V
R_{OUT}	Output Resistance (FCT2XXX – 25Ω)	Vcc = Min. I_{OL} = 12 mA (MIL) I_{OL} = 12 mA (COM)	— 20	25 28	— 40	Ω

Notes:
1. Typical values indicate Vcc = 5.0V and T_A = 25°C.
2. Not more than one output should be shorted and the duration is ≤1 second.
3. These parameters are guaranteed by design but not tested.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Commercial T_A = 0°C to 70°C, Vcc = 5.0V ± 5% Military T_A = –55°C to 125°C, Vcc = 5.0V ± 10%
C_{LOAD} = 50 pF, R_{LOAD} = 500Ω unless otherwise noted.

Symbol	Description		841A 843A 845A 2841A 2843A 2845A Min	841A 843A 845A 2841A 2843A 2845A Max	841B 843B 845B 2841B 2843B 2845B Min	841B 843B 845B 2841B 2843B 2845B Max	841C 843C 845C 2841C 2843C 2845C Min	841C 843C 845C 2841C 2843C 2845C Max	Unit
t_{PHL}	Data to Y Delay	COM		9.0		6.5		5.5	ns
t_{PLH}	$\overline{OE}$ = LOW, 841/3/5	MIL		10		7.5		6.3	
t_{PHL}	Data to Y Delay[2,3]	COM		13		13		13	ns
t_{PLH}	$\overline{OE}$ = LOW, 841/3/5	MIL		15		15		15	
t_{PHL}	Data to Y Delay	COM		9.5		6.5		5.5	ns
t_{PLH}	$\overline{OE}$ = LOW, 2841/3/5	MIL		11		7.5		6.3	
t_{PHL}	Data to Y Delay[2,3]	COM		20		13		13	ns
t_{PLH}	$\overline{OE}$ = LOW, 2841/3/5	MIL		20		15		15	
t_S	Data to LE Setup	COM	2.5		2.5		2.5		ns
		MIL	2.5		2.5		2.5		
t_H	Data to LE Hold Time	COM	2.5		2.5		2.5		ns
		MIL	3.0		2.5		2.5		
t_{LEY}	LE to Y Delay	COM		12		8.0		6.4	ns
	$\overline{OE}$ = LOW, 841/3/5	MIL		13		10.5		6.8	
t_{LEY}	LE to Y Delay[2,3]	COM		16		15.5		15	ns
	$\overline{OE}$ = LOW, 841/3/5	MIL		20		18		16	
t_{LEY}	LE to Y Delay	COM		12		8		8	ns
	$\overline{OE}$ = LOW, 2841/3/5	MIL		13		10.5		10.5	
t_{LEY}	LE to Y Delay[2,3]	COM		16		15.5		15	ns
	$\overline{OE}$ = LOW, 2841/3/5	MIL		20		18		16	

Notes:
1. See Test Circuit and Waveforms.
2. This parameter is guaranteed by design but not tested.
3. C_{LOAD} = 300 pF.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Commercial T_A = 0°C to 70°C, Vcc = 5.0V ± 5% Military T_A = –55°C to 125°C, Vcc = 5.0V ± 10%
C_{LOAD} = 50 pF, R_{LOAD} = 500Ω unless otherwise noted.

Symbol	Description[1]		841A 843A 845A 2841A 2843A 2845A Min	841A 843A 845A 2841A 2843A 2845A Max	841B 843B 845B 2841B 2843B 2845B Min	841B 843B 845B 2841B 2843B 2845B Max	841C 843C 845C 2841C 2843C 2845C Min	841C 843C 845C 2841C 2843C 2845C Max	Unit
t_{SLEC}	$\overline{CLR}$ to LE Setup	COM	3		2.5		2.5		ns
		MIL	3		2.5		2.5		
t_{CLR}	$\overline{CLR}$, $\overline{PRE}$ to Y Delay, 843/5	COM		12		8		7	ns
t_{PRE}		MIL		14		10		9	
t_{CLR}	$\overline{CLR}$, $\overline{PRE}$ to Y Delay,	COM		12		8		7	ns
t_{PRE}	2843/5	MIL		14		10		9	
t_{CLRR}	$\overline{CLR}$, $\overline{PRE}$[2]	COM		14		8		8	ns
t_{PRER}	Recovery Time	MIL		17		10		9	
t_{LEH}	LE Pulse Width HIGH[2]	COM	6		4		4		ns
		MIL	6		4		4		
t_{PREL}	$\overline{PRE}$, $\overline{CLR}$[2]	COM	8		4		4		ns
	Pulse Width LOW	MIL	9		4		4		
t_{PZH}	Output Enable Time	COM		11.5		8		6.5	ns
t_{PZL}	$\overline{OE}$ to Yi, 841	MIL		13		8.5		8.5	
t_{PZH}	Output Enable Time[2,3]	COM		23		14		12	ns
t_{PZL}	$\overline{OE}$ to Yi, 841	MIL		25		15		13	
t_{PZH}	Output Enable Time	COM		11.5		8		6.5	ns
t_{PZL}	$\overline{OE}$ to Yi, 2841	MIL		13		8.5		8.5	
t_{PZH}	Output Enable Time[2,3]	COM		23		14		12	ns
t_{PZL}	$\overline{OE}$ to Yi, 2841	MIL		25		15		13	
t_{PHZ}	Output Disable Time[2,4]	COM		7		6		5.7	ns
t_{PLZ}	$\overline{OE}$ to Yi	MIL		9		6.5		6	
t_{PHZ}	Output Disable Time[2]	COM		8		7		6	ns
t_{PLZ}	$\overline{OE}$ to Yi	MIL		10		7.5		6.3	

Notes:
1. See Test Circuit and Waveforms.
2. This parameter is guaranteed by design but not tested.
3. C_{LOAD} = 300 pF.
4. C_{LOAD} = 5 pF.