

GD54/74HC259, GD54/74HCT259

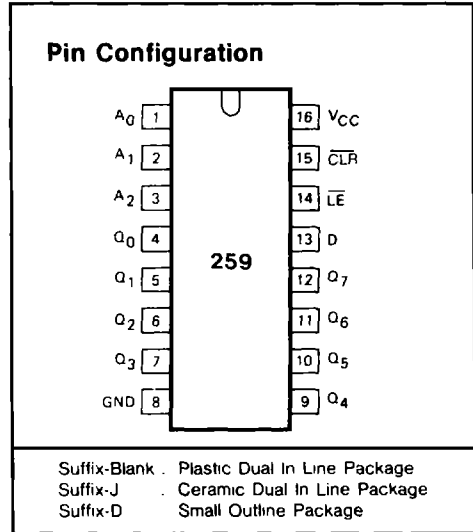
8-BIT ADDRESSABLE LATCH/3-TO-8 LINE DECODER

General Description

These devices are identical in pinout to the 54/74LS259. This 8-Bit Addressable latch can perform four basic functions in the addressable latch mode, data is read into the addressed stage of the latch. In the memory mode, the latch contents are stored regardless of any other inputs. In the 8-line decoder mode, data flows through to the addressed output. And in the clear mode, all stages are cleared to the low state. To eliminate the possibility of entering erroneous data into the latches, the enable should be held high (inactive) while the address lines are changing.

Features

- Low Power consumption characteristic of CMOS devices
- Output drive capability. 10 LS TTL Loads Min.
- Operating speed superior to LS TTL
- Wide operating voltage range. for HC 2 to 6 volts
for HCT 4.5 to 5.5 volts
- Low input current 1 μ A Max
- Low quiescent current. 80 μ A Max (74HC)
- High noise immunity characteristic of CMOS
- Diode protection on all inputs



Logic Diagram

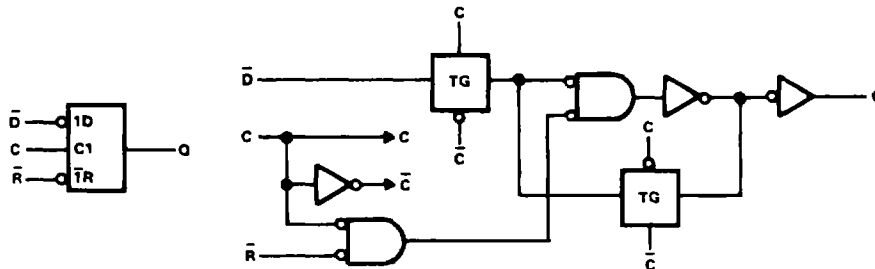


Fig. 1 Logic diagram (each latch)

Function Table

OPERATING MODES	INPUTS						OUTPUTS							
	CLR	LE	D	A ₀	A ₁	A ₂	Q ₀	Q ₁	Q ₂	Q ₃	Q ₄	Q ₅	Q ₆	Q ₇
master clear	L	H	X	X	X	X	L	L	L	L	L	L	L	L
demultiplex (active HIGH) decoder (when D = H)	L	L	d	L	L	L	Q=d	L	L	L	L	L	L	L
	L	L	d	H	L	L	L	Q=d	L	L	L	L	L	L
	L	L	d	L	H	L	L	L	L	L	L	L	L	L
	L	L	d	H	H	L	L	L	L	L	L	L	L	L
store (do nothing)	L	L	d	L	L	L	L	L	L	L	L	L	L	L
	L	L	d	H	L	L	L	L	L	L	L	L	L	L
	L	L	d	L	H	L	L	L	L	L	L	L	L	L
	L	L	d	H	H	L	L	L	L	L	L	L	L	L
addressable latch	H	H	X	X	X	X	q ₀	q ₁	q ₂	q ₃	q ₄	q ₅	q ₆	q ₇
	H	L	d	L	L	L	Q=d	q ₀	q ₁	q ₂	q ₃	q ₄	q ₅	q ₆
	H	L	d	L	L	L	Q=d	q ₀	q ₁	Q=d	q ₃	q ₄	q ₅	q ₆
	H	L	d	L	L	L	Q=d	q ₀	q ₁	q ₂	Q=d	q ₄	q ₅	q ₆
	H	L	d	L	L	H	q ₀	q ₁	q ₂	q ₃	Q=d	q ₅	q ₆	q ₇
	H	L	d	L	H	L	q ₀	q ₁	q ₂	q ₃	q ₄	Q=d	q ₆	q ₇
	H	L	d	L	H	H	q ₀	q ₁	q ₂	q ₃	q ₄	q ₅	Q=d	q ₇
	H	L	d	L	H	H	q ₀	q ₁	q ₂	q ₃	q ₄	q ₅	q ₆	Q=d

H = HIGH voltage level
 L = LOW voltage level
 X = don't care
 d = HIGH or LOW data one set-up time prior to the LOW-to-HIGH LE transition
 q = lower case letters indicate the state of the referenced output established during the last cycle in which it was addressed or cleared

Logic Diagram

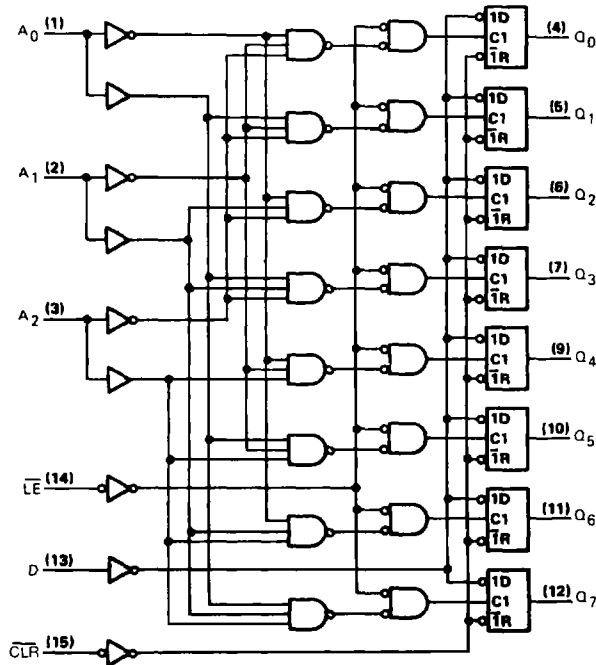


Fig. 2 Logic diagram

Absolute Maximum Ratings

SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	UNIT
V_{CC}	DC Supply voltage		-0.5	+7	V
I_{IK}, I_{OK}	DC input or output diode current	for $V_I < -0.5$ or $V_I > V_{CC} + 0.5V$		20	mA
I_O	DC output source or sink current	for $-0.5V < V_O < V_{CC} + 0.5V$		25	mA
I_{CC}	DC V_{CC} or GND current			50	mA
T_{sig}	Storage temperature range		-65	150	°C
P_D	Power dissipation per package	above +70°C derate linearly with 8mW/K		500	mW
T_L	Lead temperature	At distance 1/16 ± 1/32 in from case for 60 sec(CERAMIC) 10 sec(PLASTIC)		300 260	°C

Recommended Operating Conditions

CHARACTERISTIC	LIMITS		UNITS
	MIN	MAX	
Supply-Voltage Range V_{CC} : GD54/74HC Types GD54/74HCT Types	2 4.5	6 5.5	V
DC Input or Output Voltage V_I, V_O	0	V_{CC}	V
Operating Temperature T_A : GD74 Types GD54 Types	-40 -55	+85 +125	°C
Input Rise and Fall times t_r, t_f : GD54/74HC Types at 2V at 4.5V at 6V GD54/74HCT Types at 4.5V		1000 500 400 500	ns

DC Electrical Characteristics for HC

SYMBOL	PARAMETER	TEST CONDITION	V _{CC} (V)	T _A =25°C			GD74HC259		GD54HC259		UNIT	
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.		
V _{IH}	HIGH level input Voltage		2.0	1.5			1.5		1.5		V	
			4.5	3.15			3.15		3.15			
			6.0	4.2			4.2		4.2			
V _{IL}	LOW level input voltage		2.0			0.3		0.3		0.3	V	
			4.5			0.9		0.9		0.9		
			6.0			1.2		1.2		1.2		
V _{OH}	HIGH level output voltage	V _{IN} =V _{IH}	I _{OH} =-20μA	2.0	1.9	2.0		1.9		1.9	V	
				4.5	4.4	4.5		4.4		4.4		
		or V _{IL}	I _{OH} =-4mA	4.5	3.98	4.3		3.84		3.7		
				6.0	5.48	5.2		5.34		5.2		
V _{OL}	LOW level output voltage	V _{IN} =V _{IH}	I _{OL} =20μA	2.0			0.1		0.1		V	
				4.5			0.1		0.1			0.1
		or V _{IL}	I _{OL} =4mA	4.5		0.17	0.26		0.33			0.4
				6.0		0.15	0.26		0.33			0.4
I _{IN}	Input leakage Current	V _{IN} =V _{CC} or GND	6.0			0.1		1.0		1.0	μA	
I _{CC}	Quiescent Supply Current	V _{IN} =V _{CC} or GND I _{out} =0μA	6.0			8		80		160	μA	

DC Electrical Characteristics for HCT

SYMBOL	PARAMETER	TEST CONDITION	V _{CC} (V)	T _A =25°C			GD74HCT259		GD54HCT259		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
V _{IH}	HIGH level input Voltage		4.5								V
			to 5.5	2.0			2.0		2.0		
V _{IL}	LOW level input voltage		4.5								V
			to 5.5			0.8		0.8		0.8	
V _{OH}	HIGH level output voltage	V _{IN} =V _{IH}	I _{OH} =-20μA	4.5	4.4	4.5		4.4		4.4	V
				4.5	3.98	4.3		3.84		3.7	
V _{OL}	LOW level output voltage	V _{IN} =V _{IH}	I _{OL} =20μA	4.5			0.1		0.1		V
				4.5		0.17	0.26		0.33		
I _{IN}	Input leakage Current	V _{IN} =V _{CC} or GND	5.5			0.1		1.0		1.0	μA
			5.5			8		80		160	
I _{CC}	Quiescent Supply Current	V _{IN} =V _{CC} or GND I _{out} =0μA	5.5			8		80		160	μA

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Timing Requirements for HC: $t_r=t_f=6\text{ns}$ $C_L=50\text{ pF}$

SYMBOL	PARAMETER		V_{CC} (V)	$T_A=25^\circ\text{C}$			GD74HCT259		GD54HCT259		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_w	Pulse width	\overline{LE} , \overline{CLR} high or low	2.0	80	30		100		120		ns
			4.5	16	10		20		25		
			6.0	14	8		18		22		
t_{SU}	Setup time	Data after $LE\downarrow$	2.0	60	30		100		120		ns
			4.5	12	10		20		25		
			6.0	10	8		18		22		
t_h	Hold time	Data before $LE\downarrow$	2.0	3	0		3		3		ns
			4.5	3	0		3		3		
			6.0	3	0		3		3		

AC Characteristics for HC: $t_r=t_f=6\text{ns}$ $C_L=50\text{ pF}$

SYMBOL	PARAMETER		V_{CC} (V)	$T_A=25^\circ\text{C}$			GD74HCT259		GD54HCT259		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
$t_{PLH}/$ t_{PHL}	Propagation Delay Time D to Qn		2.0		50	160		210		260	ns
			4.5		18	35		42		50	
			6.0		17	30		38		46	
$t_{PLH}/$ t_{PHL}	Propagation Delay Time An to Qn		2.0		50	160		210		260	ns
			4.5		18	35		42		50	
			6.0		17	30		38		46	
$t_{PLH}/$ t_{PHL}	Propagation Delay Time \overline{LE} to Qn		2.0		48	150		200		250	ns
			4.5		17	33		40		48	
			6.0		16	28		36		42	
t_{PHL}	Propagation Delay Time \overline{CLR} to Qn		2.0		48	150		200		250	ns
			4.5		17	32		40		48	
			6.0		16	28		36		42	
$t_{TLH}/$ t_{THL}	Output Transition Time		2.0		25	70		85		100	ns
			4.5		8	15		18		22	
			6.0		7	13		16		19	

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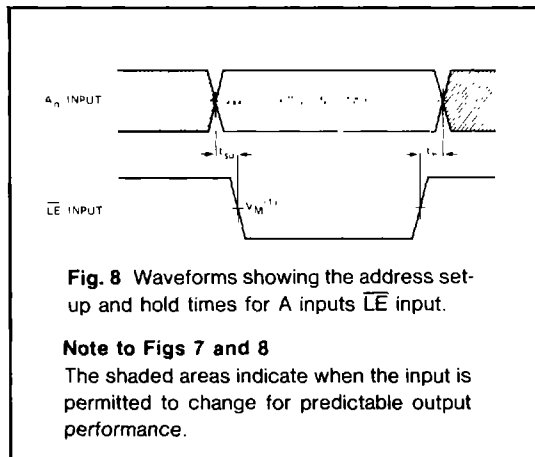
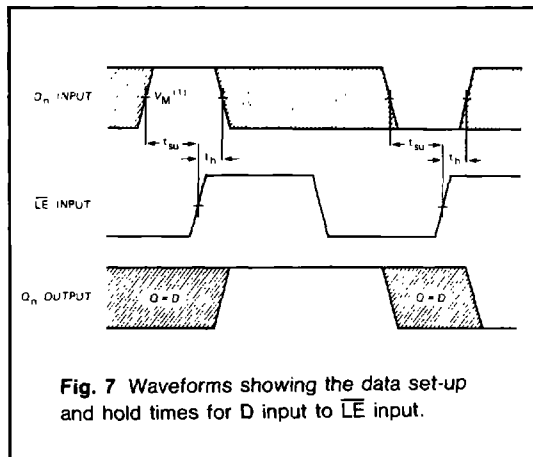
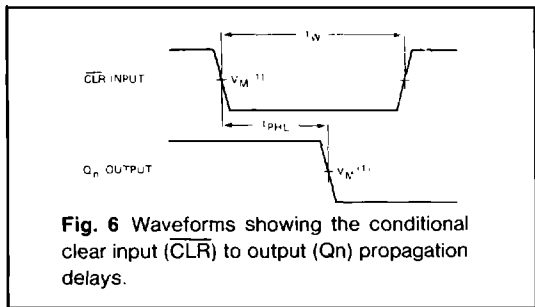
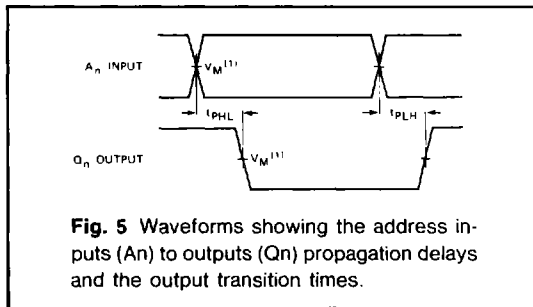
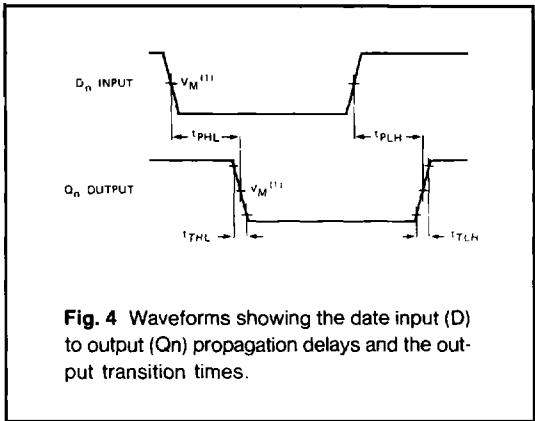
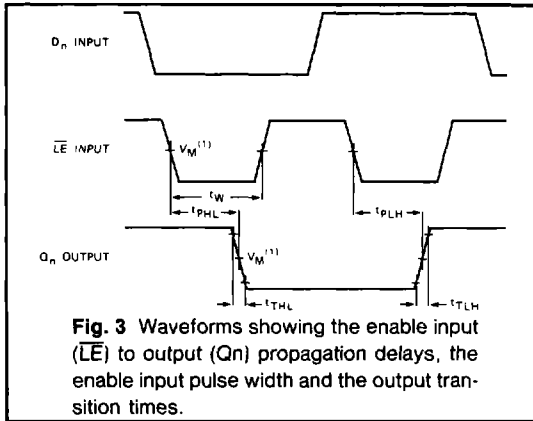
Timing Requirements for HCT : $t_r=t_f=6\text{ns}$ $C_L=50\text{ pF}$

SYMBOL	PARAMETER		V_{CC} (V)	$T_A=25^\circ\text{C}$			GD74HCT259		GD54HCT259		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_w	Pulse width	\overline{LE} , \overline{CLR} high or low	4.5	16	10		20		25		ns
t_{su}	Setup time	Data after $\overline{LE} \downarrow$	4.5	12	10		20		25		ns
t_h	Hold time	Data before $\overline{LE} \downarrow$	4.5	3	0		3		3		ns

AC Characteristics for HCT: $t_r=t_f=6\text{ns}$ $C_L=50\text{ pF}$

SYMBOL	PARAMETER		V_{CC} (V)	$T_A=25^\circ\text{C}$			GD74HCT259		GD54HCT259		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation Delay Time D to Qn		4.5		20	38		46		55	ns
t_{PLH}' t_{PHL}	Propagation Delay Time An to Qn		4.5		20	38		46		55	ns
t_{PLH}' t_{PHL}	Propagation Delay Time \overline{LE} to Qn		4.5		19	36		44		52	ns
t_{PHL}	Propagation Delay Time \overline{CLR} to Qn		4.5		19	36		44		52	ns
t_{TLH}' t_{THL}	Output Transition Time		4.5		8	15		18		22	ns

AC Waveforms



Note to AC waveforms

- (1) HC : $V_M = 50\%$, $V_I = \text{GND to } V_{CC}$
- HCT : $V_M = 1.3V$, $V_I = \text{GND to } 3V$.