LOW POWER SCHOTTKY INTEGRATED CIRCUITS

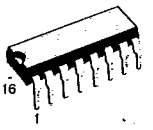
T54LS173A
T74LS173A

PRELIMINARY DATA

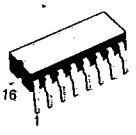
4-BIT D-TYPE REGISTER WITH 3-STATE OUTPUTS

DESCRIPTION

The T54LS173A/T74LS173A is a 4-Bit D-Type Register with 3-State outputs. The clock being fully edge-triggered allows either a load from the D inputs or a hold (retain register contents) depending on the state of the Input Enable Lines ($\overline{IE}_1$, $\overline{IE}_2$). HIGH on either Output Enable line ($\overline{OE}_1$, $\overline{OE}_2$) leads the output to a high impedence state without affecting the actual register contents. A HIGH on the Master Reset (MR) input resets the Register on a spite of the state of the clock (CP), the Output Enable ($\overline{OE}_1$, $\overline{OE}_2$) or the Input Enable ($\overline{IE}_1$, $\overline{IE}_2$) lines.



B1
Plastic Package



D1/D2
Ceramic Package

M1
Micro Package

C1
Plastic Chip Carrier

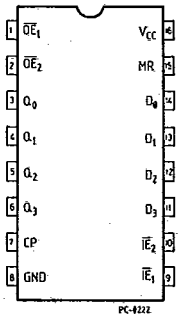
ORDERING NUMBERS:

T54LS173A D2
T74LS173A D1
T74LS173A B1
T74LS173A C1
T74LS173A M1

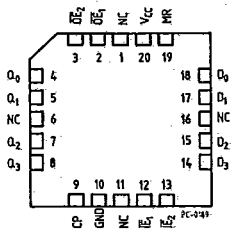
- 3-STATE OUTPUTS
- FULLY EDGE-TRIGGERED
- GATED INPUT AND OUTPUT ENABLES
- INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS

PIN CONNECTION
(top view)

DUAL IN LINE



CHIP CARRIER



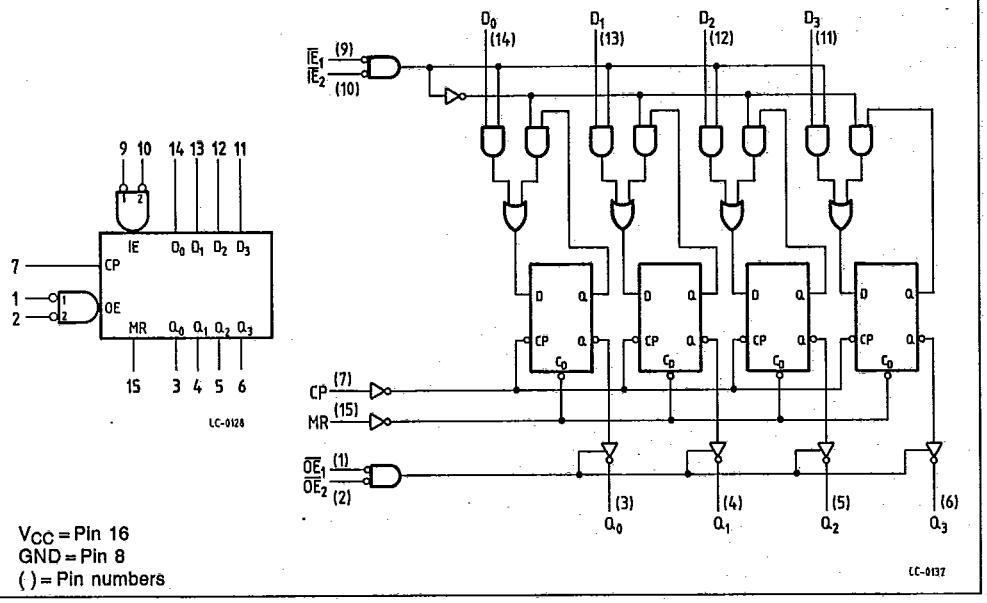
NC = No Internal Connection

PIN NAMES

D_0-D_3	Data Inputs
$\overline{IE}_1$, $\overline{IE}_2$	Input Enable (Active LOW)
($\overline{OE}_1$, $\overline{OE}_2$)	Output Enable (Active LOW) Inputs
CP	Clock Inputs (Active HIGH Going Edge) Inputs
MR	Master Reset Input (Active HIGH)
Q_0-Q_3	Outputs

T54LS173A
T74LS173A

LOGIC SYMBOL AND LOGIC DIAGRAM



V_{CC} = Pin 16
GND = Pin 8
( ) = Pin numbers

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	−0.5 to 7	V
V_I	Input Voltage, Applied to Input	−0.5 to 15	V
V_O	Output Voltage, Applied to Output	0 to 10	V
I_I	Input Current, Into Inputs	−30 to 5	mA
I_O	Output Current, Into Outputs	50	mA

Stresses in excess of those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

GUARANTEED OPERATING RANGES

Part Numbers	Supply Voltage			Temperature
	Min	Typ	Max	
T54LS173AD2	4.5 V	5.0 V	5.5 V	−55°C to +125°C
T74LS173AXX	4.75 V	5.0 V	5.25 V	0°C to +70°C

XX = package type.

T54LS173A
T74LS173A

TRUTH TABLE

MR	CP	$\overline{IE}_1$	$\overline{IE}_2$	D_n	Q_n
H	X	X	X	X	L
L	L	X	X	X	Q_n
L	I	H	X	X	Q_n
L	I	X	H	X	Q_n
L	I	L	L	L	L
L	I	L	L	H	H

When either $\overline{OE}_1$ or $\overline{OE}_2$ are HIGH, the output is in the off state (High Impedance); however this does not affect the contents or sequential operation of the register.

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Symbol	Parameter		Limits Min.	Limits Typ.	Limits Max.	Test Conditions (Note 1)	Units
V_{IH}	Input HIGH Voltage		2.0			Guaranteed Input HIGH Voltage for all Inputs	V
V_{IL}	Input LOW Voltage	54			0.7	Guaranteed Input LOW Voltage for all Inputs	V
		74			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V_{CC} = MIN, I_{IN} = −18mA	V
V_{OH}	Output HIGH Voltage	54	2.4	3.4		V_{CC} = MIN, I_{OH} = −400μA, V_{IN} = V_{IH} or V_{IL} per Truth Table	V
		74	2.4	3.1			
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	I_{OL} = 12mA; V_{CC} = MIN, V_{IN} = V_{IL} or V_{IH} per Truth Table	V
		74		0.35	0.5	I_{OL} = 24mA	
I_{OZH}	Output Off Current HIGH				20	V_{CC} = MAX, V_O = 2.4V	μA
I_{OZL}	Output Off Current LOW				−20	V_{CC} = MAX, V_0 = 0.4V	μA
I_{IH}	Input HIGH Current				20 0.1	V_{CC} = MAX, V_{IN} = 2.7V V_{CC} = MAX, V_{IN} = 7.0V	μA mA
I_{IL}	Input LOW Current				−0.4	V_{CC} = MAX, V_{IN} = 0.4V	mA
I_{OS}	Output Short Circuit Current (Note 2)		−30		−130	V_{CC} = MAX	mA
I_{CC}	Power Supply Current				30	V_{CC} = MAX	mA

Notes:
1) For conditions shown as MIN or MAX, use the appropriate value specified under guaranteed operating ranges.
2) Not more than one output should be shorted at a time.
3) Typical values are at V_{CC} = 5.0V, T_A = 25°C

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AC CHARACTERISTICS: $T_A = 25°C$

Symbol	Parameter	Limits			Test Conditions	Units
		Min.	Typ.	Max.		
f_{MAX}	Maximum Clock Frequency	30	50		$V_{CC} = 5.0V$ $C_L = 45pF$ $R_L = 667\Omega$	MHz
t_{PLH} t_{PHL}	Propagation Delay, Clock to Output		17 22	25 30		ns
t_{PHL}	Propagation Delay, MR to Output		26	35		ns
t_{PZH} t_{PZL}	Output Enable Time		15 18	23 27		ns
t_{PLZ} t_{PHZ}	Output Disable Time		11 11	17 17	$C_L = 5.0pF$	ns

AC SET-UP REQUIREMENTS: $T_A = 25°C$

Symbol	Parameter	Limits			Test Conditions	Units
		Min.	Typ.	Max.		
t_W	Clock or MR Pulse Width	20			$V_{CC} = 5.0V$	ns
t_s	Data Enable Set-up Time	35				ns
t_s	Data Set-up Time	17				ns
t_h	Hold Time, Any Input	0				ns
t_{rec}	Recovery Time	10				ns

AC WAVEFORMS

Fig. 1

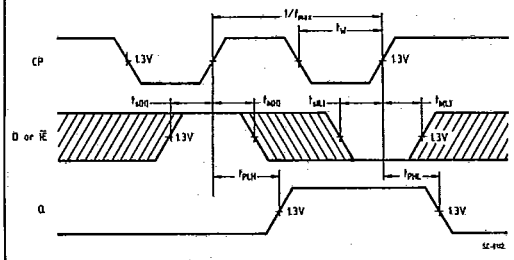


Fig. 2

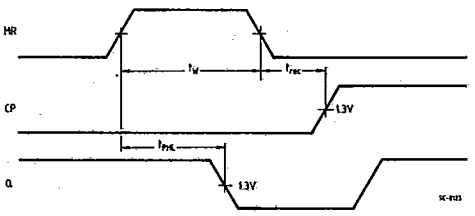


Fig. 3

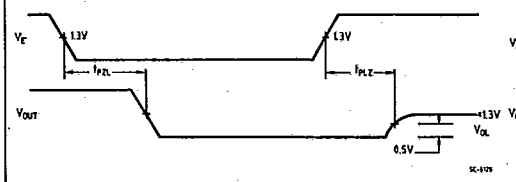
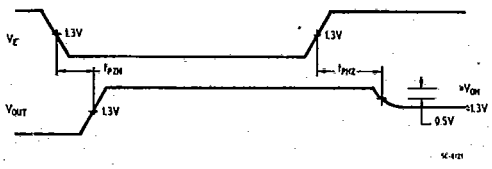
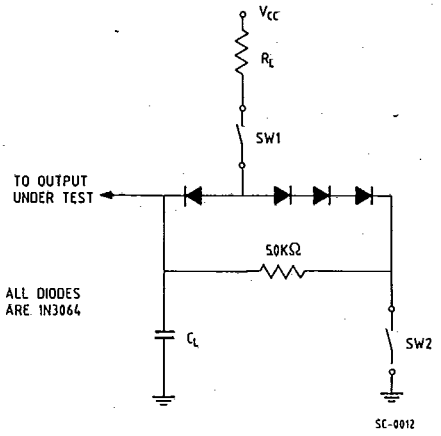


Fig. 4



AC LOAD CIRCUIT

Fig. 5

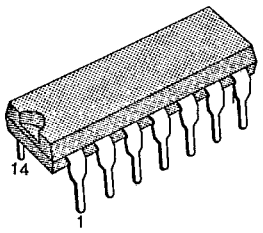


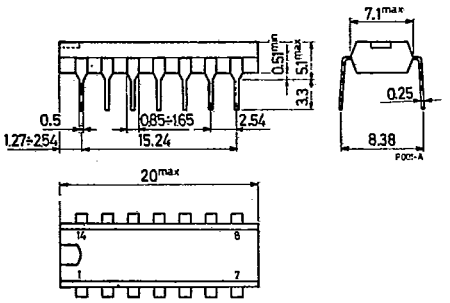
SWITCH POSITION

Symbol	SW1	SW2
t_{PZH}	Open	Closed
t_{PZL}	Closed	Open
t_{PLZ}	Closed	Closed
t_{PHZ}	Closed	Closed

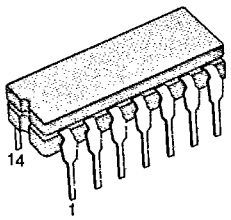
Packages

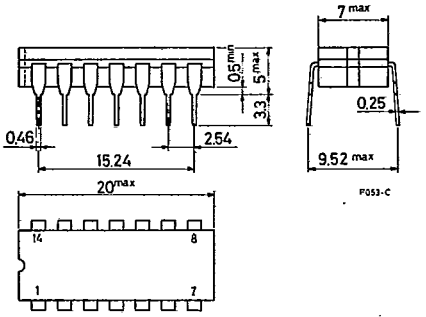
14-LEAD PLASTIC DIP



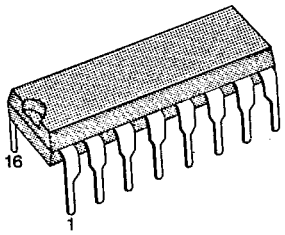


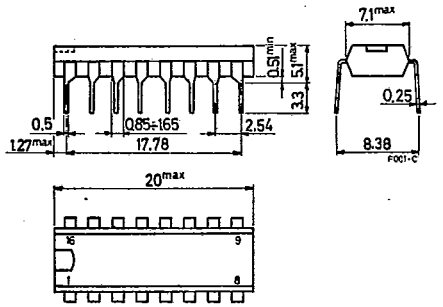
14-LEAD CERAMIC DIP





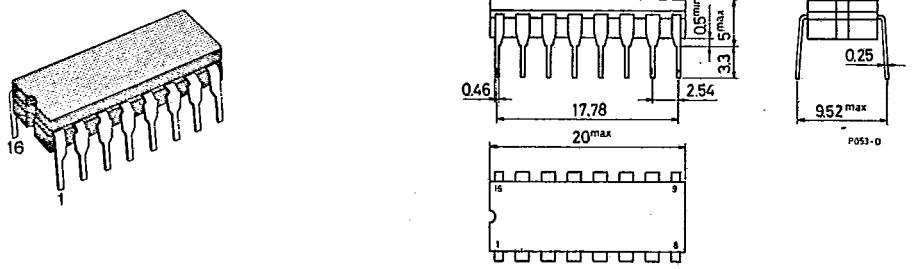
16-LEAD PLASTIC DIP





Packages

16-LEAD CERAMIC DIP



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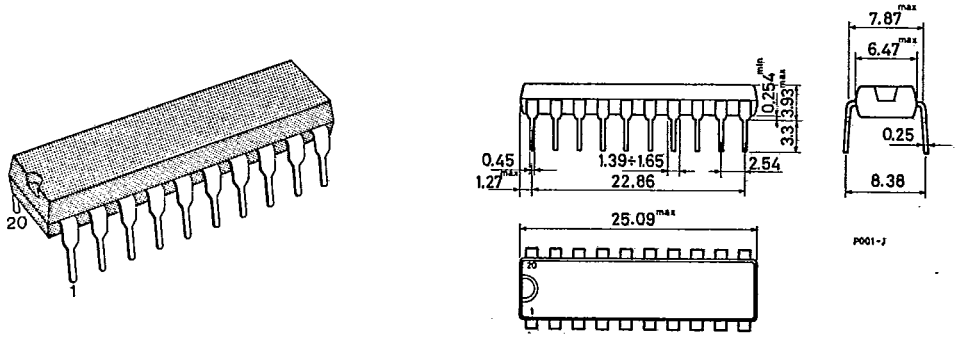

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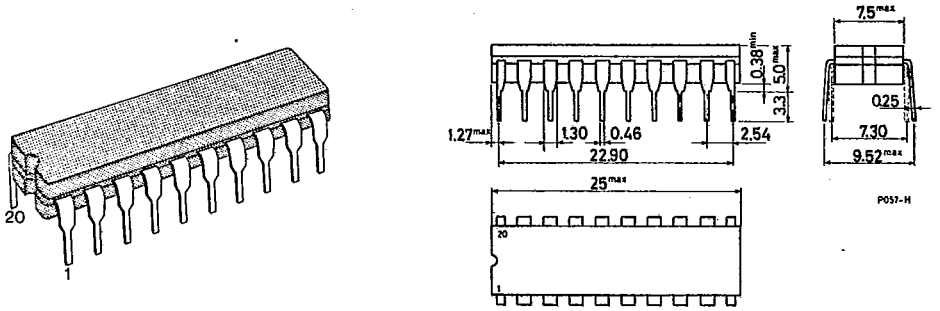
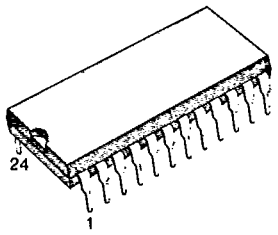
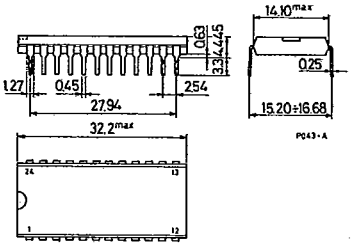


Packages

24-LEAD PLASTIC DIP





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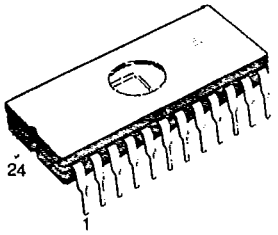
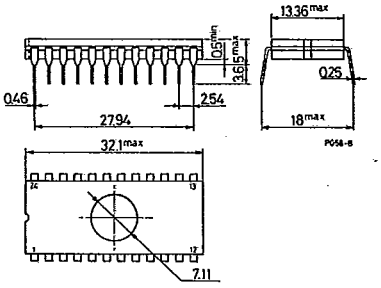
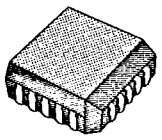
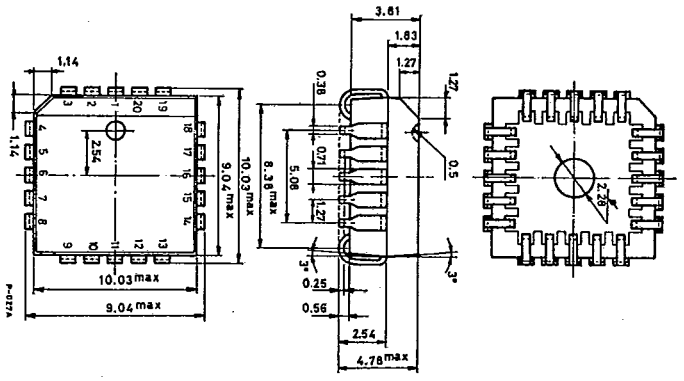




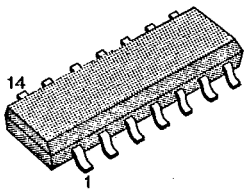
CHIP CARRIER 20 LEAD PLASTIC

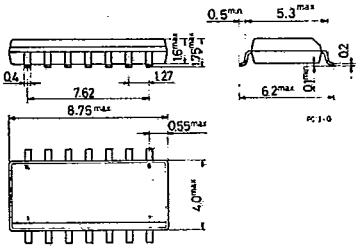




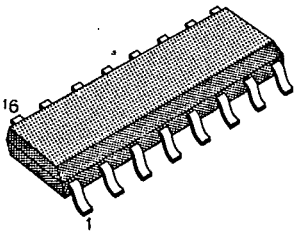
Packages

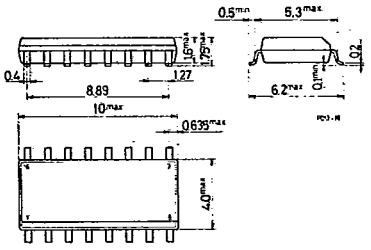
14-LEAD PLASTIC DIP MICROPACKAGE





16-LEAD PLASTIC DIP MICROPACKAGE





NOTE: FOR 20-LEAD PLASTIC DIP MICROPACKAGE CONTACT SGS

Surface Mounted

One possible solution to the important problem of PWB minimization, is that of using surface mounted components. Integrated circuits in SO (Small Outline) packages are made up of standard chips mounted in very small plastic packages.
The advantages given by using these devices are:

PWB Reduction

This is by far the most important advantage since the reduction of PWB size varies from 40 to 60% in comparison with standard board types. (See page 584 for package dimensions.)

Assembly Cost Reduction

SO Devices require no preliminary operation prior to mounting and can therefore be easily utilized in fully automatic equipment.

Increasing Reliability

The following characteristics lead to a higher level of reliability with respect to their standard packaged counter parts:

- The mounting system is fully automatic
- PWB number and the interconnections between them are reduced when the same number of devices are used.
- The high density of components on the board makes it thermally much more stable.

Noise Reduction and Improved Frequency Response

The reduction of the length of the connecting wires between the leads and the silicon guarantees a more homogeneous propogation delay between the external pins, with respect to the standard type.

Assembly Without Board Holes

The devices are placed on the board and soldered. This technology permits a higher level of tolerance in the positioning (automatic) of the device. For the standard DIP types this must be done with great accuracy due to the insertion of the leads into their holes.