Dual J-K Flip-Flop with Clear

The TC74HC73A is a high speed CMOS DUAL J-K FLIP-FLOP fabricated with silicon gate C^2MOS technology.

It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

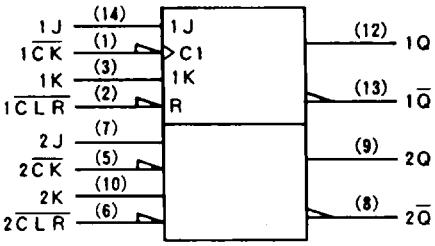
Depending on the logic levels applied to J and K input, this device changes state on the negative going transition of the clock input pulse ($\overline{CK}$).

The clear function is accomplished independently of the clock condition when the clear input ($\overline{CLR}$) is taken low,

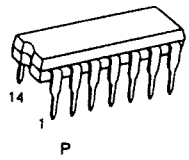
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

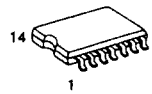
Features

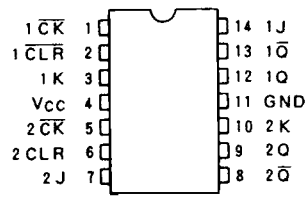
- High Speed: f_{MAX} = 55MHz(Typ.) at V_{CC} = 5V
- Low Power Dissipation: I_{CC} = 2μA(Max.) at Ta = 25°C
- High Noise Immunity: $V_{NIH} = V_{NIL}$ = 28%V_{CC}(Min.)
- Output Drive Capability: 10 LSTTL Loads
- Symmetrical Output Impedance: $|I_{OH}| = I_{OL}$ = 4mA(Min.)
- Balanced Propagation Delays: $t_{pLH} = t_{pHL}$
- Wide Operating Voltage Range: V_{CC}(opr) = 2V ~ 6V
- Pin and Function Compatible with 74LS73



IEC Logic Symbol







(Top View)

Pin Assignment

Truth Table

Inputs				Outputs		Function
$\overline{CLR}$	J	K	$\overline{CK}$	Q	$\overline{Q}$	
L	X	X	X	L	H	Clear
H	L	L	↓	Qn	$\overline{Qn}$	No Change
H	L	H	↓	L	H	–
H	H	L	↓	H	L	–
H	H	H	↓	$\overline{Qn}$	Qn	Toggle
H	X	X	↑	Qn	$\overline{Qn}$	No Change

X: Don't Care

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Supply Voltage Range	V_{CC}	-0.5 ~ 7	V
DC Input Voltage	V_{IN}	-0.5 ~ V_{CC} + 0.5	V
DC Output Voltage	V_{OUT}	-0.5 ~ V_{CC} + 0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)*/180(MFP)	mW
Storage Temperature	T_{stg}	-65 ~ 150	°C
Lead Temperature 10sec	T_L	300	°C

*500mW in the range of Ta = -40°C ~ 65°C. From Ta = 65°C to 85°C a derating factor of -10mW/°C shall be applied until 300mW.

Recommended Operating Conditions

Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC}	2 ~ 6	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	-40 ~ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ~ 1000(V_{CC} = 2.0V) 0 ~ 500(V_{CC} = 4.5V) 0 ~ 400(V_{CC} = 6.0V)	ns

DC Electrical Characteristics

Parameter	Symbol	Test Condition		Ta = 25°C				Ta = -40 ~ 85°C		Unit
				V_{CC}	Min	Typ.	Max.	Min.	Max.	
High-Level Input Voltage	V_{IH}	–		2.0 4.5 6.0	1.5 3.15 4.2	– – –	– – –	1.5 3.15 4.2	– – –	V
Low-Level Input Voltage	V_{IL}	–		2.0 4.5 6.0	– – –	– – –	0.5 1.35 1.8	– – –	0.5 1.35 1.8	V
High-Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} = -20μA	2.0 4.5 6.0	1.9 4.4 5.9	2.0 4.5 6.0	– – –	1.9 4.4 5.9	– – –	V
			I_{OH} = -4 mA I_{OH} = -5.2mA	4.5 6.0	4.18 5.68	4.31 5.80	– –	4.13 5.63	– –	
Low-Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 20μA	2.0 4.5 6.0	– – –	0.0 0.0 0.0	0.1 0.1 0.1	– – –	0.1 0.1 0.1	V
			I_{OL} = 4 mA I_{OL} = 5.2mA	4.5 6.0	– –	0.17 0.18	0.26 0.26	– –	0.33 0.33	
Input Leakage Current	I_{IN}	V_{IN} = V_{CC} or GND		6.0	–	–	±0.1	–	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		6.0	–	–	2.0	–	20.0	

Timing Requirements (Input $t_r = t_f = 6ns$)

Parameter	Symbol	Test Condition		Ta = 25°C		Ta = -40 ~ 85°C	Unit
			V_{CC}	Typ.	Limit	Limit	
Minimum Pulse Width (CLOCK)	$t_{W(L)}$ $t_{W(H)}$	–	2.0	–	75	95	ns
			4.5	–	15	19	
			6.0	–	13	16	
Minimum Pulse Width ($\overline{CLR}$)	$t_{W(L)}$	–	2.0	–	75	95	
			4.5	–	15	19	
			6.0	–	13	16	
Minimum Set-up Time	t_s	–	2.0	–	75	95	
			4.5	–	15	19	
			6.0	–	13	16	
Minimum Hold Time	t_h	–	2.0	–	0	0	
			4.5	–	0	0	
			6.0	–	0	0	
Minimum Removal Time ($\overline{CLR}$)	t_{rem}	–	2.0	–	75	95	
			4.5	–	15	19	
			6.0	–	13	16	
Clock Frequency	f	–	2.0	–	6	5	MHz
			4.5	–	30	24	
			6.0	–	35	28	

AC Electrical Characteristics ($C_L = 15pF$, $V_{CC} = 5V$, Ta = 25°C)

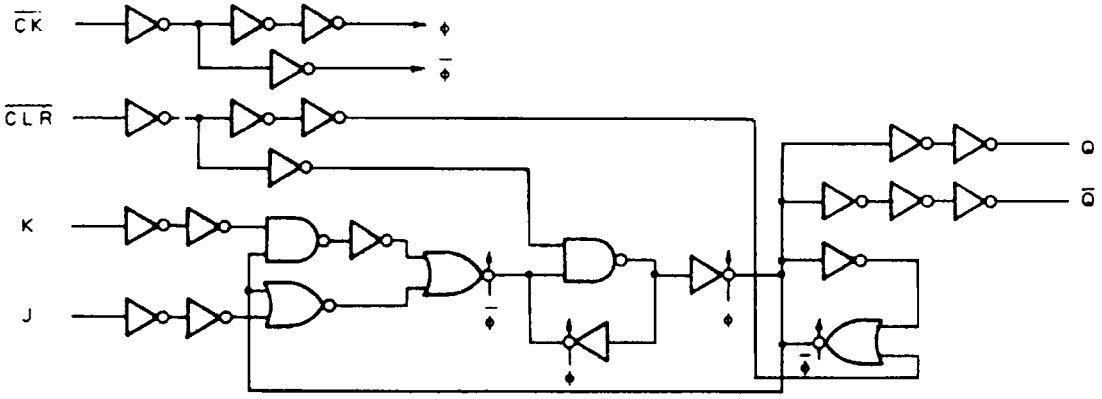
Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Output Transition Time	t_{TLH} t_{THL}	–	–	6	12	ns
Propagation Delay Time (CLOCK-Q,$\overline{Q}$)	t_{pLH} t_{pHL}	–	–	11	21	
Propagation Delay Time ($\overline{CLR}$-Q,$\overline{Q}$)	t_{pLH} t_{pHL}	–	–	15	25	
Maximum Clock Frequency	f_{MAX}	–	35	75	–	MHz

AC Electrical Characteristics ($C_L = 50pF$, Input $t_r = t_f = 6ns$)

Parameter	Symbol	Test Condition		Ta = 25°C			Ta = -40 ~ 85°C		Unit
			V_{CC}	Min	Typ.	Max.	Min.	Max.	
Output Transition Time	t_{TLH} t_{THL}	–	2.0	–	30	75	–	95	ns
			4.5	–	8	15	–	19	
			6.0	–	7	13	–	16	
Propagation Delay Time (CLOCK--Q,$\overline{Q}$)	t_{pLH} t_{pHL}	–	2.0	–	42	125	–	155	
			4.5	–	14	25	–	31	
			6.0	–	12	21	–	26	
Propagation Delay Time (CLOCK--Q,$\overline{Q}$)	t_{pLH} t_{pHL}	–	2.0	–	54	145	–	180	
			4.5	–	18	29	–	36	
			6.0	–	15	25	–	31	
Maximum Clock Frequency	f_{MAX}	–	2.0	6	15	–	5	–	MHz
			4.5	30	60	–	24	–	
			6.0	35	80	–	28	–	
Input Capacitance	C_{IN}	–		–	5	10	–	10	pF
Power Dissipation Capacitance	C_{PD}(1)	–		–	35	–	–	–	

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation:

$I_{CC(opr)} = C_{PD} \bullet V_{CC} \bullet f_{IN} + I_{CC}/2$(per F/F)



Logic Diagram