Features

- ESD Protection for 1 Line with Bi-directional.
- Provide ESD protection for the protected line to
  IEC 61000-4-2 (ESD) ±20kV (air), ±12kV (contact)
  IEC 61000-4-4 (EFT) 40A (5/50ns)
  IEC 61000-4-5 (Lightning) 7A (8/20μs)
  Cable Discharge Event (CDE)
- Ultra-small SOD-523 package saves board space.
- Protect one I/O line or one power line
- Fast turn-on and Low clamping voltage
- For low operating voltage applications: 5V, 4.2V, 3.3V, 2.5V
- Solid-state silicon-avalanche and active circuit triggering technology

Applications

- Computer Interfaces Protection
- Microprocessors Protection
- Serial and Parallel Ports Protection
- Control Signal Lines Protection
- Power lines on PCB Protection
- Latchup Protection

Description

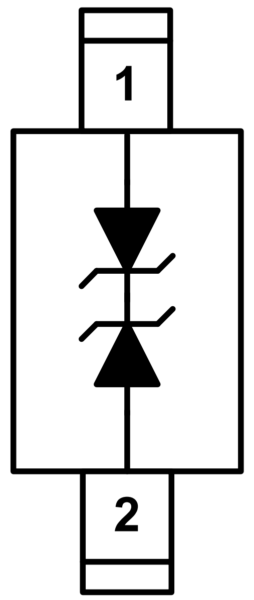
AZ2025-01H is a design which includes a bi-directional surge rated clamping cell to protect one power line, or one control line, or one low speed data line in an electronic systems. The AZ2025-01H has been specifically designed to protect sensitive components which are connected to power and control lines from over-voltage damage and latch-up caused by Electrostatic Discharging (ESD), Electrical Fast Transients (EFT), Lightning, and Cable Discharge Event (CDE).

AZ2025-01H is a unique design which includes proprietary clamping cells in a single package. During transient conditions, the proprietary clamping cells prevent over-voltage on the power line or control/data lines, protecting any downstream components.

AZ2025-01H is bi-directional and may be used on lines where the signal swings above and below ground.

AZ2025-01H may be used to meet the ESD immunity requirements of IEC 61000-4-2, Level 4 (±15kV air, ±8kV contact discharge).

Circuit Diagram / Pin Configuration



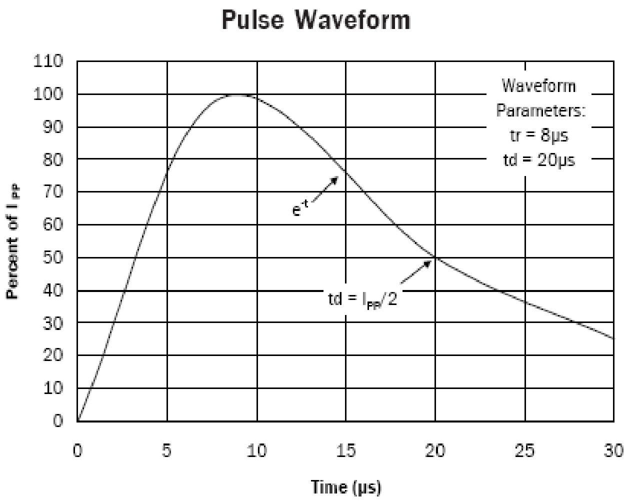
SOD-523 (Top View)

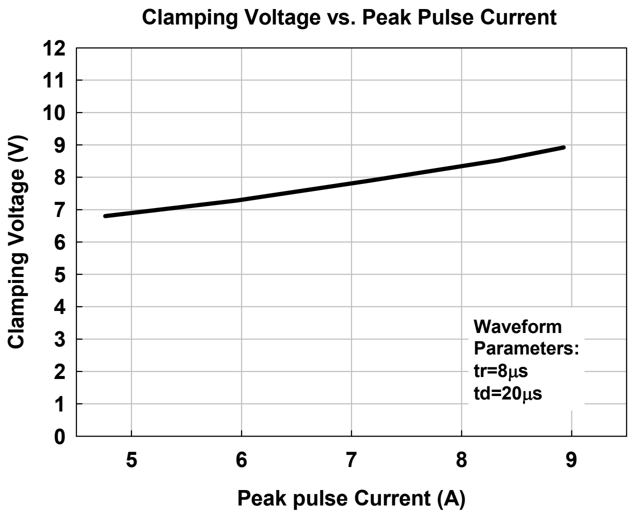
SPECIFICATIONS

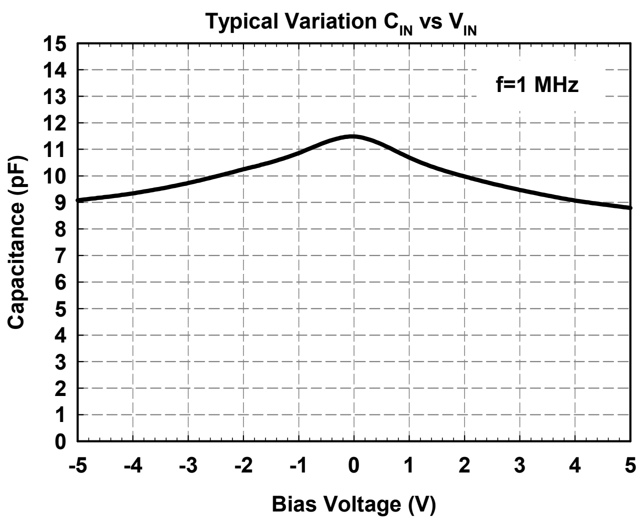
ABSOLUTE MAXIMUM RATINGS			
PARAMETER	PARAMETER	RATING	UNITS
Peak Pulse Current (tp =8/20us)	I_{PP}	8.5	A
Operating Supply Voltage (pin-1,-2 to pin-3)	V_{DC}	6	V
ESD per IEC 61000-4-2 (Air) ESD per IEC 61000-4-2 (Contact)	V_{ESD-1}	±22 ±15	kV
Lead Soldering Temperature	T_{SOL}	260 (10 sec.)	^oC
Operating Temperature	T_{OP}	-55 to +125	^oC
Storage Temperature	T_{STO}	-55 to +150	^oC

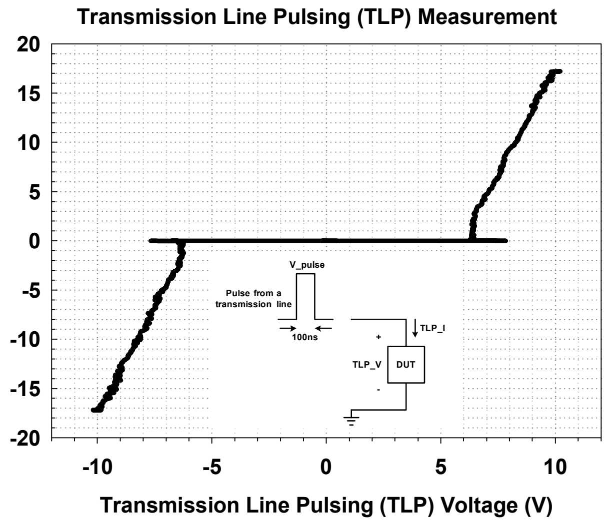
ELECTRICAL CHARACTERISTICS						
PARAMETER	SYMBOL	CONDITIONS	MINI	TYP	MAX	UNITS
Reverse Stand-Off Voltage	V_{RWM}	T=25 ^oC.			5	V
Reverse Leakage Current	I_{Leak}	V_{RWM} = 5V, T=25 ^oC.			2.5	μA
Reverse Breakdown Voltage	V_{BV}	I_{BV} = 1mA, T=25 ^oC.	6.1		9	V
Clamping Voltage	V_{CL}	I_{PP}=5A, tp=8/20us, T=25 ^oC.		7	8	V
Clamping Voltage	V_{CL}	I_{PP}=7A, tp=8/20us, T=25 ^oC.		8	9	V
ESD Holding Voltage	V_{hold}	IEC 61000-4-2 6kV, T=25 ^oC, Contact mode.		10.5		V
Channel Input Capacitance	C_{IN}	V_R = 0V, f = 1MHz, T=25 ^oC.		11.5	13.5	pF

Typical Characteristics









Applications Information

The AZ2025-01H is designed to protect one line against System ESD/EFT/Lightning pulses by clamping them to an acceptable reference. It provides bi-directional protection.

The usage of the AZ2025-01H is shown in Fig. 1. Protected line, such as data lines, control lines, or power lines, is connected at pin 1. The pin 2 is connected to a ground plane on the board. Since AZ2025-01H is bi-directional, these connections can be reversed (protected line to pin 2, ground to pin 1). In order to minimize parasitic inductance in the board traces, all path lengths connected to the pins of AZ2025-01H should be kept as short as possible.

In order to obtain enough suppression of ESD induced transient, good circuit board is critical. Thus, the following guidelines are recommended:

- Minimize the path length between the protected lines and the AZ2025-01H.
- Place the AZ2025-01H near the input terminals or connectors to restrict transient coupling.
- The ESD current return path to ground should be kept as short as possible.
- Use ground planes whenever possible.
- NEVER route critical signals near board edges and near the lines which the ESD transient easily injects to.

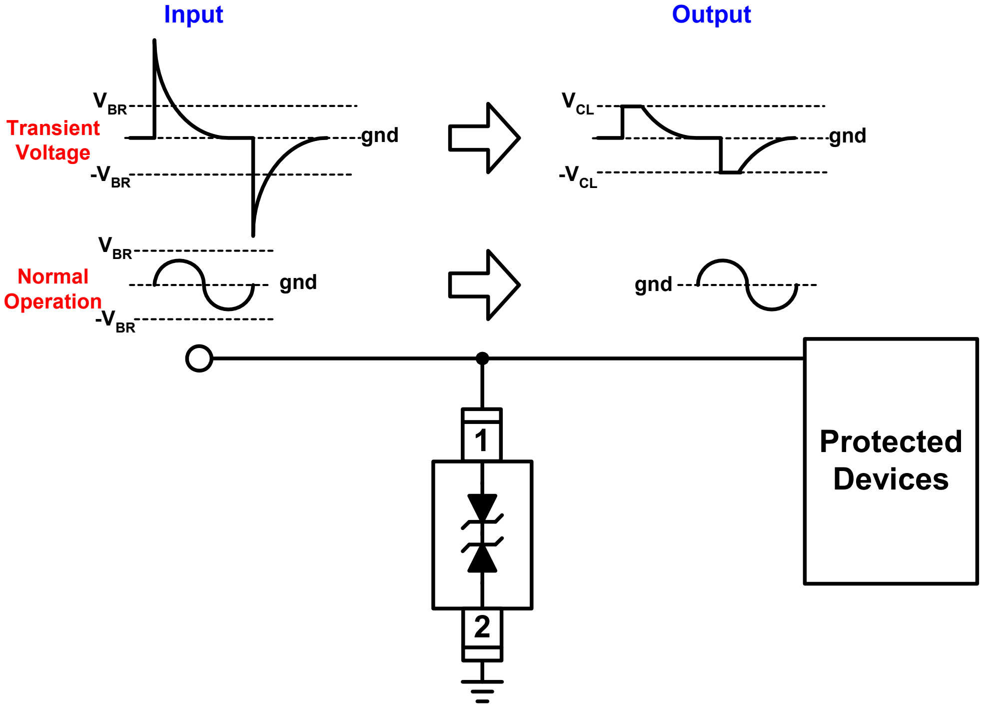
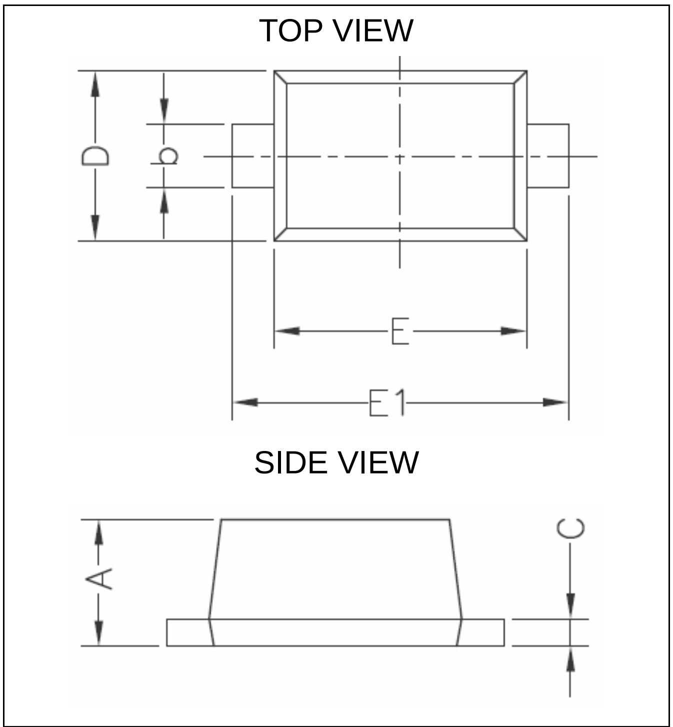


Fig. 1

Mechanical Details

SOD-523

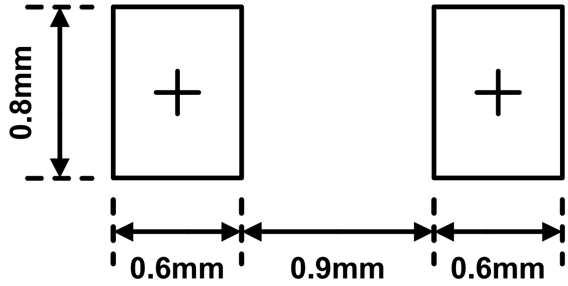
PACKAGE DIAGRAMS



PACKAGE DIMENSIONS

Symbol	Milimeters		Inches	
	MIN.	MAX.	MIN.	MAX.
A	0.50	0.70	.020	.028
b	0.30 BSC		.012 BSC	
C	0.08	0.20	.0031	.0078
D	0.70	0.90	.028	.035
E	1.10	1.30	.043	.051
E1	1.50	1.70	.059	.067

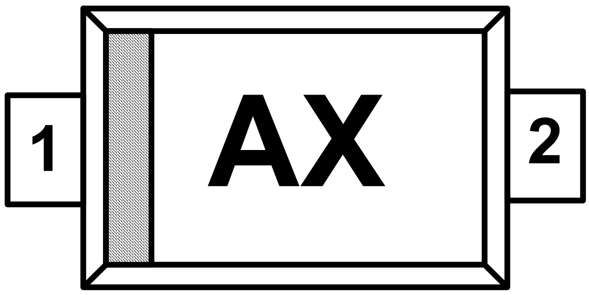
LAND LAYOUT



Notes:

This LAND LAYOUT is for reference purposes only. Please consult your manufacturing partners to ensure your company's PCB design guidelines are met.

MARKING CODE



A = Device Code
X = Date Code

Part Number	Marking Code
AZ2025-01H (Rohs part)	AX
AZ2025-01H (Green part)	aX

Revision History

Revision	Modification Description
Revision 2006/10/20	Original Release.
Revision 2006/12/08	1. Change the clamping cell symbol for easy understanding. 2. Change the TLP characterization from 6A to 17A. 3. Add the ESD holding voltage characterization under IEC 61000-4-2 6kV contact mode. 4. Update the C_{IN} value (typ, max.) from (12 pF, 15 pF) to (11.5 pF, 13.5 pF).
Revision 2007/02/07	1. Change the Characterization Temp of V_{RWM}, V_{Leak}, and V_{BV} from 125°C to 25°C. 2. Modify the ABSOLUTE MAXIMUM RATINGS of ESD.
Revision 2007/05/15	Change Qty per Reel from 3000 to 4000 in the Ordering Information.
Revision 2007/08/01	Remove the Ordering Information.
Revision 2008/03/24	Modify the description in the Features, from “Low operating voltage: 5V” to “For low operating voltage applications: 5V, 4.2V, 3.3V, 2.5V”.
Revision 2008/04/10	Add marking code for the Green part.