

# SN74CBT3257 4-BIT 1-OF-2 FET MULTIPLEXER/DEMULTIPLEXER

SCDS0171 – MAY 1995 – REVISED MAY 1998

- Functionally Equivalent to QS3257
- 5-Ω Switch Connection Between Two Ports
- TTL-Compatible Input Levels
- Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB, DBQ), and Thin Shrink Small-Outline (PW) Packages

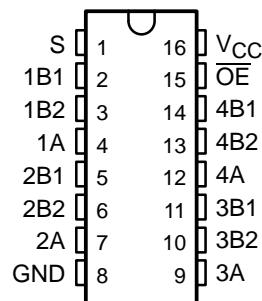
## description

The SN74CBT3257 is a 4-bit 1-of-2 high-speed TTL-compatible FET multiplexer/demultiplexer. The low on-state resistance of the switch allows connections to be made with minimal propagation delay.

Output-enable ( $\overline{OE}$ ) and select-control (S) inputs select the appropriate B1 and B2 outputs for the A-input data.

The SN74CBT3257 is characterized for operation from  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ .

D, DB, DBQ, OR PW PACKAGE  
(TOP VIEW)



FUNCTION TABLE

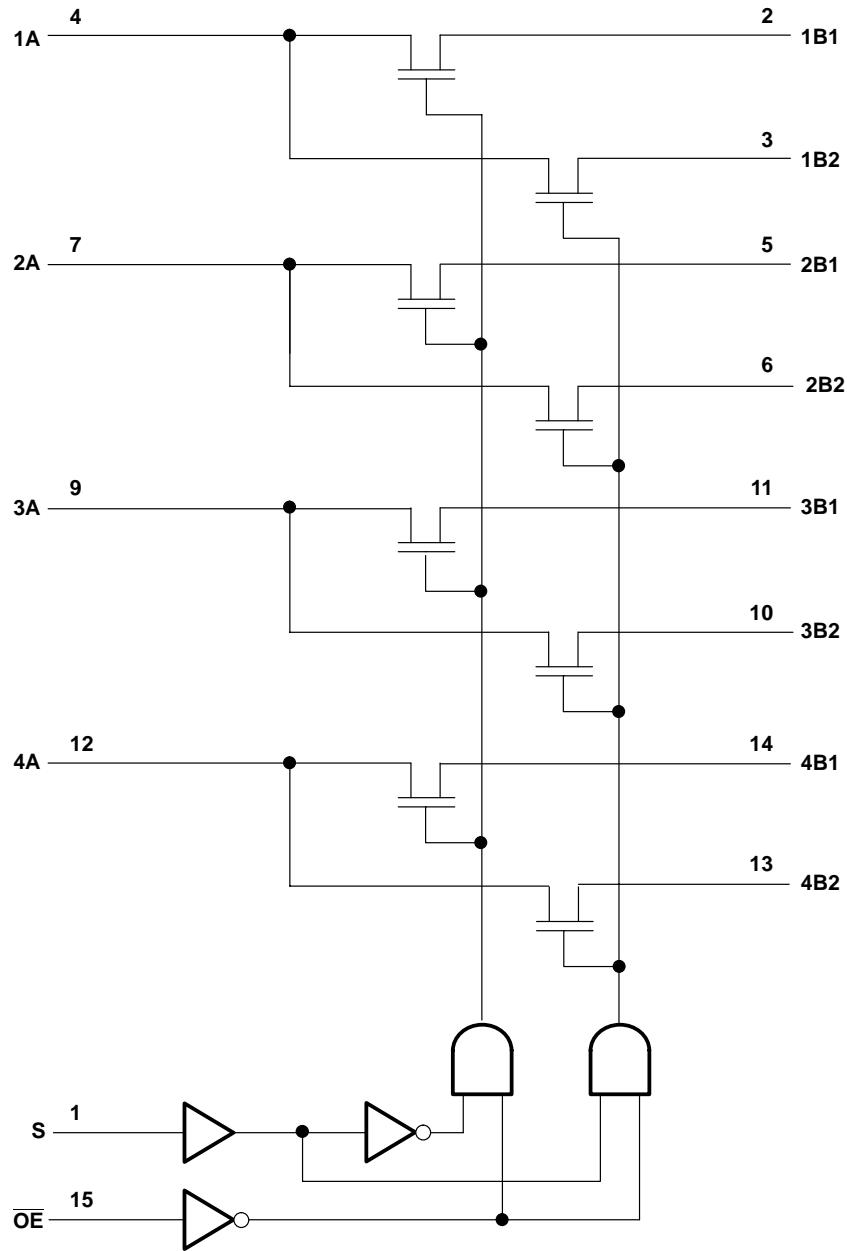
INPUTS		FUNCTION
$\overline{OE}$	S	
L	L	A port = B1 port
L	H	A port = B2 port
H	X	Disconnect

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### logic diagram (positive logic)



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### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ .....	–0.5 V to 7 V	
Input voltage range, $V_I$ (see Note 1) .....	–0.5 V to 7 V	
Continuous channel current .....	128 mA	
Input clamp current, $I_K$ ( $V_{I/O} < 0$ ) .....	–50 mA	
Package thermal impedance, $\theta_{JA}$ (see Note 2):	D package .....	113°C/W
	DB package .....	131°C/W
	DBQ package .....	139°C/W
	PW package .....	149°C/W
Storage temperature range, $T_{stg}$ .....	–65°C to 150°C	

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.  
 2. The package thermal impedance is calculated in accordance with JESD 51.

### recommended operating conditions (see Note 3)

	MIN	MAX	UNIT
$V_{CC}$ Supply voltage	4	5.5	V
$V_{IH}$ High-level control input voltage	2		V
$V_{IL}$ Low-level control input voltage		0.8	V
$T_A$ Operating free-air temperature	–40	85	°C

NOTE 3: All unused control inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP‡	MAX	UNIT
$V_{IK}$	$V_{CC} = 4.5$ V, $I_I = -18$ mA			–1.2	V
$I_I$	$V_{CC} = 5.5$ V, $V_I = 5.5$ V or GND			±1	µA
$I_{CC}$	$V_{CC} = 5.5$ V, $I_O = 0$ , $V_I = V_{CC}$ or GND			3	µA
$\Delta I_{CC}^{\S}$	Control inputs $V_{CC} = 5.5$ V, One input at 3.4 V, Other inputs at $V_{CC}$ or GND			2.5	mA
$C_i$	Control inputs $V_I = 3$ V or 0		3.5		pF
$C_{iO(OFF)}$	A port $V_O = 3$ V or 0, $\overline{OE} = V_{CC}$		6.5		pF
	B port		4		
$r_{on}^{\parallel}$	$V_{CC} = 4$ V, TYP at $V_{CC} = 4$ V	$V_I = 2.4$ V,		$I_I = 15$ mA	Ω
	$V_{CC} = 4.5$ V	$V_I = 0$		$I_I = 64$ mA	
		$V_I = 2.4$ V,		$I_I = 30$ mA	
		$V_I = 2.4$ V,		$I_I = 15$ mA	

‡ All typical values are at  $V_{CC} = 5$  V (unless otherwise noted),  $T_A = 25^\circ\text{C}$ .

§ This is the increase in supply current for each input that is at the specified TTL voltage level rather than  $V_{CC}$  or GND.

∥ Measured by the voltage drop between the A and the B terminals at the indicated current through the switch. On-state resistance is determined by the lowest voltage of the two (A or B) terminals.



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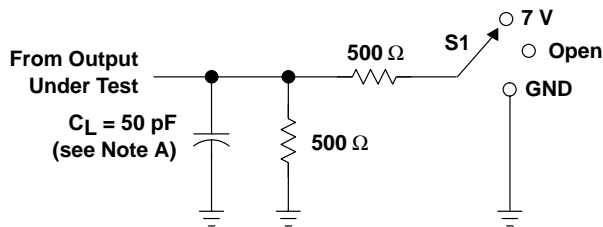
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switching characteristics over recommended operating free-air temperature range,  $C_L = 50$  pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 4$ V		$V_{CC} = 5$ V $\pm 0.5$ V		UNIT
			MIN	MAX	MIN	MAX	
$t_{pd}^\dagger$	A or B	B or A	0.35		0.25		ns
$t_{pd}$	S	A	5.5		1.6	5	ns
$t_{en}$	S	B	5.7		1.6	5.2	ns
	$\overline{OE}$	A or B	5.6		1.8	5.1	
$t_{dis}$	S	B	5.2		1	5	ns
	$\overline{OE}$	A or B	5.5		2.2	5.5	

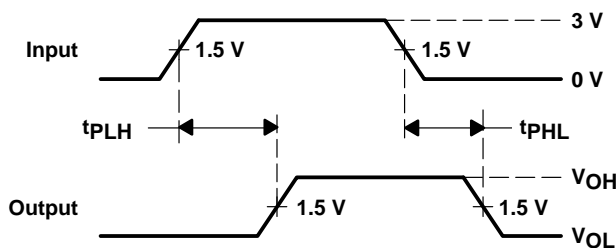
$^\dagger$  The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

### PARAMETER MEASUREMENT INFORMATION

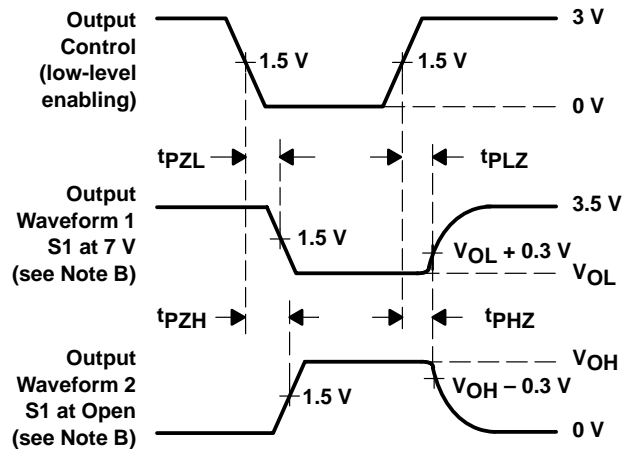


LOAD CIRCUIT

TEST	S1
$t_{pd}$	Open
$t_{PLZ}/t_{PZL}$	7 V
$t_{PHZ}/t_{PZH}$	Open



VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES

- NOTES:
- $C_L$  includes probe and jig capacitance.
  - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10$  MHz,  $Z_O = 50 \Omega$ ,  $t_r \leq 2.5$  ns,  $t_f \leq 2.5$  ns.
  - The outputs are measured one at a time with one transition per measurement.
  - $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
  - $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
  - $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .

Figure 1. Load Circuit and Voltage Waveforms