Octal D-type flip-flop with 5-volt tolerant inputs/outputs; positive edge-trigger; 3-state

74LVC374A 74LVCH374A

FEATURES

- **5-Volt tolerant inputs/outputs, for interfacing with 5-volt logic.**
- **Supply voltage range of 2.7 V to 3.6 V**
- **In accordance with JEDEC standard no. 8-1A.**
- **CMOS low power consumption**
- **Direct interface with TTL levels**
- **High impedance when V_{CC}= 0 V**
- **8-bit positive edge-triggered register**
- **Independent register and 3-state buffer operation**
- **Bushold on all data inputs (LVCH374A only).**

DESCRIPTION

The 74LVC(H)374A is a high-performance, low-power, low-voltage, Si-gate CMOS device and superior to most advanced CMOS compatible TTL families.

Inputs can be driven from either 3.3 V or 5 V devices. In 3-state operation, outputs can handle 5 V.This feature allows the use of these devices as translators in a mixed 3.3 V/5 V environment.

The 74LVC(H)374A is an octal D-type flip-flop featuring separate D-type inputs for each flip-flop and 3-state outputs for bus oriented applications. A clock (CP) and an output enable ($\overline{OE}$) input are common to all flip-flops.

The eight flip-flops will store the state of their individual D-inputs that meet the set-up and hold times requirements on the LOW-to-HIGH CP transition.

When $\overline{OE}$ is LOW, the contents of the eight flip-flops is available at the outputs. When $\overline{OE}$ is HIGH, the outputs go to the high impedance OFF-state. Operation of the $\overline{OE}$ input does not affect the state of the flip-flops. The '374' is functionally identical to the '574', but the '574' has a different pin arrangement.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	propagation delay CP to Q_n	C_L = 50 pF V_{CC} = 3.3 V	4.8	ns
f_{max}	maximum clock frequency		150	MHz
C_I	input capacitance		5.0	pF
C_{PD}	power dissipation capacitance per flip-flop	notes 1 and 2	20	pF

Notes to the quick reference data

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.
2. The condition is V_I = GND to V_{CC}.

ORDERING INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74LVC(H)374AD	20	SO	plastic	SOT163-1
74LVC(H)374ADB	20	SSOP	plastic	SOT339-1
74LVC(H)374APW	20	TSSOP	plastic	SOT360-1

PINNING

PIN	SYMBOL	NAME AND FUNCTION
1	$\overline{OE}$	output enable input (active LOW)
2, 5, 6, 9, 12, 15, 16, 19	Q_0 to Q_7	3-state flip-flop outputs
3, 4, 7, 8, 13, 14, 17, 18	D_0 to D_7	data inputs
10	GND	ground (0 V)
11	CP	clock input (LOW-to-HIGH, edge-triggered)
20	V_{CC}	positive supply voltage

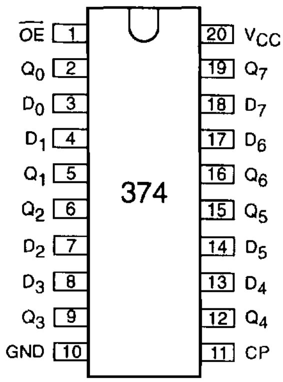


Fig.1 Pin configuration.

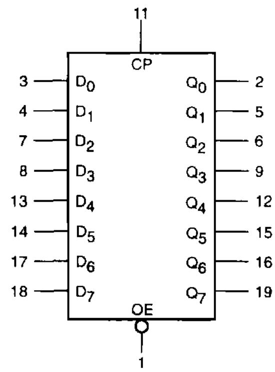


Fig.2 Logic symbol.

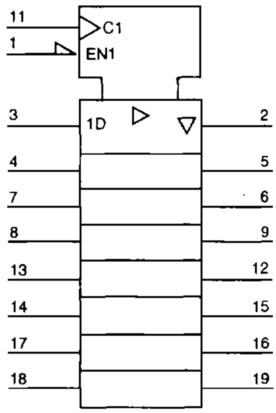


Fig3. IEC logic symbol.

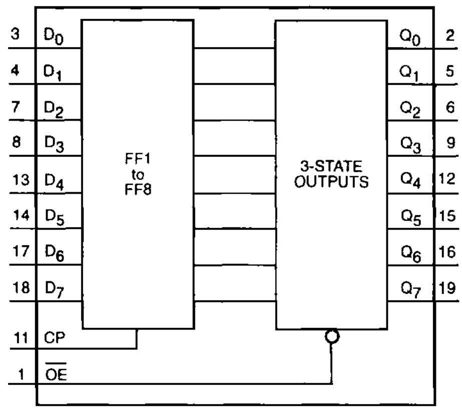


Fig.4 Functional diagram.

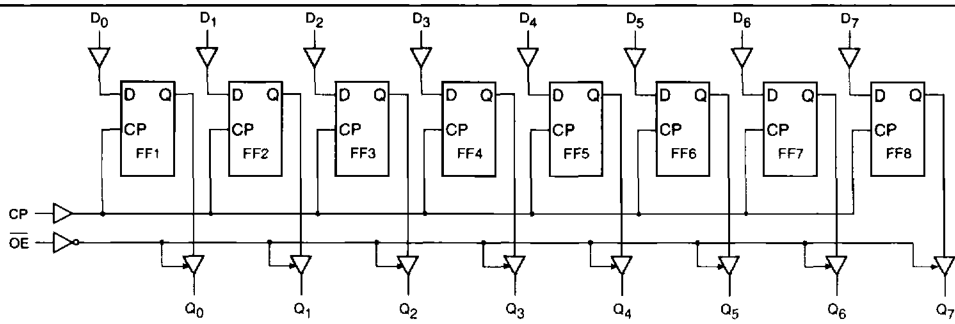


Fig.5 Logic diagram.

FUNCTION TABLE

OPERATING MODES	INPUTS			INTERNAL FLIP-FLOPS	OUTPUTS
	$\overline{OE}$	CP	D_n		Q_0 to Q_7
load and read register	L L	↑ ↑	l h	L H	L H
load register and disable outputs	H H	↑ ↑	l h	L H	Z Z

H = HIGH voltage level
h = HIGH voltage level one set-up time prior to the LOW-to-HIGH CP transition
L = LOW voltage level
l = LOW voltage level one set-up time prior to the LOW-to-HIGH CP transition
Z = high impedance OFF-state
↑ = LOW-to-HIGH clock transition

DC CHARACTERISTICS FOR 74LVC(H)374A
For the DC characteristics see chapter "LVC(H)-A family characteristics", section "Family specifications".

AC CHARACTERISTICS FOR 74LVC(H)374A
GND = 0 V; $t_r = t_f \leq 2.5$ ns; $C_L = 50$ pF

SYMBOL	PARAMETER	T_{amb} (°C) -40 to +85			UNIT	TEST CONDITIONS	
		MIN.	TYP.	MAX.		V_{CC} (V)	WAVEFORMS
t_{PHL}/t_{PLH}	propagation delay CP to Q_n	– 1.5 1.5	– – –	– 9.5 8.5	ns	1.2 2.7 3.0 to 3.6	Figs 6, 9
t_{PZH}/t_{PZL}	3-state output enable time $\overline{OE}$ to Q_n	– 1.5 1.5	– – –	– 8.5 7.5	ns	1.2 2.7 3.0 to 3.6	Figs 7, 9
t_{PHZ}/t_{PLZ}	3-state output disable time $\overline{OE}$ to Q_n	– 1.5 1.5	– – –	– 6.5 6.0	ns	1.2 2.7 3.0 to 3.6	Figs 7, 9
t_W	clock pulse width HIGH or LOW	– –	– –	– –	ns	2.7 3.0 to 3.6	Fig.6
t_{su}	set-up time D_n to CP	– –	– –	– –	ns	2.7 3.0 to 3.6	Fig.8
t_h	hold time D_n to CP	1.0 1.0	– –	– –	ns	2.7 3.0 to 3.6	Fig.8
f_{max}	maximum clock pulse frequency	– 75	– –	– –	MHz	2.7 3.0 to 3.6	Fig.6

Notes: All typical values are measured at T_{amb} = 25 °C.
* Typical values are measured at V_{CC} = 3.3 V.

AC WAVEFORMS

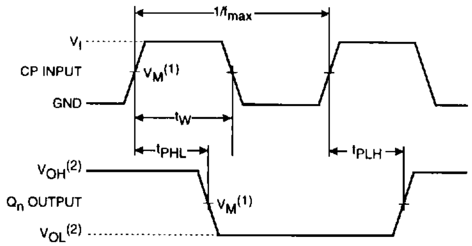


Fig.6 Waveforms showing the clock (CP) to output (Q_n) propagation delays, the clock pulse width, output transition times and the maximum clock pulse frequency.

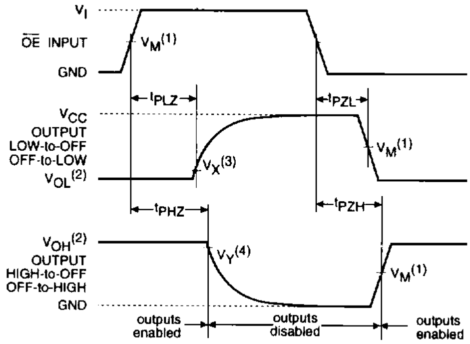


Fig.7 Waveforms showing the 3-state enable and disable times.

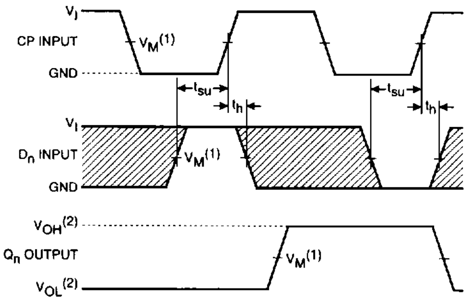
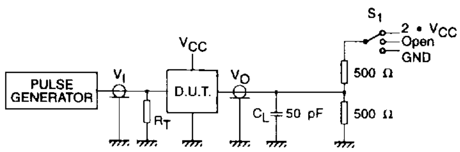


Fig.8 Waveforms showing the data set-up and hold times for the D_n input to the CP input.

Note to Fig.8:

The shaded areas indicate when the input is permitted to change for predictable output performance.



V_{CC}	V_I
< 2.7 V	V_{CC}
2.7 - 3.6 V	2.7 V

Test	S_1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 • V_{CC}
t_{PHZ}/t_{PZH}	GND

Fig.9 Load circuitry for switching times.

Notes:

(1) $V_M = 1.5$ V at $V_{CC} \geq 2.7$ V
$V_M = 0.5 \cdot V_{CC}$ at $V_{CC} < 2.7$ V

(2) V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load

(3) $V_X = V_{OL} + 0.3$ V at $V_{CC} \geq 2.7$ V
$V_X = V_{OL} + 0.1 \cdot V_{CC}$ at $V_{CC} < 2.7$ V

(4) $V_Y = V_{OH} - 0.3$ V at $V_{CC} \geq 2.7$ V
$V_Y = V_{OH} - 0.1 \cdot V_{CC}$ at $V_{CC} < 2.7$ V