SDLS118 – DECEMBER 1983 – REVISED MARCH 1988

- **Package Options Include Plastic "Small Outline" Packages, Flat Packages, and Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

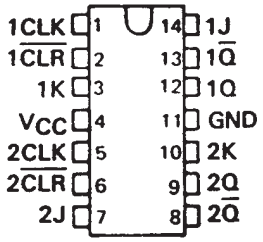
## description

The '73, and 'H73, contain two independent J-K flip-flops with individual J-K, clock, and direct clear inputs. The '73, and 'H73, are positive pulse-triggered flip-flops. J-K input is loaded into the master while the clock is high and transferred to the slave on the high-to-low transition. For these devices the J and K inputs must be stable while the clock is high.

The 'LS73A contains two independent negative-edge-triggered flip-flops. The J and K inputs must be stable one setup time prior to the high-to-low clock transition for predictable operation. When the clear is low, it overrides the clock and data inputs forcing the Q output low and the $\overline{Q}$ output high.

The SN5473, SN54H73, and the SN54LS73A are characterized for operation over the full military temperature range of −55°C to 125°C. The SN7473, and the SN74LS73A are characterized for operation from 0°C to 70°C.

**SN5473, SN54LS73A . . . J OR W PACKAGE**
**SN7473 . . . N PACKAGE**
**SN74LS73A . . . D OR N PACKAGE**
**(TOP VIEW)**




**'73**
**FUNCTION TABLE**

| INPUTS | | | | OUTPUTS | |
|---|---|---|---|---|---|
| $\overline{CLR}$ | CLK | J | K | Q | $\overline{Q}$ |
| L | X | X | X | L | H |
| H | ⊓ | L | L | $Q_0$ | $\overline{Q}_0$ |
| H | ⊓ | H | L | H | L |
| H | ⊓ | L | H | L | H |
| H | ⊓ | H | H | TOGGLE | |

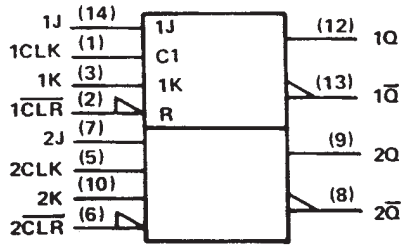
**'LS73A**
**FUNCTION TABLE**

| INPUTS | | | | OUTPUTS | |
|---|---|---|---|---|---|
| $\overline{CLR}$ | CLK | J | K | Q | $\overline{Q}$ |
| L | X | X | X | L | H |
| H | ↓ | L | L | $Q_0$ | $\overline{Q}_0$ |
| H | ↓ | H | L | H | L |
| H | ↓ | L | H | L | H |
| H | ↓ | H | H | TOGGLE | |
| H | H | X | X | $Q_0$ | $\overline{Q}_0$ |

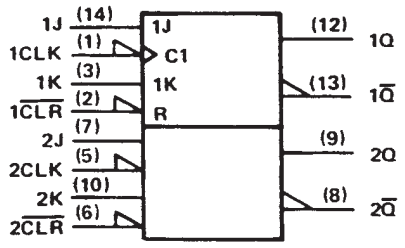
**FOR CHIP CARRIER INFORMATION, CONTACT THE FACTORY**

## logic symbols†

'73




'LS73A

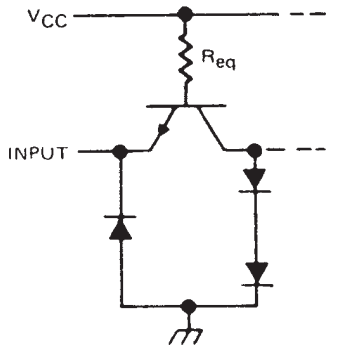



†These symbols are in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12.

## schematics of inputs and outputs

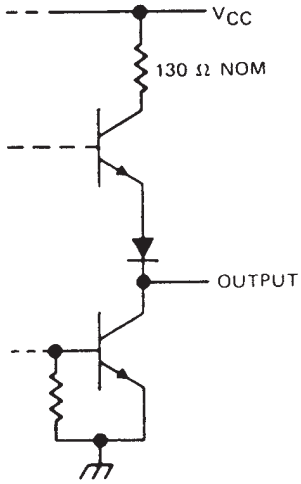
'73

EQUIVALENT OF EACH INPUT



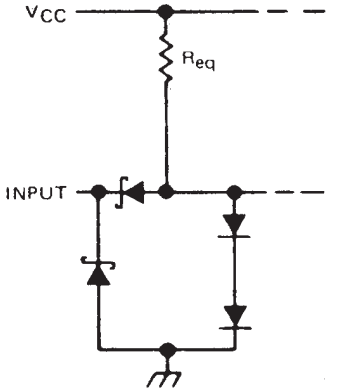

| $I_{IL}$ MAX | $R_{eq}$ NOM |
|---|---|
| – 1.6 mA | 4 kΩ |
| – 3.2 mA | 2 kΩ |

TYPICAL OF ALL OUTPUTS



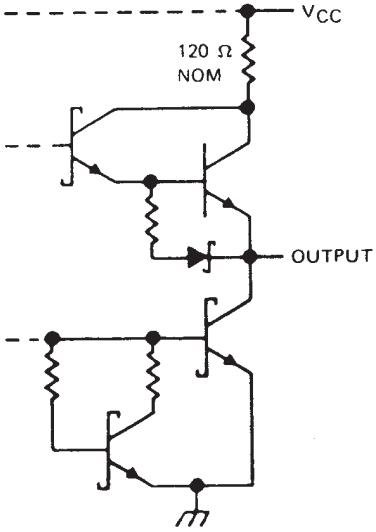

'LS73

EQUIVALENT OF EACH INPUT



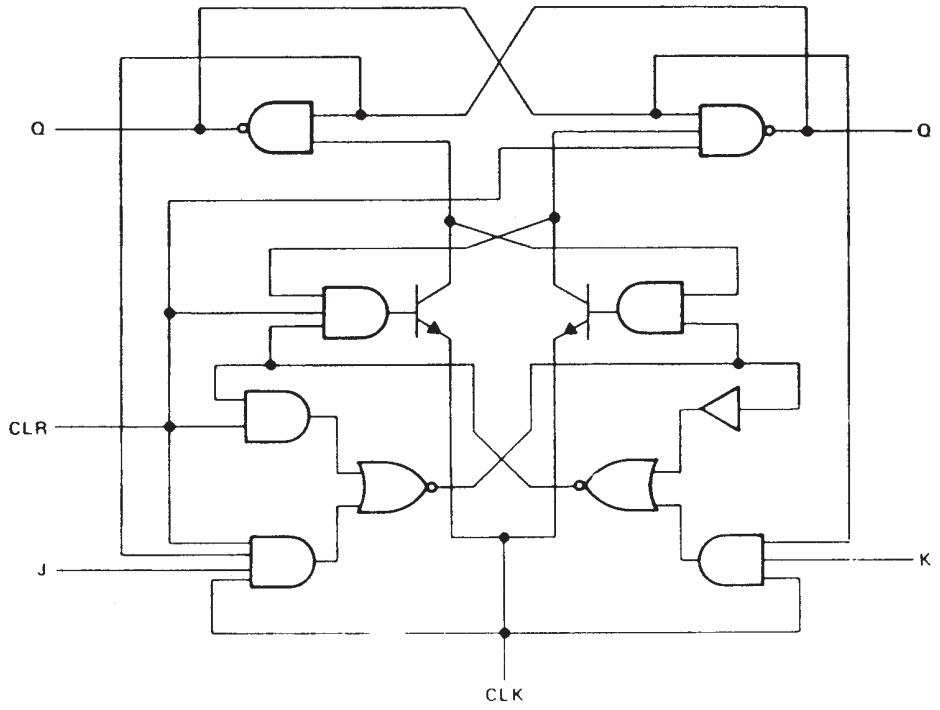

| $I_{IL}$ MAX | $R_{eq}$ NOM |
|---|---|
| – 0.4 mA | 30 kΩ |
| – 0.8 mA | 8.25 kΩ |

TYPICAL OF ALL OUTPUTS

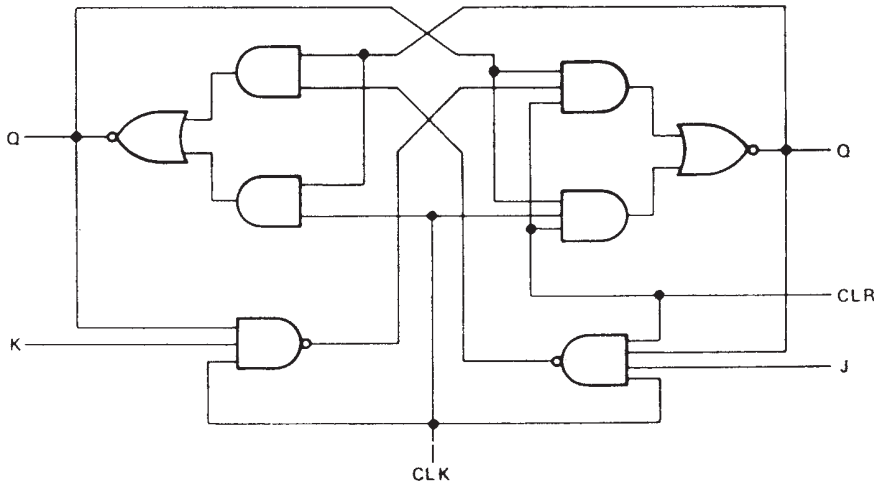


## logic diagrams (positive logic)

'73




'LS73A




## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, $V_{CC}$ (See Note 1) . . . . . 7 V
Input voltage: '73 . . . . . 5.5 V
'LS73A . . . . . 7 V
Operating free-air temperature range: SN54' . . . . . −55°C to 125°C
SN74' . . . . . 0° C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

## recommended operating conditions

| | | | SN5473 | | | SN7473 | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | NOM | MAX | MIN | NOM | MAX | |
| $V_{CC}$ | Supply voltage | | 4.5 | 5 | 5.5 | 4.75 | 5 | 5.25 | V |
| $V_{IH}$ | High-level input voltage | | 2 | | | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | | 0.8 | | | 0.8 | V |
| $I_{OH}$ | High-level output current | | | | −0.4 | | | −0.4 | mA |
| $I_{OL}$ | Low-level output current | | | | 16 | | | 16 | mA |
| $t_w$ | Pulse duration | CLK high | 20 | | | 20 | | | ns |
| | | CLK low | 47 | | | 47 | | | |
| | | $\overline{CLR}$ low | 25 | | | 25 | | | |
| $t_{su}$ | Input setup time before CLK↑ | | 0 | | | 0 | | | ns |
| $t_h$ | Input hold time data after CLK↓ | | 0 | | | 0 | | | ns |
| $T_A$ | Operating free-air temperature | | −55 | | 125 | 0 | | 70 | °C |

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS† | | | SN5473 | | | SN7473 | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | MIN | TYP‡ | MAX | MIN | TYP‡ | MAX | |
| $V_{IK}$ | | $V_{CC}$ = MIN, | $I_I$ = −12 mA | | | | −1.5 | | | −1.5 | V |
| $V_{OH}$ | | $V_{CC}$ = MIN, $I_{OH}$ = −0.4 mA | $V_{IH}$ = 2 V, | $V_{IL}$ = 0.8 V, | 2.4 | 3.4 | | 2.4 | 3.4 | | V |
| $V_{OL}$ | | $V_{CC}$ = MIN, $I_{OL}$ = 16 mA | $V_{IH}$ = 2 V, | $V_{IL}$ = 0.8 V, | | 0.2 | 0.4 | | 0.2 | 0.4 | V |
| $I_I$ | | $V_{CC}$ = MAX, | $V_I$ = 5.5 V | | | | 1 | | | 1 | mA |
| $I_{IH}$ | J or K | $V_{CC}$ = MAX, | $V_I$ = 2.4 V | | | | 40 | | | 40 | μA |
| | $\overline{CLR}$ or CLK | | | | | | 80 | | | 80 | |
| $I_{IL}$ | J or K | $V_{CC}$ = MAX, | $V_I$ = 0.4 V | | | | −1.6 | | | −1.6 | mA |
| | $\overline{CLR}$ | | | | | | −3.2 | | | −3.2 | |
| | CLK | | | | | | −3.2 | | | −3.2 | |
| $I_{OS}$§ | | $V_{CC}$ = MAX | | | −20 | | −57 | −18 | | −57 | mA |
| $I_{CC}$¶ | | $V_{CC}$ = MAX, | See Note 2 | | | 10 | 20 | | 10 | 20 | mA |

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.
§ Not more than one output should be shorted at a time.
¶ Average per flip-flop.
NOTE 2: With all outputs open, $I_{CC}$ is measured with the Q and $\overline{Q}$ outputs high in turn. At the time of measurement, the clock input is grounded.

## switching characteristics, $V_{CC}$ = 5 V, $T_A$ = 25°C (see note 3)

| PARAMETER# | FROM (INPUT) | TO (OUTPUT) | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $f_{max}$ | | | $R_L$ = 400 Ω, $C_L$ = 15 pF | 15 | 20 | | MHz |
| $t_{PLH}$ | $\overline{CLR}$ | $\overline{Q}$ | | | 16 | 25 | ns |
| $t_{PHL}$ | | Q | | | 25 | 40 | ns |
| $t_{PLH}$ | CLK | Q or $\overline{Q}$ | | | 16 | 25 | ns |
| $t_{PHL}$ | | | | | 25 | 40 | ns |

#$f_{max}$ = maximum clock frequency: $t_{PLH}$ = propagation delay time, low-to-high-level output; $t_{PHL}$ = propagation delay time, high-to-low-level output.
NOTE 3: Load circuits and voltage waveforms are shown in Section 1.

## recommended operating conditions

| | | | SN54LS73A | | | SN74LS73A | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | NOM | MAX | MIN | NOM | MAX | |
| $V_{CC}$ | Supply voltage | | 4.5 | 5 | 5.5 | 4.75 | 5 | 5.25 | V |
| $V_{IH}$ | High-level input voltage | | 2 | | | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | | 0.7 | | | 0.8 | V |
| $I_{OH}$ | High-level output current | | | | −0.4 | | | −0.4 | mA |
| $I_{OL}$ | Low-level output current | | | | 4 | | | 8 | mA |
| $f_{clock}$ | Clock frequency | | 0 | | 30 | 0 | | 30 | MHz |
| $t_w$ | Pulse duration | CLK high | 20 | | | 20 | | | ns |
| | | $\overline{CLR}$ low | 25 | | | 20 | | | |
| $t_{su}$ | Set up time-before CLK↓ | data high or low | 20 | | | 20 | | | ns |
| | | $\overline{CLR}$ inactive | 20 | | | 20 | | | |
| $t_h$ | Hold time-data after CLK↓ | | 0 | | | 0 | | | ns |
| $T_A$ | Operating free-air temperature | | −55 | | 125 | 0 | | 70 | °C |

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS† | | | SN54LS73A | | | SN74LS73A | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | MIN | TYP‡ | MAX | MIN | TYP‡ | MAX | |
| $V_{IK}$ | | $V_{CC}$ = MIN, | $I_I$ = −18 mA | | | | −1.5 | | | −1.5 | V |
| $V_{OH}$ | | $V_{CC}$ = MIN, $I_{OH}$ = −0.4 mA | $V_{IH}$ = 2 V, | $V_{IL}$ = MAX, | 2.5 | 3.4 | | 2.7 | 3.4 | | V |
| $V_{OL}$ | | $V_{CC}$ = MIN, $I_{OL}$ = 4 mA | $V_{IL}$ = MAX, | $V_{IH}$ = 2 V, | | 0.25 | 0.4 | | 0.25 | 0.4 | V |
| | | $V_{CC}$ = MIN, $I_{OL}$ = 8 mA | $V_{IL}$ = MAX, | $V_{IH}$ = 2 V, | | | | | 0.35 | 0.5 | |
| $I_I$ | J or K | $V_{CC}$ = MAX, | $V_I$ = 7 V | | | | 0.1 | | | 0.1 | mA |
| | $\overline{CLR}$ | | | | | | 0.3 | | | 0.3 | |
| | CLK | | | | | | 0.4 | | | 0.4 | |
| $I_{IH}$ | J or K | $V_{CC}$ = MAX, | $V_I$ = 2.7 V | | | | 20 | | | 20 | μA |
| | $\overline{CLR}$ | | | | | | 60 | | | 60 | |
| | CLK | | | | | | 80 | | | 80 | |
| $I_{IL}$ | J or K | $V_{CC}$ = MAX, | $V_I$ = 0.4 V | | | | −0.4 | | | −0.4 | mA |
| | $\overline{CLR}$ or CLK | | | | | | −0.8 | | | −0.8 | |
| $I_{OS}$§ | | $V_{CC}$ = MAX, | See Note 4 | | −20 | | −100 | −20 | | −100 | mA |
| $I_{CC}$ (Total) | | $V_{CC}$ = MAX, | See Note 2 | | | 4 | 6 | | 4 | 6 | mA |

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.
§ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.
NOTE 2: With all outputs open, $I_{CC}$ is measured with the Q and $\overline{Q}$ outputs high in turn. At the time of measurement, the clock input is grounded.
NOTE 4: For certain devices where state commutation can be caused by shorting an output to ground, an equivalent test may be performed with $V_O$ = 2.25 V and 2.125 V for the 54 family and the 74 family, respectively, with the minimum and maximum limits reduced to one half of their stated values.

## switching characteristics, $V_{CC}$ = 5 V, $T_A$ = 25°C (see note 3)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| $f_{max}$ | | | $R_L$ = 2 kΩ, | $C_L$ = 15 pF | 30 | 45 | | MHz |
| $t_{PLH}$ | $\overline{CLR}$ or CLK | Q or $\overline{Q}$ | | | | 15 | 20 | ns |
| $t_{PHL}$ | | | | | | 15 | 20 | ns |

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.

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**PRODUCT FOLDER** | PRODUCT INFO: FEATURES | DESCRIPTION | DATASHEETS | PRICING/AVAILABILITY/PKG | APPLICATION NOTES | USER GUIDES | MORE LITERATURE

PRODUCT SUPPORT: TRAINING

## SN54LS73A, Dual J-K Flip-Flops With Clear and 3-state Outputs

DEVICE STATUS: **ACTIVE**

| PARAMETER NAME | SN54LS73A | SN74LS73A |
|---|---|---|
| Voltage Nodes (V) | 5 | 5 |
| Vcc range (V) | 4.5 to 5.5 | 4.75 to 5.25 |
| Input Level | TTL | TTL |
| Output Level | TTL | TTL |
| Output Drive (mA) | | -0.4/8 |
| th (ns) | | 0 |
| tpd max (ns) | | 20 |
| tsu (ns) | | 20 |

### FEATURES

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- Package Options Include Plastic “Small Outline" Packages, Flat Packages, and Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

### DESCRIPTION

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The '73, and 'H73, contain two independent J-K flip-flops with individual J-K, clock, and direct clear inputs. The '73, and 'H73, are positive pulse-triggered flip-flops. J-K input is loaded into the master while the clock is high and transferred to the slave on the high-to-low transition. For these devices the J and K inputs must be stable while the clock is high.

The 'LS73A contains two independent negative-edge-triggered flip-flops. The J and K inputs must be stable one setup time prior to the high-to-low clock transition for predictable operation. When the clear is low, it overrides the clock and data inputs forcing the Q output low and the Q\ output high.

The SN5473, SN54H73, and the SN54LS73A are characterized for operation over the full military temperature range of -55°C to 125°C. The SN7473, and the SN74LS73A are characterized for operation from 0°C to 70°C.

### TECHNICAL DOCUMENTS

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To view the following documents, Acrobat Reader 4.0 is required.

To download a document to your hard drive, right-click on the link and choose 'Save'.

### DATASHEET

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Full datasheet in Acrobat PDF: sn54ls73a.pdf (206 KB) (Updated: 03/01/1988)

### APPLICATION NOTES

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View Application Notes for Digital Logic

Product Folder: SN54LS73A, Dual J-K Flip-Flops With Clear and 3-state Outputs

- Designing With Logic (Rev. C) (SDYA009C - Updated: 06/01/1997)
- Designing with the SN54/74LS123 (Rev. A) (SDLA006A - Updated: 03/01/1997)
- Evaluation of Nickel/Palladium/Gold-Finished Surface-Mount Integrated Circuits (SZZA026 - Updated: 06/20/2001)
- Input and Output Characteristics of Digital Integrated Circuits (SDYA010 - Updated: 10/01/1996)
- Live Insertion (SDYA012 - Updated: 10/01/1996)
- TI IBIS File Creation, Validation, and Distribution Processes (SZZA034 - Updated: 08/29/2002)
- Understanding and Interpreting Texas Instruments Standard-Logic Products Data Sh (Rev. A) (SZZA036A - Updated: 02/27/2003)

## MORE LITERATURE

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- Enhanced Plastic Portfolio Brochure (SGZB004, 387 KB - Updated: 08/19/2002)
- Logic Reference Guide (SCYB004, 1032 KB - Updated: 10/23/2001)
- MicroStar Junior BGA Design Summary (SCET004, 167 KB - Updated: 07/28/2000)
- Military Brief (SGYN138, 803 KB - Updated: 10/10/2000)
- Overview of IEEE Std 91-1984, Explanation of Logic Symbols Training Booklet (Rev. A) (SDYZ001A, 138 KB - Updated: 07/01/1996)
- Palladium Lead Finish User's Manual (SDYV001, 2041 KB - Updated: 11/01/1996)
- QML Class V Space Products Military Brief (Rev. A) (SGZN001A, 257 KB - Updated: 10/07/2002)

## USER GUIDES

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- LOGIC Pocket Data Book (SCYD013, 4837 KB - Updated: 12/05/2002)

## PRICING/AVAILABILITY/PKG

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**DEVICE INFORMATION**
Updated Daily

| ORDERABLE DEVICE | STATUS | PACKAGE TYPE \| PINS | TEMP (°C) | DSCC NUMBER | PRODUCT CONTENT | BUDGETARY PRICING QTY \| $US | STD PACK QTY |
|---|---|---|---|---|---|---|---|
| 5962-9675101QCA | ACTIVE | CDIP (J) \| 14 | -55 TO 125 | | View Contents | 1KU \| 1.93 | 1 |
| 5962-9675101QDA | ACTIVE | CFP (W) \| 14 | -55 TO 125 | | View Contents | 1KU \| 7.29 | 1 |
| SN54LS73AJ | ACTIVE | CDIP (J) \| 14 | -55 TO 125 | | View Contents | 1KU \| 1.65 | 1 |
| | | | | | | | |
| SNJ54LS73AFD | OBSOLETE | LCCC (FK) \| 20 | -55 TO 125 | | View Contents | 1KU \| | |
| | | | | | | | |
| SNJ54LS73AJ | ACTIVE | CDIP (J) \| 14 | -55 TO 125 | 5962-9675101QCA | View Contents | 1KU \| 1.93 | 1 |
| SNJ54LS73AW | ACTIVE | CFP (W) \| 14 | -55 TO 125 | 5962-9675101QDA | View Contents | 1KU \| 7.29 | 1 |

**TI INVENTORY STATUS**
As Of 09:00 AM GMT, 17 Apr 2003

| IN STOCK | IN PROGRESS QTY \| DATE | LEAD TIME |
|---|---|---|
| 270* | >10k \| 20 May | 6 WKS |
| 42* | >10k \| 20 May | 6 WKS |
| 243* | >10k \| 20 May | 6 WKS |
| | | |
| 0* | 3580 \| 20 May | 6 WKS |
| | >10k \| 27 May | |
| 450* | >10k \| 20 May | 6 WKS |
| 46* | >10k \| 20 May | 6 WKS |

**REPORTED DISTRIBUTOR INVENTORY**
As Of 09:00 AM GMT, 17 Apr 2003

| DISTRIBUTOR COMPANY \| REGION | IN STOCK | PURCHASE |
|---|---|---|
| Avnet \| Americas | 562 | BUY NOW |
| None Reported View Distributors | | |
| Avnet-SILICA \| Europe | 175 | BUY NOW |
| EBV Electronik \| Europe | 50 | BUY NOW |
| None Reported View Distributors | | |
| | | |
| Avnet-SILICA \| Europe | 95 | BUY NOW |
| None Reported View Distributors | | |

**Table Data Updated on: 4/17/2003**

Product Folder: SN54LS73A, Dual J-K Flip-Flops With Clear and 3-state Outputs