

16-Bit Buffer/Line Driver with 3-State Outputs

GENERAL DESCRIPTION

The ML6516241 is a BiCMOS, 16-bit buffer/line driver with 3-state outputs. This device was specifically designed for high speed bus applications. Its 16 channels support propagation delay of 2.5ns maximum, and fast output enable and disable times of 7.0ns or less to minimize datapath delay.

This device is designed to minimize undershoot, overshoot, and ground bounce to decrease noise delays. These transceivers implement a unique digital and analog implementation to eliminate the delays and noise inherent in traditional digital designs. The device offers a new method for quickly charging up a bus load capacitor to minimize bus settling times, or FastBus™ Charge. FastBus Charge is a transition current, (specified as $I_{DYNAMIC}$) that injects between 60 to 200mA (depending on output load) of current during the rise time and fall time. This current is used to reduce the amount of time it takes to charge up a heavily-capacitive loaded bus, effectively reducing the bus settling times, and improving data/clock margins in tight timing budgets.

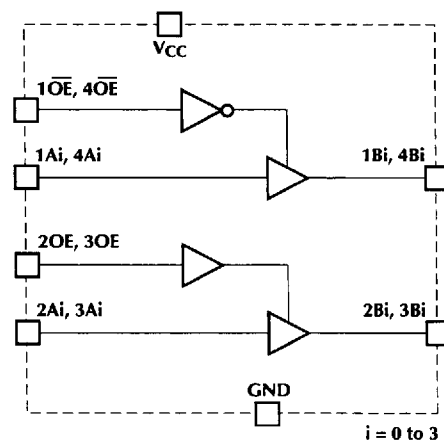
Micro Linear's solution is intended for applications for critical bus timing designs that include minimizing device propagation delay, bus settling time, and time delays due to noise. Applications include; high speed memory arrays, bus or backplane isolation, bus to bus bridging, and sub-2.5ns propagation delay schemes.

The ML6516241 follows the pinout and functionality of the industry standard 3.3V-logic families.

FEATURES

- Low propagation delays — 2.5ns maximum for 3.3V
2.25ns maximum for 5.0V
- Fast output enable/disable times of 7.0ns maximum
- FastBus Charge current to minimize the bus settling time during active capacitive loading
- 3.0 to 3.6V and 4.5 to 5.5V V_{CC} supply operation; LV-TTL compatible input and output levels with 3-state capability
- Industry standard pinout compatible to FCT, ALV, LCX, LVT, and other low voltage logic families
- ESD protection exceeds 2000V
- Full output swing for increased noise margin
- Undershoot and overshoot protection to 400mV typically
- Low ground bounce design

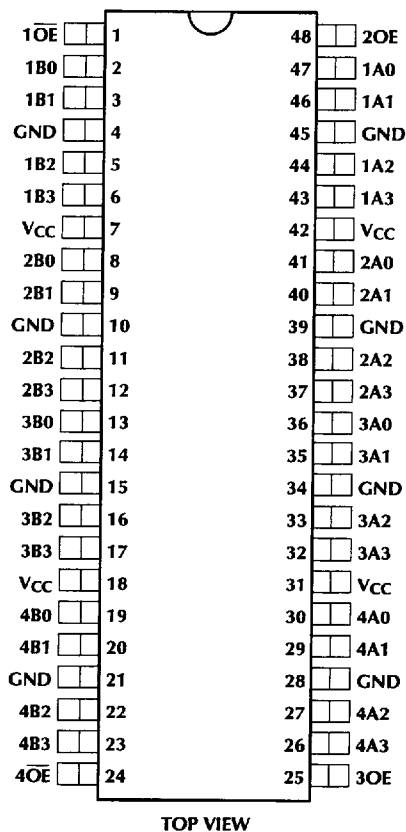
BLOCK DIAGRAM



ML6516241

PIN CONFIGURATION

ML6516241
48-Pin SSOP (R48)
48-Pin TSSOP (T48)



FUNCTION TABLE

(Each 4-bit section)

| INPUTS | | OUTPUTS |
|----------------------------------|----------|----------|
| $\overline{1OE}, \overline{4OE}$ | 1Ai, 4Ai | 1Bi, 4Bi |
| L | H | H |
| L | L | L |
| H | X | Z |

| INPUTS | | OUTPUTS |
|----------|----------|----------|
| 2OE, 3OE | 2Ai, 3Ai | 2Bi, 3Bi |
| H | H | H |
| H | L | L |
| L | X | Z |

L = Logic Low, H = Logic High, X = Don't Care, Z = High Impedance

i = 0 to 3

PIN DESCRIPTION

| PIN | NAME | FUNCTION | PIN | NAME | FUNCTION |
|-----|-------------------|--------------------------|-----|-----------------|---------------------------|
| 1 | 1 \overline{OE} | Output Enable Active Low | 25 | 3OE | Output Enable Active High |
| 2 | 1B0 | Data Output | 26 | 4A3 | Data Input |
| 3 | 1B1 | Data Output | 27 | 4A2 | Data Input |
| 4 | GND | Signal Ground | 28 | GND | Signal Ground |
| 5 | 1B2 | Data Output | 29 | 4A1 | Data Input |
| 6 | 1B3 | Data Output | 30 | 4A0 | Data Input |
| 7 | V _{CC} | 3.3V or 5.0V Supply | 31 | V _{CC} | 3.3V or 5.0V Supply |
| 8 | 2B0 | Data Output | 32 | 3A3 | Data Input |
| 9 | 2B1 | Data Output | 33 | 3A2 | Data Input |
| 10 | GND | Signal Ground | 34 | GND | Signal Ground |
| 11 | 2B2 | Data Output | 35 | 3A1 | Data Input |
| 12 | 2B3 | Data Output | 36 | 3A0 | Data Input |
| 13 | 3B0 | Data Output | 37 | 2A3 | Data Input |
| 14 | 3B1 | Data Output | 38 | 2A2 | Data Input |
| 15 | GND | Signal Ground | 39 | GND | Signal Ground |
| 16 | 3B2 | Data Output | 40 | 2A1 | Data Input |
| 17 | 3B3 | Data Output | 41 | 2A0 | Data Input |
| 18 | V _{CC} | 3.3V or 5.0V Supply | 42 | V _{CC} | 3.3V or 5.0V Supply |
| 19 | 4B0 | Data Output | 43 | 1A3 | Data Input |
| 20 | 4B1 | Data Output | 44 | 1A2 | Data Input |
| 21 | GND | Signal Ground | 45 | GND | Signal Ground |
| 22 | 4B2 | Data Output | 46 | 1A1 | Data Input |
| 23 | 4B3 | Data Output | 47 | 1A0 | Data Input |
| 24 | 4 \overline{OE} | Output Enable Active Low | 48 | 2OE | Output Enable Active High |

ML6516241

ABSOLUTE MAXIMUM RATINGS

Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

Storage Temperature Range -65°C to 150°C
 Junction Temperature 150°C
 Lead Temperature (Soldering, 10sec) 150°C
 Thermal Impedance (θ_{JA}) 76°C/W

V_{CC} 7V
 DC Input Voltage -0.3V to $V_{CC} + 0.3V$
 AC Input Voltage (PW < 20ns) -3.0V
 DC Output Voltage -0.3V to 7VDC
 Output Current, Source or Sink (AC) 180mA

OPERATING CONDITIONS

Temperature Range 0°C to 70°C
 V_{IN} Operating Range 3.0V to 5.5V

ELECTRICAL CHARACTERISTICS – 3.3V OPERATION

Unless otherwise specified, $V_{IN} = 3.3V$, $T_A =$ Operating Temperature Range (Note 1).

| SYMBOL | PARAMETER | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|--|-----|------|------|---------|
| AC ELECTRICAL CHARACTERISTICS ($C_{LOAD} = 50pF$) | | | | | | |
| t_{PHL}, t_{PLH} | Propagation Delay | Ai to Bi | 1.8 | 2.1 | 2.5 | ns |
| t_{OE} | Output Enable Time | OE to Ai | | | 7.0 | ns |
| t_{OD} | Output Disable Time | OE to Ai | | | 7.0 | ns |
| T_{OS} | Output-to-Output Skew | | | | 500 | ps |
| C_{IN} | Input Capacitance | | | | 5 | pF |
| DC ELECTRICAL CHARACTERISTICS ($C_{LOAD} = 50pF$, $R_{LOAD} =$ Open) | | | | | | |
| V_{IH} | Input High Voltage | Logic high | 2.0 | | | V |
| V_{IL} | Input Low Voltage | Logic low | | | 0.8 | V |
| I_{IH} | Input High Current | Per pin, $V_{IN} = 3V$ | | | 300 | μA |
| I_{IL} | Input Low Current | Per pin, $V_{IN} = 0V$ | | | 300 | μA |
| I_{HI-Z} | Three-State Output Current | $V_{CC} = 3.6V, 0 < V_{IN} < V_{CC}$ | | | 5 | μA |
| V_{IC} | Input Clamp Voltage | $V_{CC} = 3.6V, I_{IN} = 18mA$ | | -0.7 | -0.2 | V |
| $I_{DYNAMIC}$ | Dynamic Transition Current (FastBus Charge) | Low to high transitions | | 80 | | mA |
| | | High to low transitions | | 80 | | mA |
| V_{OH} | Output High Voltage | $V_{CC} = 3.6V, I_{OH} = -2mA$ | 2.4 | | | V |
| V_{OL} | Output Low Voltage | $V_{CC} = 3.6V, I_{OL} = 2mA$ | | | 0.6 | V |
| I_{CC} | Quiescent Power Supply Current | $V_{CC} = 3.6V, f = 0Hz,$ inputs = V_{CC} or 0V | | | 3 | μA |

Note 1: Limits are guaranteed by 100% testing, sampling, or correlation with worst case test conditions.

ELECTRICAL CHARACTERISTICS – 5V OPERATION

Unless otherwise specified, $V_{IN} = 5V$, T_A = Operating Temperature Range (Note 1).

| SYMBOL | PARAMETER | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|--|--|-----|------|------|---------|
| AC ELECTRICAL CHARACTERISTICS ($C_{LOAD} = 50pF$) | | | | | | |
| t_{PHL}, t_{PLH} | Propagation Delay | Ai to Bi | 1.6 | 1.9 | 2.25 | ns |
| t_{OE} | Output Enable Time | OE to Ai | | | 7.0 | ns |
| t_{OD} | Output Disable Time | OE to Ai | | | 7.0 | ns |
| T_{OS} | Output-to-Output Skew | | | | 500 | ps |
| C_{IN} | Input Capacitance | | | | 5 | pF |
| DC ELECTRICAL CHARACTERISTICS ($C_{LOAD} = 50pF$, $R_{LOAD} = \text{Open}$) | | | | | | |
| V_{IH} | Input High Voltage | Logic high | 3.6 | | | V |
| V_{IL} | Input Low Voltage | Logic low | | | 0.8 | V |
| I_{IH} | Input High Current | Per pin, $V_{IN} = 4.5V$ | | | 300 | μA |
| I_{IL} | Input Low Current | Per pin, $V_{IN} = 0V$ | | | 300 | μA |
| I_{HI-Z} | Three-State Output Current | $V_{CC} = 5.5V, 0 < V_{IN} < V_{CC}$ | | | 5 | μA |
| V_{IC} | Input Clamp Voltage | $V_{CC} = 5.5V, I_{IN} = 18mA$ | | -0.7 | -0.2 | V |
| $I_{DYNAMIC}$ | Dynamic Transition Current (FastBus Charge) | Low to high transitions | | 120 | | mA |
| | | High to low transitions | | 120 | | mA |
| V_{OH} | Output High Voltage | $V_{CC} = 5.5V, I_{OH} = -2mA$ | 4.5 | | | V |
| V_{OL} | Output Low Voltage | $V_{CC} = 5.5V, I_{OL} = 2mA$ | | | 1.2 | V |
| I_{CC} | Quiescent Power Supply Current | $V_{CC} = 5.5V, f = 0Hz,$ inputs = V_{CC} or $0V$ | | | 3 | μA |

Note 1: Limits are guaranteed by 100% testing, sampling, or correlation with worst case test conditions.

PERFORMANCE DATA 3.3V OPERATION

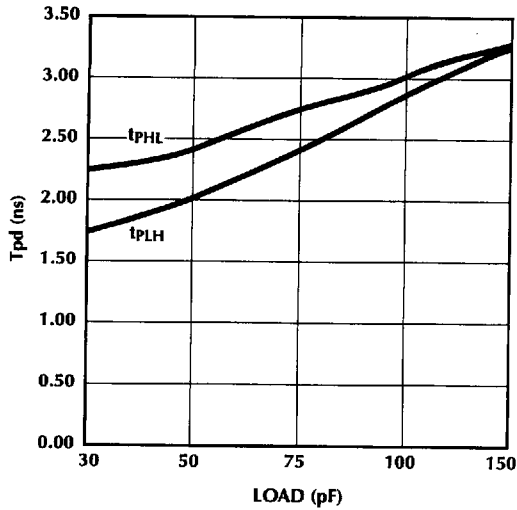


Figure 1. Propagation Delay over Load Capacitance: 30 to 150pF, $V_{CC} = V_{IN} = 3.3V$, 20MHz

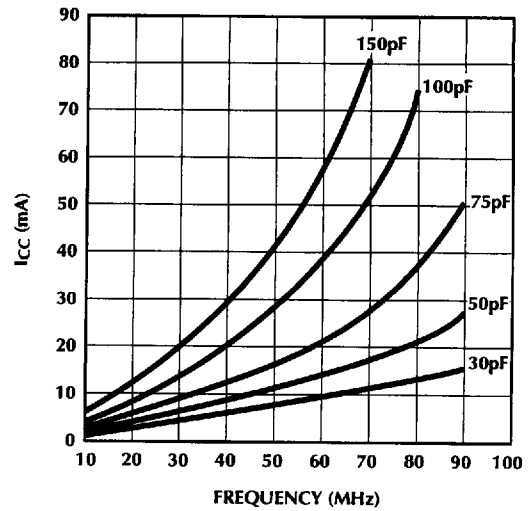


Figure 2. I_{CC} vs. Frequency (10 to 100 MHz) over Load, $V_{CC} = V_{IN} = 3.3V$

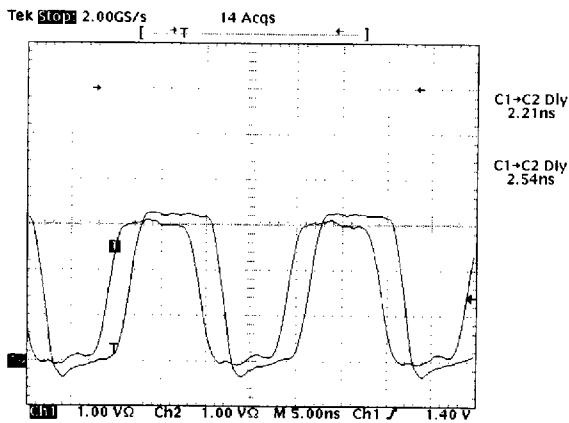


Figure 3. Ground Bounce:
 $V_{CC} = V_{IN} = 3.0V$
 V_{IN} : $t_{RISE} = t_{FALL} = 2ns$

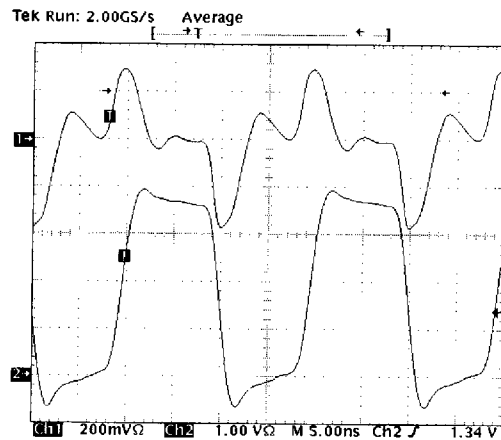


Figure 4. $I_{DYNAMIC}$ Current (FastBus Charge):
 $V_{CC} = V_{IN} = 3.3V$, 50pF load,
40mA/DIV, V_{IN} : $t_{RISE} = t_{FALL} = 2ns$

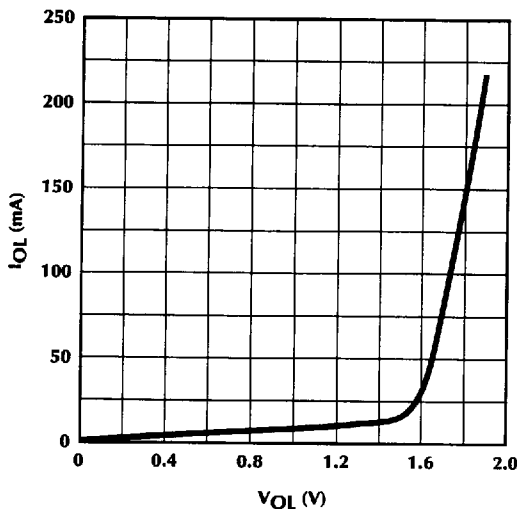


Figure 5a. Typical V_{OL} vs. I_{OL} for One Buffer Output

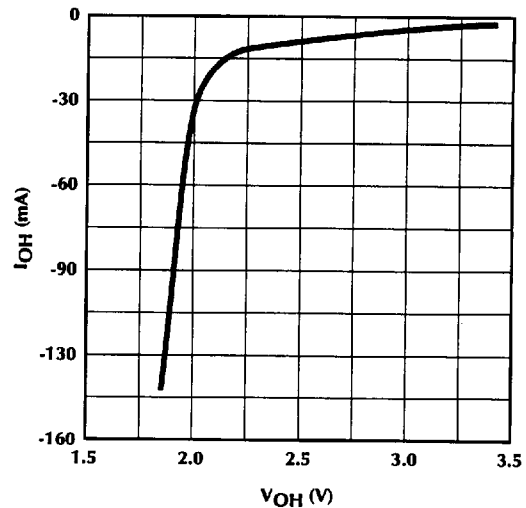


Figure 5b. Typical V_{OH} vs. I_{OH} for One Buffer Output

PERFORMANCE DATA 5.0V OPERATION

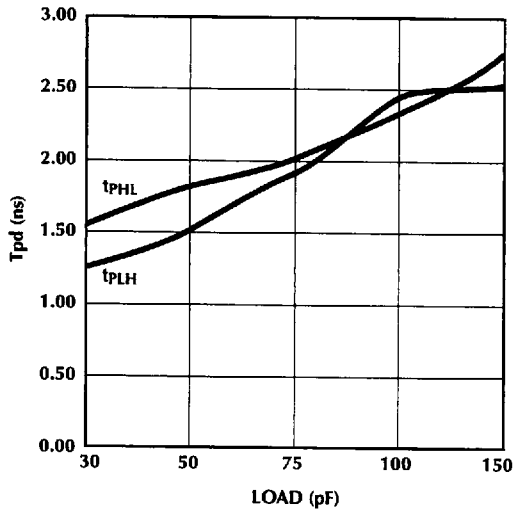


Figure 6. Propagation Delay over Load Capacitance: 30 to 150pF, V_{CC} = V_{IN} = 5.0V, 20MHz

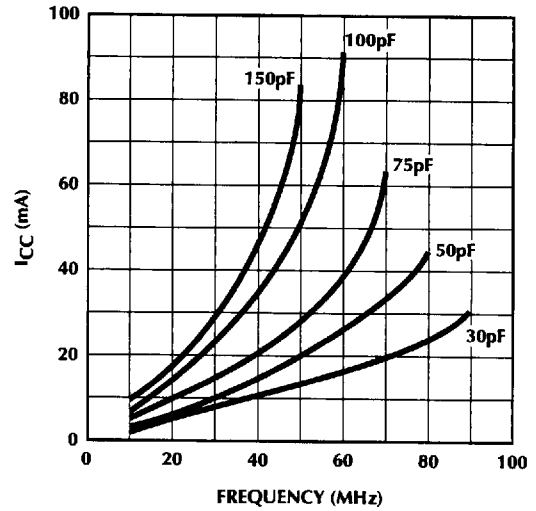


Figure 7. I_{CC} vs. Frequency (10 to 100 MHz) over Load, V_{CC} = V_{IN} = 5.0V

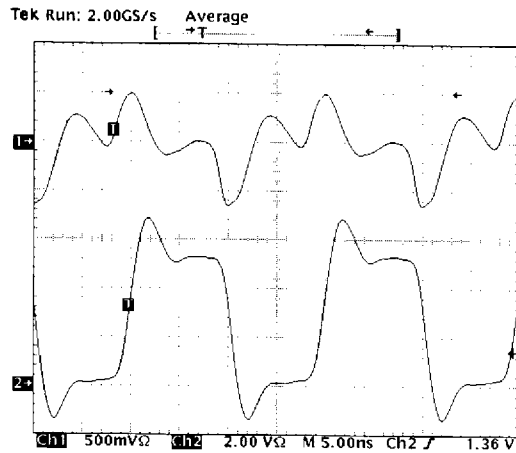


Figure 8. I_{DYNAMIC} Current (FastBus Charge): V_{CC} = V_{IN} = 5.0V, 50pF load, 100mA/DIV, V_{IN}: t_{RISE} = t_{FALL} = 2ns

FUNCTIONAL DESCRIPTION

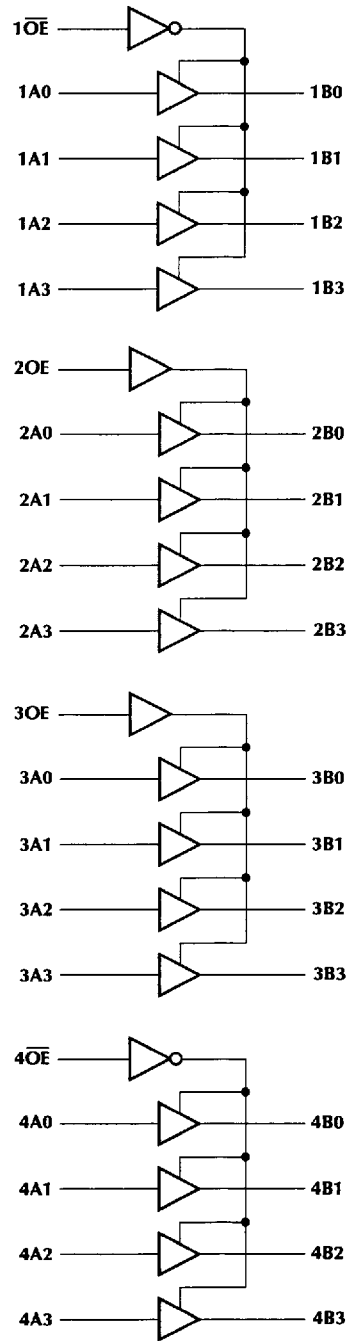


Figure 9. Logic Diagram

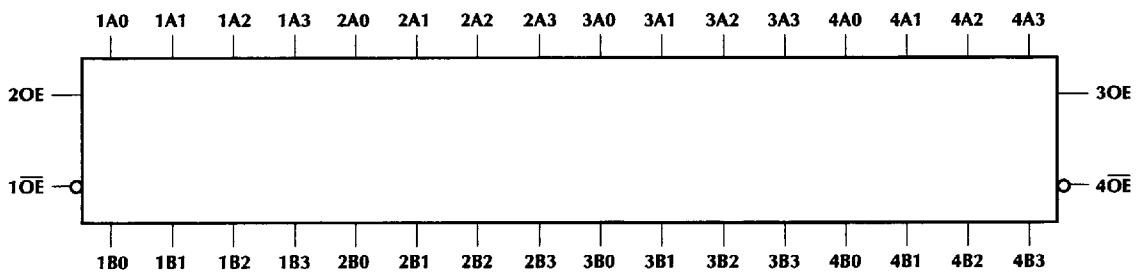


Figure 10. Logic Symbol

ARCHITECTURAL DESCRIPTION

The ML6516241 is a 16-bit buffer/line driver with 3-state outputs designed for 3.0V to 3.6V and 4.5V to 5.5V V_{CC} operation. This device is designed for Quad-Nibble, Dual-Byte memory interleaving operations. Each bank has an independently controlled 3-state output enable pin with output enable/disable access times of less than 7.0ns. Each bank is configured to have four independent buffer/line drivers. Two banks are active high enabled and the other two banks are active low enabled. Thus making this device ideal for nibble or byte swapping operations in cache or main memory designs by toggling between the active low and active high output enable pins.

Until now, these transceivers were typically implemented in CMOS logic and made to be TTL compatible by sizing the input devices appropriately. In order to buffer large capacitances with CMOS logic, it is necessary to cascade an even number of inverters, each successive inverter larger than the preceding, eventually leading to an inverter that will drive the required load capacitance at the required frequency. Each inverter stage represents an additional delay in the gating process because in order for a single gate to switch, the input must slew more than half of the supply voltage. The best of these 16-bit CMOS buffers has managed to drive 50pF load capacitance with a delay of 3.6ns.

Micro Linear has produced a 16-bit buffer/line driver with a delay less than 2.5ns by using a unique circuit architecture that does not require cascade logic gates.

The basic architecture of the ML6516241 is shown in Figure 11. In this circuit, there are two paths to the output. One path sources current to the load capacitance where the signal is asserted, and the other path sinks current from the output when the signal is negated.

The assertion path is the Darlington pair consisting of transistors Q1 and Q2. The effect of transistor Q1 is to increase the current gain through the stage from input to output, to increase the input resistance and to reduce input capacitance. During an input low-to-high transition, the output transistor Q2 sources large amount of current to quickly charge up a highly capacitive load which in effect reduces the bus settling time. This current is specified as $I_{DYNAMIC}$.

The negation path is also the Darlington pair consisting of transistor Q3 and transistor Q4. With M1 connecting to the input of the Darlington pair, Transistor Q4 then sinks a large amount of current during the input transition from high-to-low.

Inverter X2 is a helpful buffer that not only drives the output toward the upper rail but also pulls the output to the lower rail.

There are a number of MOSFETs not shown in Figure 3. These MOSFETs are used to 3-state the buffers. For instance, R1 and R2 were implemented as resistive transmission gates to ensure that disabled buffers do not load the lines of which they are connected.

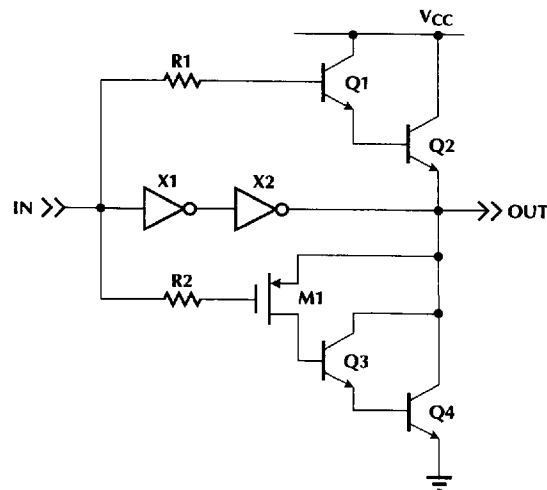


Figure 11. One Buffer Cell of the ML6516241

CIRCUITS AND WAVE FORMS

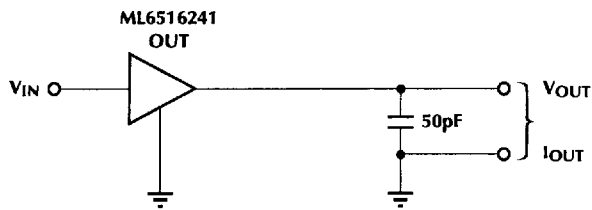


Figure 12. Test circuits for All Outputs

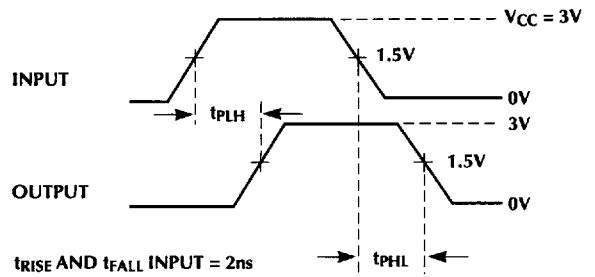


Figure 13. Propagation Delay

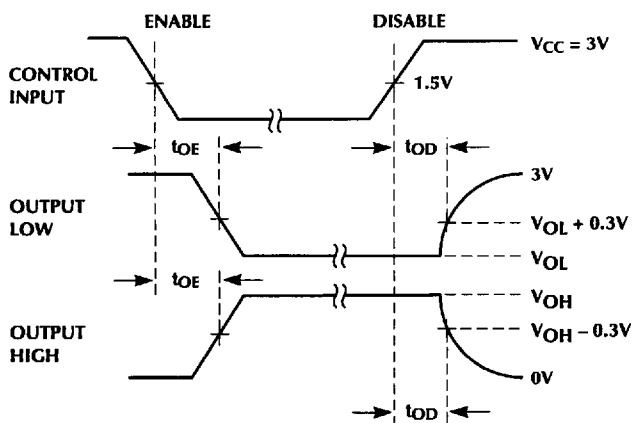


Figure 14. Enable and Disable Times

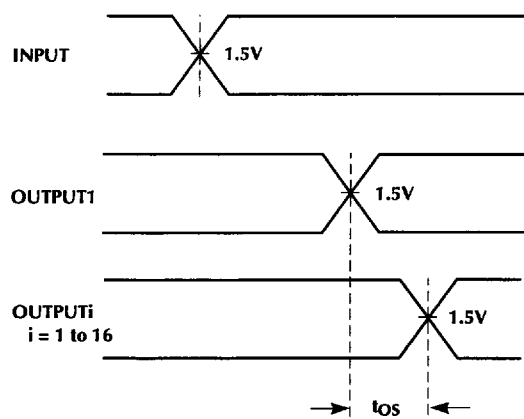
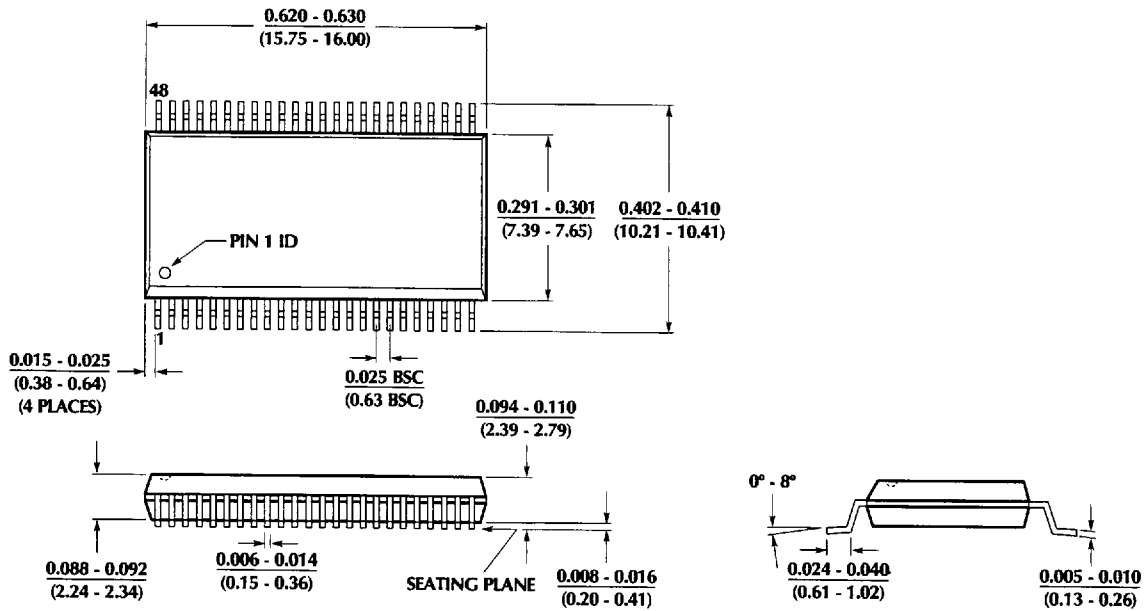


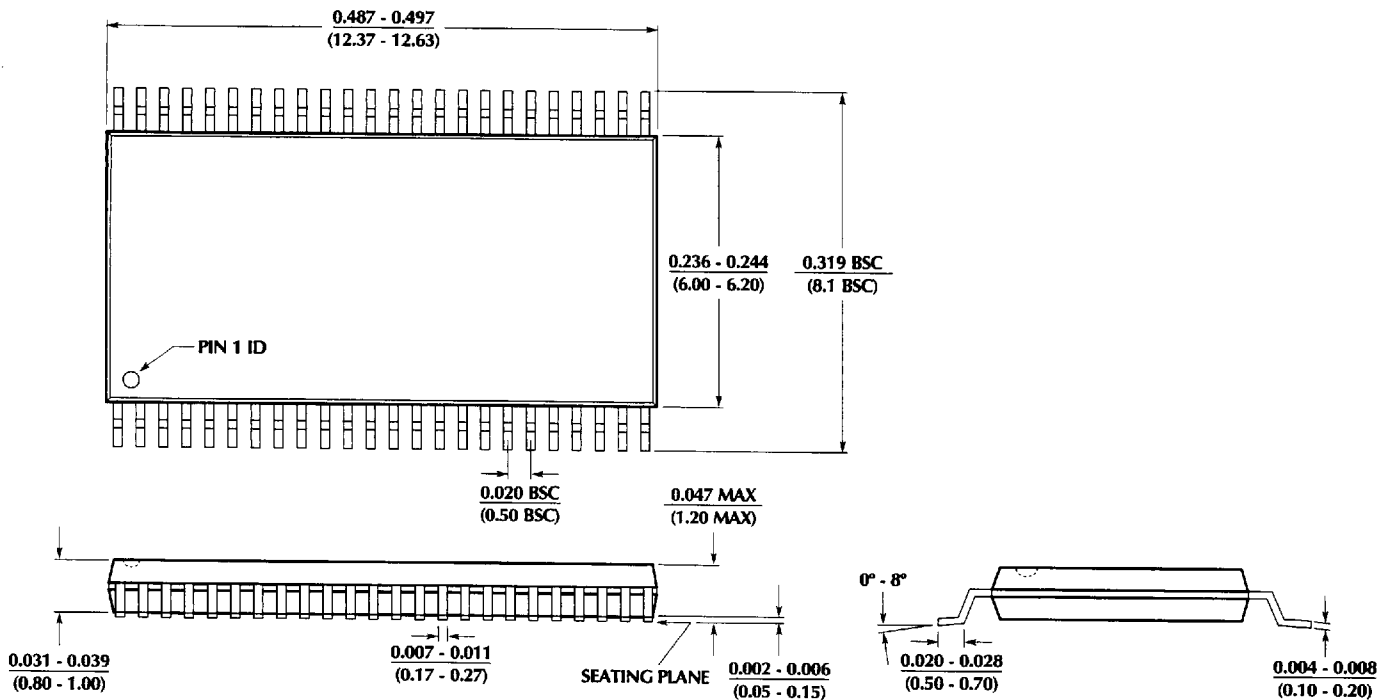
Figure 15. Output Skew

PHYSICAL DIMENSIONS inches (millimeters)

Package: R48
48-Pin SSOP




Package: T48
48-Pin TSSOP



ORDERING INFORMATION

| PART NUMBER | TEMPERATURE RANGE | PACKAGE |
|-------------|-------------------|--------------------|
| ML6516241CR | 0°C to 70°C | 48-Pin SSOP (R48) |
| ML6516241CT | 0°C to 70°C | 48-Pin TSSOP (T48) |

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