Octal buffer/line driver; 3-state

74LVC244

FEATURES

- Wide supply voltage range of 1.2 V to 3.6 V
- In accordance with JEDEC standard no. 8-1A.
- Inputs accept voltages up to 5.5 V
- CMOS low power consumption
- Direct interface with TTL levels
- Output drive capability 50 Ω transmission lines @ 85 °C

DESCRIPTION

The 74LVC244 is a high-performance, low-power, low-voltage, Si-gate CMOS device and superior to most advanced CMOS compatible TTL families.

Inputs can be driven from either 3.3 V or 5 V devices. This feature allows the use of these devices as translators in a mixed 3.3 V/5 V environment

The 74LVC244 is an octal non-inverting buffer/line driver with 3-state outputs. The 3-state outputs are controlled by the output enable inputs 1$\overline{OE}$ and 2$\overline{OE}$. A HIGH on n$\overline{OE}$ causes the outputs to assume a high impedance OFF-state. Schmitt-trigger action at all inputs makes the circuit highly tolerant for slower input rise and fall times. The '244' is identical to the '240' but has non-inverting outputs.

FUNCTION TABLE

INPUTS		OUTPUT
n$\overline{OE}$	nA_n	nY_n
L	L	L
L	H	H
H	X	Z

H = HIGH voltage level
L = LOW voltage level
X = don't care
Z = high impedance OFF-state

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; t_r = t_f ≤ 2.5 ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	propagation delay 1A_n to 1Y_n; 2A_n to 2Y_n	C_L = 50 pF V_{CC} = 3.3 V	4.9	ns
C_I	input capacitance		5.0	pF
C_{PD}	power dissipation capacitance per buffer	notes 1 and 2	30	pF

Notes to the quick reference data

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW)
$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$
f_i = input frequency in MHz; C_L = output load capacity in pF;
f_o = output frequency in MHz; V_{CC} = supply voltage in V;
$\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is V_I = GND to V_{CC}

ORDERING INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74LVC244D	20	SO	plastic	SOT163-1
74LVC244DB	20	SSOP	plastic	SOT339-1
74LVC244PW	20	TSSOP	plastic	SOT360-1

PINNING

PIN NO.	SYMBOL	NAME AND FUNCTION
1	1$\overline{OE}$	output enable input (active LOW)
2, 4, 6, 8	1A_0 to 1A_3	data inputs
3, 5, 7, 9	2Y_0 to 2Y_3	bus outputs
10	GND	ground (0 V)
17, 15, 13, 11	2A_0 to 2A_3	data inputs
18, 16, 14, 12	1Y_0 to 1Y_3	bus outputs
19	2$\overline{OE}$	output enable input (active LOW)
20	V_{CC}	positive power supply
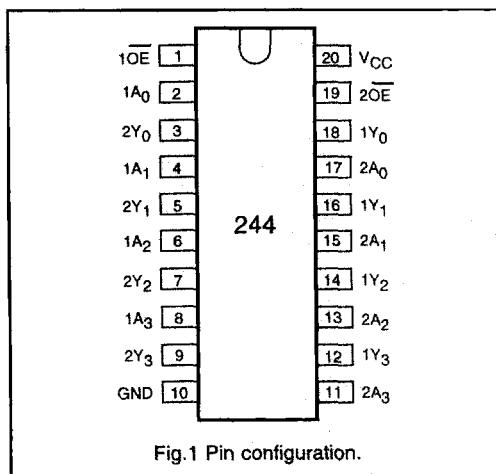
Fig.1 Pin configuration.
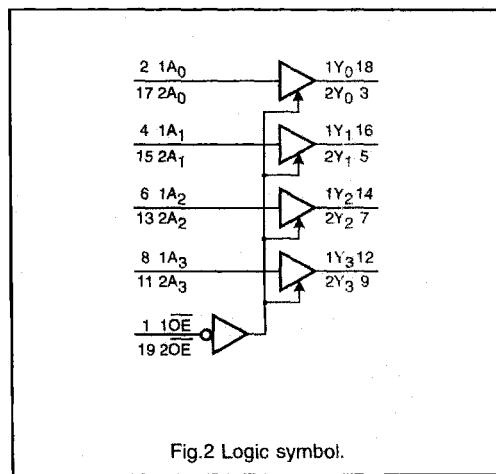
Fig.2 Logic symbol.
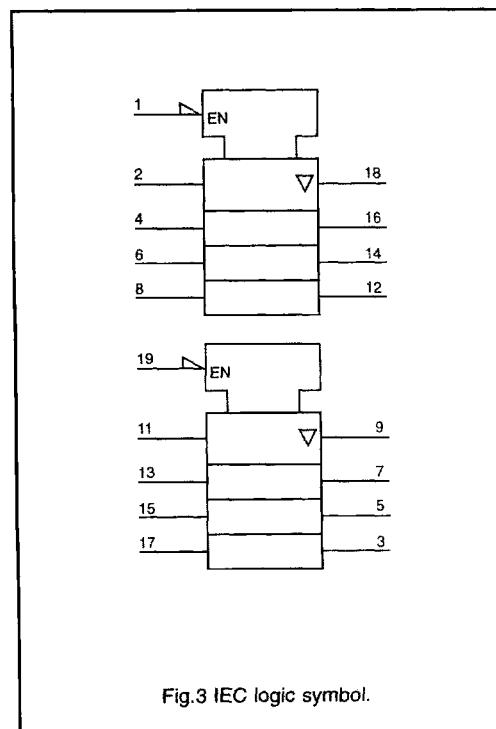
Fig.3 IEC logic symbol.
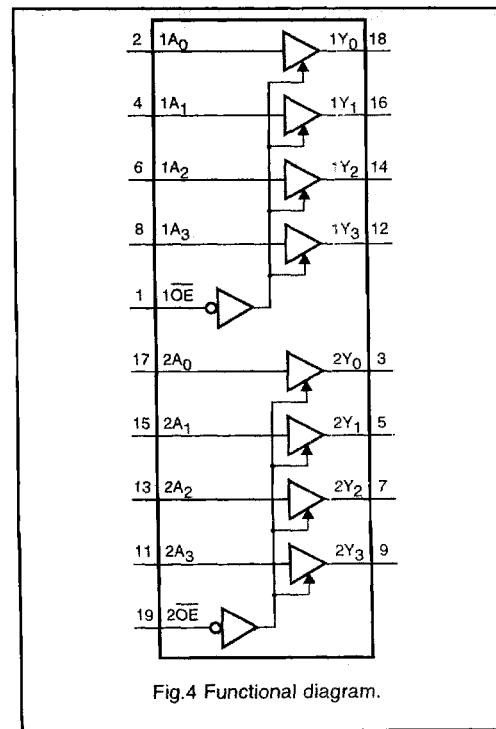
Fig.4 Functional diagram.

Octal buffer/line driver; 3-state

74LVC244

DC CHARACTERISTICS FOR 74LVC244

For the DC characteristics see chapter "LVC family characteristics", section "Family specifications".
I_{CC} category: MSI

### AC CHARACTERISTICS FOR 74LVC244

GND = 0 V; $t_r = t_f \leq 2.5$ ns; $C_L = 50$ pF

SYMBOL	PARAMETER	T_{amb} (°C) -40 to +85			UNIT	TEST CONDITIONS	
		MIN.	TYP.	MAX.		V_{CC} (V)	WAVEFORMS
t_{PHL}/t_{PLH}	propagation delay	–	21	–	ns	1.2	
	$1A_n$ to $1Y_n$;	1.5	5.2	8.0		2.7	Figs 5, 7
	$2A_n$ to $2Y_n$	1.5	4.9*	7.0		3.0 to 3.6	
t_{PZH}/t_{PZL}	3-state output enable time	–	45	–	ns	1.2	
	$1\overline{OE}$ to $1Y_n$;	1.5	6.1	10.0		2.7	Figs 6, 7
	$2\overline{OE}$ to $2Y_n$	1.5	5.8*	8.0		3.0 to 3.6	
t_{PHZ}/t_{PLZ}	3-state output disable time	–	5.8	–	ns	1.2	
	$1\overline{OE}$ to $1Y_n$;	1.5	3.5	8.5		2.7	Figs 6, 7
	$2\overline{OE}$ to $2Y_n$	1.5	3.3*	7.5		3.0 to 3.6	

Notes: All typical values are measured at T_{amb} = 25 °C.
* Typical values are measured at V_{CC} = 3.3 V.
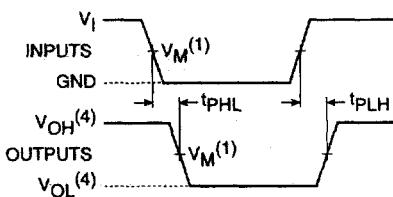
AC WAVEFORMS

Fig.5 Waveforms showing the input (1A$_n$, 2A$_n$) to output (1Y$_n$, 2Y$_n$) propagation delays.
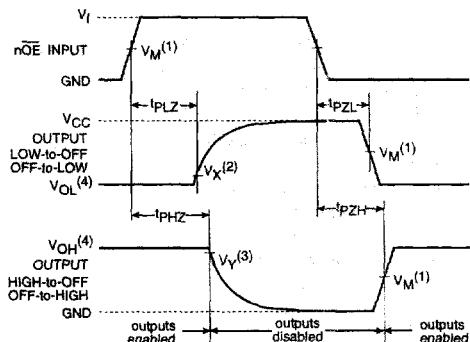
Fig.6 Waveforms showing the 3-state enable and disable times.

Fig.7 Load circuitry for switching times.

V$_{CC}$	V$_I$
< 2.7 V	V$_{CC}$
2.7 - 3.6 V	2.7 V

Test	S$_1$
t$_{PLH}$/t$_{PHL}$	Open
t$_{PLZ}$/t$_{PZL}$	2 · V$_{CC}$
t$_{PHZ}$/t$_{PZH}$	GND

Notes:
(1) V$_M$ = 0.5 · V$_{CC}$ at V$_{CC}$ < 2.7 V
    V$_M$ = 1.5 V at V$_{CC}$ ≥ 2.7 V
(2) V$_X$ = V$_{OL}$ + 0.3 V at V$_{CC}$ ≥ 2.7 V
    V$_X$ = V$_{OL}$ + 0.1 · V$_{CC}$ at V$_{CC}$ < 2.7 V
(3) V$_Y$ = V$_{OH}$ − 0.3 V at V$_{CC}$ ≥ 2.7 V
    V$_Y$ = V$_{OH}$ − 0.1 · V$_{CC}$ at V$_{CC}$ < 2.7 V
(4) V$_{OL}$ and V$_{OH}$ are the typical output voltage drop that occur with the output load.