MOTOROLA

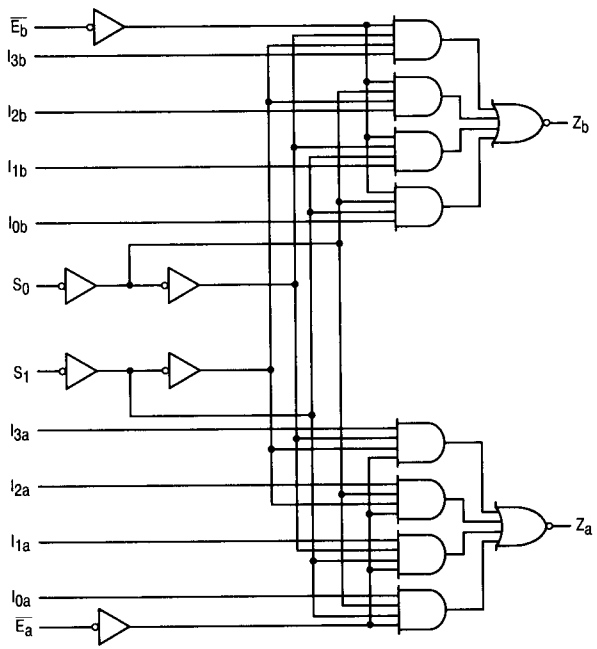
Dual 4-Input Data Selector/ Multiplexer With Inverted Outputs

ELECTRICALLY TESTED PER:
MIL-M-38510/33909

The 54F352 is a very high-speed dual 4-input multiplexer with common Select inputs and individual Enable inputs for each section. It can select two bits of data from four sources. The two buffered outputs present data in the inverted (complementary) form. The 'F352 is the functional equivalent of the 'F153 except with inverted outputs.

- Inverted Version of 'F153
- Separate Enable For Each Multiplexer
- Input Clamp Diode Limits High Speed Termination Effects

LOGIC DIAGRAM



Military 54F352

AVAILABLE AS:

1) JAN: JM38510/33909BXA
2) SMD: N/A
3) 883: 54F352/BXAJC

X = CASE OUTLINE AS FOLLOWS:
PACKAGE: CERDIP: E
CERFLAT: F
LCC: 2

THE LETTER "M" APPEARS BEFORE THE / ON LCC.

PIN ASSIGNMENTS

FUNCT.	DIL 620-09	FLATS 650-05	LCC 756A-02	BURN-IN (COND. A)
$\overline{E}_a$	1	1	2	V_{CC}
S_1	2	2	3	V_{CC}
I_{3a}	3	3	4	V_{CC}
I_{2a}	4	4	5	V_{CC}
I_{1a}	5	5	7	V_{CC}
I_{0a}	6	6	8	V_{CC}
$\overline{Z}_a$	7	7	9	OPEN
GND	8	8	10	GND
$\overline{Z}_b$	9	9	12	OPEN
I_{0b}	10	10	13	V_{CC}
I_{1b}	11	11	14	V_{CC}
I_{2b}	12	12	15	V_{CC}
I_{3b}	13	13	17	V_{CC}
S_0	14	14	18	V_{CC}
$\overline{E}_b$	15	15	19	V_{CC}
V_{CC}	16	16	20	V_{CC}

BURN-IN CONDITIONS:
V_{CC} = 5.0 V MIN/6.0 V MAX

4

FUNCTIONAL DESCRIPTION

The 'F352 is a dual 4-input multiplexer. It selects two bits of data from up to four sources under the control of the common Select inputs (S_0, S_1). The two 4-input multiplexer circuits have individual active-LOW Enables ($\overline{E_a}$, $\overline{E_b}$) which can be used to strobe the outputs independently. When the Enables ($\overline{E_a}$, $\overline{E_b}$) are HIGH, the corresponding outputs ($\overline{Z_a}$, $\overline{Z_b}$) are forced HIGH.

The 'F352 can be used to move data from a group of registers to a common output bus. The particular register from which the data came would be determined by the state of the select inputs. A less obvious application is as a function generator. The 'F352 can generate two functions of three variables. This is useful for implementing highly irregular random logic.

The logic equations for the outputs are shown below:

$$\overline{Z_a} = E_a \bullet (I_{0a} \bullet \overline{S_1} \bullet \overline{S_0} + I_{1a} \bullet \overline{S_1} \bullet S_0 + I_{2a} \bullet S_1 \bullet \overline{S_0} + I_{3a} \bullet S_1 \bullet S_0)$$

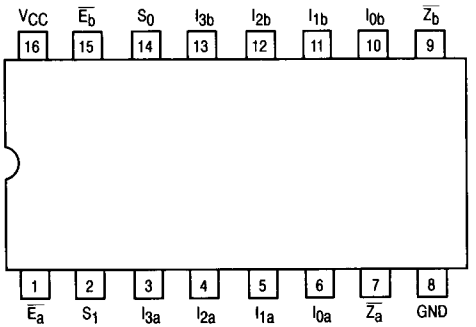
$$\overline{Z_b} = E_b \bullet (I_{0b} \bullet \overline{S_1} \bullet \overline{S_0} + I_{1b} \bullet \overline{S_1} \bullet S_0 + I_{2b} \bullet S_1 \bullet \overline{S_0} + I_{3b} \bullet S_1 \bullet S_0)$$

TRUTH TABLE

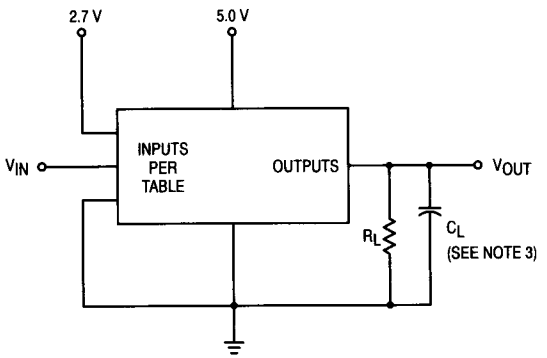
Select Inputs		Inputs (a or b)					Output
S_0	S_1	$\overline{E}$	I_0	I_1	I_2	I_3	$\overline{Z}$
X	X	H	X	X	X	X	H
L	L	L	L	X	X	X	H
L	L	L	H	X	X	X	L
H	L	L	X	L	X	X	H
H	L	L	X	H	X	X	L
L	H	L	X	X	L	X	H
L	H	L	X	X	H	X	L
H	H	L	X	X	X	L	H
H	H	L	X	X	X	H	L

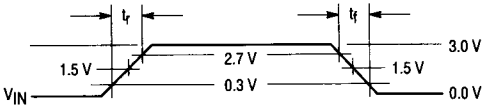
H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

CONNECTION DIAGRAM



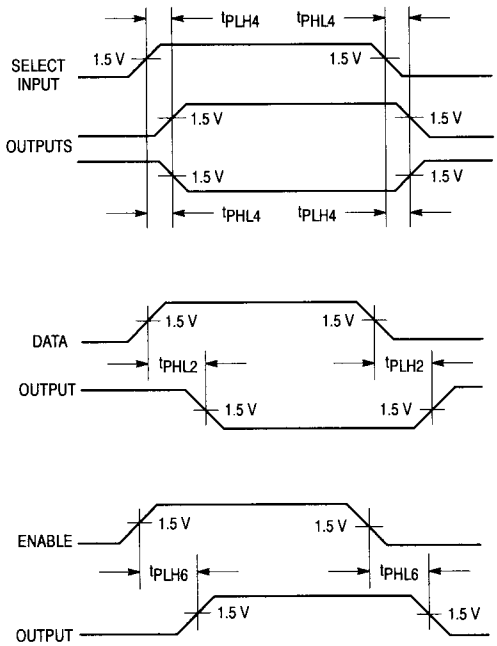
AC TEST CIRCUIT





REFERENCE NOTES ON PAGE 4-153

WAVEFORMS



NOTES:

1. V_{IN} input pulse has the following characteristics: $t_r = t_f \leq 2.5$ ns, PRR ≤ 1.0 MHz, $Z_{OUT} \approx 50\ \Omega$.
2. Terminal conditions (pins not designated may be high ≥ 2.0 V, low ≤ 0.8 V, or open.
3. $C_L = 50$ pF $\pm$ 10%, including scope probe, wiring and stray capacitance without package in test fixture.
4. Voltage measurements are to be made with respect to network ground terminal.
5. $R_L = 499\ \Omega \pm 5.0\%$.

Symbol	Parameter	Limits						Unit	Test Condition (Unless Otherwise Specified)
	Static Parameters:	+ 25°C		+ 125°C		− 55°C			
		Subgroup 1		Subgroup 2		Subgroup 3			
		Min	Max	Min	Max	Min	Max		
V_{OH}	Logical "1" Output Voltage	2.5		2.5		2.5		V	V_{CC} = 4.5 V, I_{OH} = −1.0 mA, V_{IL} = 0.8 V, other inputs are open, $\overline{E}_{a/b}$ = 0.8 V/2.0 V, $S_{1/0}$ = 0.8 V/2.0 V.
V_{OL}	Logical "0" Output Voltage		0.5		0.5		0.5	V	V_{CC} = 4.5 V, I_{OL} = 20 mA, V_{IH} = 2.0 V, other inputs are open, $\overline{E}_{a/b}$ = 0.8 V/open, $S_{1/0}$ = 0.8 V/2.0 V.
V_{IC}	Input Clamping Voltage		−1.2					V	V_{CC} = 4.5 V, I_{IN} = −18 mA, other inputs are open.
I_{IH}	Logical "1" Input Current		20		20		20	µA	V_{CC} = 5.5 V, V_{IH} = 2.7 V, other inputs are open, $\overline{E}_{a/b}$ = 4.5 V or (2.7 V), $S_{1/0}$ = 0 V, 4.5 V or (2.7 V).
I_{IHH}	Logical "1" Input Current		100		100		100	µA	V_{CC} = 5.5 V, V_{IHH} = 7.0 V, other inputs are open, $\overline{E}_{a/b}$ = 4.5 V or (7.0 V), $S_{1/0}$ = 0.7 V, 0 V or (4.5 V).
I_{OD}	Diode Current	60		60		60		mA	V_{CC} = 4.5 V, V_{IN} = 5.5 V, other inputs are open, $\overline{E}_{a/b}$ & $S_{1/0}$ = 0 V, V_{OUT} = 2.5 V.
I_{IL}	Logical "0" Input Current	−0.03	−0.6	−0.03	−0.6	−0.03	−0.6	mA	V_{CC} = 5.5 V, V_{IN} = 0.5 V, other inputs are open, $\overline{E}_{a/b}$ = 0 V or (0.5 V), $S_{1/0}$ = 0 V, 4.5 V or (0.5 V).
I_{OS}	Output Short Circuit Current	−60	−150	−60	−150	−60	−150	mA	V_{CC} = 5.5 V, V_{IN} = 0 V, other inputs are open, V_{OUT} = 0 V, $\overline{E}_{a/b}$ & $S_{1/0}$ = 0 V.
I_{CCH}	Power Supply Current		14		14		14	mA	V_{CC} = 5.5 V, V_{IN} = 0 V (all inputs).
I_{CCL}	Power Supply Current Off		20		20		20	mA	V_{CC} = 5.5 V, V_{IN} = 4.5 V (all inputs), $\overline{E}_{a/b}$ & $S_{1/0}$ = 0 V.
V_{IH}	Logical "1" Input Voltage	2.0		2.0		2.0		V	V_{CC} = 4.5 V.
V_{IL}	Logical "0" Input Voltage		0.8		0.8		0.8	V	V_{CC} = 4.5 V.
	Functional Tests	Subgroup 7		Subgroup 8A		Subgroup 8B			per Truth Table with V_{CC} = 4.5 V, (**Repeat at**) V_{CC} = 5.5 V, V_{INL} = 0.5 V, and V_{INH} = 2.5 V.

4

Symbol	Parameter	Limits						Unit	Test Condition (Unless Otherwise Specified)
	Switching Parameters:	+ 25°C		+ 125°C		− 55°C			
		Subgroup 9		Subgroup 10		Subgroup 11			
		Min	Max	Min	Max	Min	Max		
t_{PHL2}	Propagation Delay /Data-Output I_n to $\overline{Z}_n$	1.7	6.0	1.5	7.5	1.5	7.5	ns	V_{CC} = 5.0 V, C_L = 50 pF, $R_1 = R_2$ = 499 Ω.
t_{PLH2}	Propagation Delay /Data-Output I_n to $\overline{Z}_n$	2.0	7.0	2.0	9.0	2.0	9.0	ns	V_{CC} = 5.0 V, C_L = 50 pF, $R_1 = R_2$ = 499 Ω.
t_{PHL4}	Propagation Delay /Data-Output S_n to $\overline{Z}_n$	3.5	13	3.5	15	3.5	15	ns	V_{CC} = 5.0 V, C_L = 50 pF, $R_1 = R_2$ = 499 Ω.
t_{PLH4}	Propagation Delay /Data-Output S_n to $\overline{Z}_n$	3.5	13	3.5	14.5	3.5	14.5	ns	V_{CC} = 5.0 V, C_L = 50 pF, $R_1 = R_2$ = 499 Ω.
t_{PHL6}	Propagation Delay /Data-Output $\overline{E}_n$ to $\overline{Z}_n$	3.0	11	3.5	13	3.5	13	ns	V_{CC} = 5.0 V, C_L = 50 pF, $R_1 = R_2$ = 499 Ω.
t_{PLH6}	Propagation Delay /Data-Output $\overline{E}_n$ to $\overline{Z}_n$	3.5	14	3.5	17	3.5	17	ns	V_{CC} = 5.0 V, C_L = 50 pF, $R_1 = R_2$ = 499 Ω.