PI74ALVCH16524

18-Bit Registered Bus Transceiver With 3-State Outputs

Product Features

- PI74ALVCH16524 is designed for low voltage operation
- V_{CC} = 2.3V to 3.6V
- Typical V_{OLP} (Output Ground Bounce)
  < 0.8V at V_{CC} = 3.3V, T_A = 25°C
- Typical V_{OHV} (Output V_{OH} Undershoot)
  < 2.0V at V_{CC} = 3.3V, T_A = 25°C
- Bus Hold retains last active bus state during 3-State eliminating the need for external pullup resistors
- Industrial operation at –40°C to +85°C
- Packages available:
  – 56-pin 240 mil wide plastic TSSOP (A)
  – 56-pin 300 mil wide plastic SSOP (V)

Product Description

Pericom Semiconductor's PI74ALVCH series of logic circuits are produced using the Company's advanced 0.5 micron CMOS technology, achieving industry leading speed.

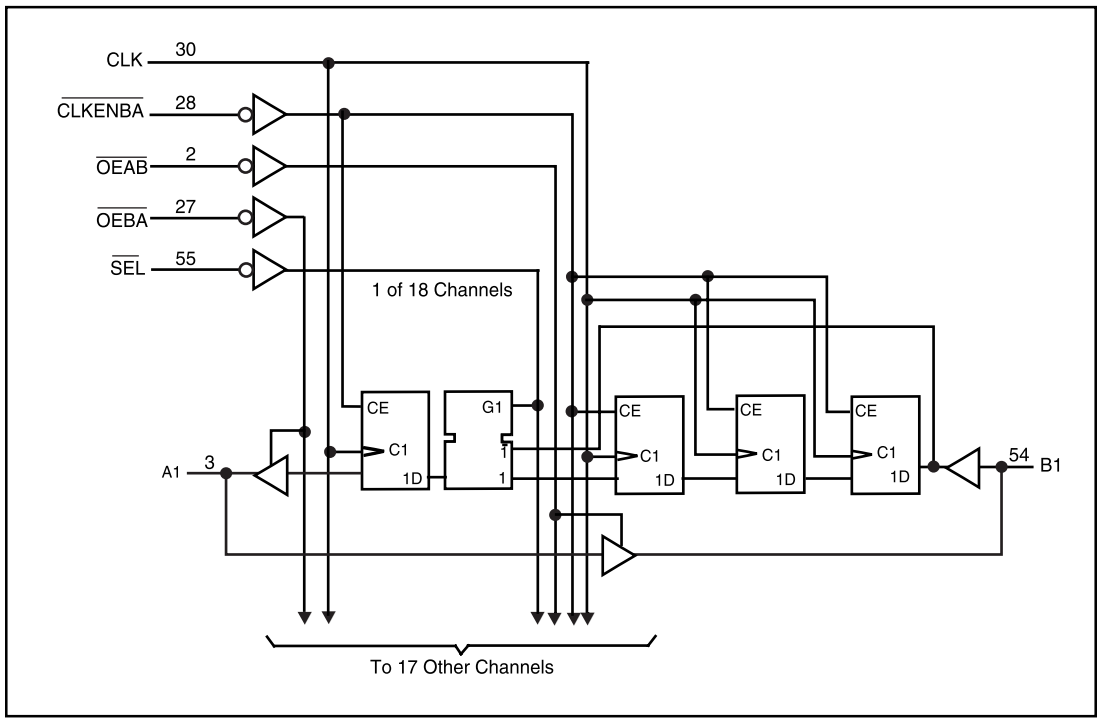
The PI74ALVCH16524 data flow in each direction is controlled by output-enable ($\overline{OEAB}$ and $\overline{OEBA}$) and clock-enable ($\overline{CLKENBA}$) inputs. For the A-to-B data flow, the data flows through a single buffer. The B-to-A data can flow through a four-stage pipeline register path, or through a single register path, depending on the state of the select ($\overline{SEL}$) input.

Data is stored in the internal registers on the low-to-high transition of the clock (CLK) input, provided that the appropriate $\overline{CLKENBA}$ input is low. The B-to-A data transfer is synchronized with CLK.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to Vcc through a pull-up resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The PI74ALVCH16524 has "Bus Hold" which retains the data input's last state whenever the data input goes to high-impedance preventing "floating" inputs and eliminating the need for pullup/down resistors.

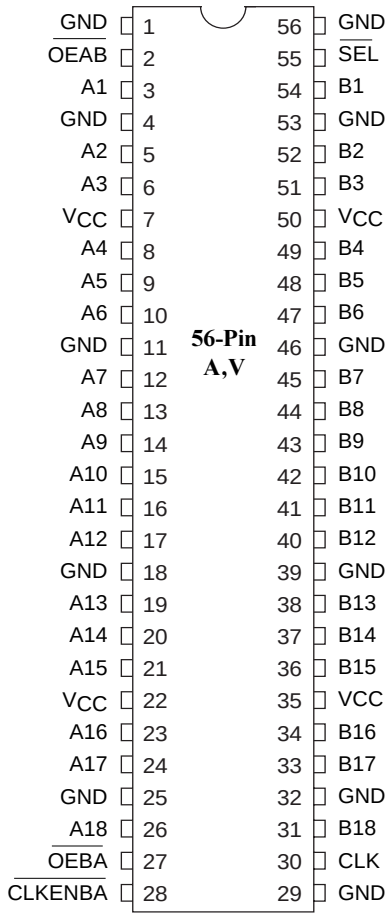
Logic Block Diagram



Product Pin Description

Pin Name	Description
$\overline{\text{CLKEN}}$	Clock Enable Input (Active LOW)
$\overline{\text{SEL}}$	Select (Active LOW)
CLK	Clock Input (Active HIGH)
Ax	Data I/O
Bx	Data I/O
GND	Ground
VCC	Power

Product Pin Configuration



Truth Table[1]† B to A Storage (OEBA = L)

Inputs				Outputs
$\overline{\text{CLKENBA}}$	CLK	$\overline{\text{SEL}}$	B	A
H	X	X	X	A_0‡
L	↑	H	L	L
L	↑	H	H	H
L	↑	L	L	L§
L	↑	L	H	H§

Note:

1. H = High Signal Level
   L = Low Signal Level
   Z = High Impedance
   ↑ = LOW-to-HIGH Transition

‡ Output level before the indicated steady-state input conditions were established.

§ Four positive CLK edges are needed to propagate data from B to A when $\overline{\text{SEL}}$ is low.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... –65°C to +150°C
Supply Voltage Range, V_{CC} ..... –0.5V to 4.6V
Input Voltage Range, V_I: Except
I/O ports(1) ..... –0.5V to 4.6V
I/O ports(1,2) ..... –0.5V to V_{CC} + 0.5V
Output Voltage Range, V_O(1,2) ..... –0.5V to V_{CC} + 0.5V
Input Clamp current, I_{IK} (V_I < 0) ..... –50mA
Output Clamp current, I_{OK} (V_O < 0) ..... –50mA
Continous Output Current, I_O ..... ±50mA
Continous Current through each V_{CC} or GND ..... ±100mA
Maximum Power Dissipation:
A package 1W
V package 1.4W

Note:
Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Notes:
1. The input and output negative-voltage ratings maybe exceeded if the input and outputclamp-current ratings are observed.
2. This value is limited to 4.6V maximum.

Recommended Operating Conditions(1)

Parameters	Description	Test Conditions	Min.	Typ.	Max.	Units
V_{CC}	Supply Voltage		2.3		3.6	V
V_{IH}	Input HIGH Voltage	V_{CC} = 2.3V to 2.7V	1.7			
		V_{CC} = 2.7V to 3.6V	2.0			
V_{IL}	Input LOW Voltage	V_{CC} = 2.3V to 2.7V			0.7	
		V_{CC} = 2.7V to 3.6V			0.8	
V_{IN}	Input Voltage		0		V_{CC}	
V_{OUT}	Output Voltage		0		V_{CC}	
I_{OH}	High-level Output Current	V_{CC} = 2.3V			–12	mA
		V_{CC} = 2.7V			–12	
		V_{CC} = 3.0V			–24	
I_{OL}	Low-level Output Current	V_{CC} = 2.3V			12	
		V_{CC} = 2.7V			12	
		V_{CC} = 3.0V			24	
T_A	Operating Free-Air Temperature		–40		85	°C
$\Delta t/\Delta v$(2)	Input Transition Rise or Fall				10	ns/V

Note:
1. Unused control inputs must be held HIGH or LOW to prevent them from floating.
2. See test circuit and waveforms.

DC Electrical Characteristics (Over the Operating Range, T_A = –40°C to +85°C, V_{CC} = 3.3V ± 10%)

Parameters	Test Conditions		V_{CC}[1]	Min.	Typ.[2]	Max.	Units
V_{OH}	I_{OH} = -100 µA		Min. to Max.	V_{CC} -0.2			V
	I_{OH} = -6 MA	V_{IH} = 1.7V	2.3V	2.0			
	I_{OH} = -12 mA	V_{IH} = 1.7V	2.3V	1.7			
		V_{IH} = 2.0V	2.7V	2.2			
		V_{IH} = 2.0V	3.0V	2.4			
	I_{OH} = -24 mA	V_{IH} = 2.0V	3.0V	2.0			
V_{OL}	I_{OL} = 100 µA		Min. to Max.			0.2	
	I_{OL} = 6 mA	V_{IL} = 0.7V	2.3V			0.4	
	I_{OL} = 12 mA	V_{IL} = 0.7V	2.3V			0.7	
		V_{IL} = 0.8V	2.7V			0.4	
	I_{OL} = 24 mA	V_{IL} = 0.8V	3.0V			0.55	
I_I	V_I = V_{CC} or GND		3.6V			±5	µA
I_I (Hold)[3]	V_I = 0.7V		2.3V	45			
	V_I = 1.7V			-45			
	V_I = 0.8V		3.0V	75			
	V_I = 2.0V			-75			
	V_I = 0 to 3.6V		3.6V			±500	
I_{OZ}[4]	V_O = V_{CC} or GND		3.6V			±10	
I_{CC}	V_I = V_{CC} or GND	I_O = 0	3.6V			40	
ΔI_{CC}	One input at V_{CC} - 0.6V, Other inputs at V_{CC} or GND		3V to 3.6V			750	
C_I Control Inputs	V_I = V_{CC} or GND		3.3V		3		pF
C_{IO} A or B ports	V_O = V_{CC} or GND		3.3V		7		pF

Notes:
1. For Max. or Min. conditions, use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 3.3V, +25°C ambient and maximum loading.
3. Bus Hold maximum dynamic current required to switch the input from one state to another.
4. For I/O ports, the I_{OZ} includes the input leakage current.

Timing Requirements over Operating Range

Parameters	Description	V_{CC} = 2.5V ± 0.2V		V_{CC} = 2.7V		V_{CC} = 3.3V ± 0.3V		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
f_{CLOCK}	Clock frequency	0	120	0	125	0	150	MHz
t_W Pulse Duration	CLK high or low	3.2		3.2		3.0		ns
t_{SU} Setup time	B Data before CLK↑	1.5		1.2		1.1		
	$\overline{SEL}$ before CLK↑	2.7		2.4		2.1		
	$\overline{CLKENBA}$ before CLK↑	2.7		2.6		2.0		
t_H Hold time	B Data after CLK↑	1.0		0.6		1.2		
	$\overline{SEL}$ after CLK↑	0.5		0.2		0.8		
	$\overline{CLKENBA}$ after CLK↑	0.1		0.1		0.3		

Switching Characteristics Over Operating Range[1]

Parameters	From (Input)	To (Output)	V_{CC} = 2.5V ± 0.2V		V_{CC} = 2.7V		V_{CC} = 3.3V ± 0.V		Units
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
f_{MAX}			120		125		150		MHz
t_{PD}	A	B	1.0	3.9		3.8	1.0	3.2	ns
t_{PD}	CLK	A		6.1		6.2		5.2	
t_{EN}	$\overline{OEAB}$ or $\overline{OEBA}$	A or B		6.1		6.1		5.1	
t_{DIS}	$\overline{OEAB}$ or $\overline{OEBA}$	A or B		6.3		5.4		4.9	

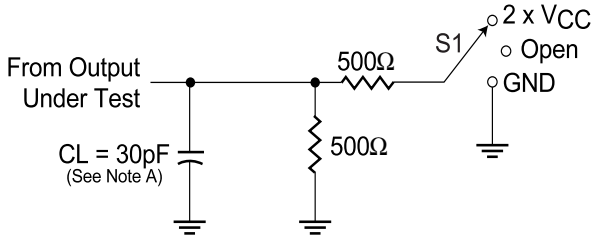
Notes:
1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.

Operating Characteristics, T_A = 25°C

Parameter		Test Conditions	V_{CC} = 2.5V ± 0.2V	V_{CC} = 3.3V ± 0.3V	Units
			Typical		
C_{PD} Power Dissipation Capacitance	Outputs Enabled	C_L = 50pF f = 10 MHz	160		pF
	Outputs Disabled				

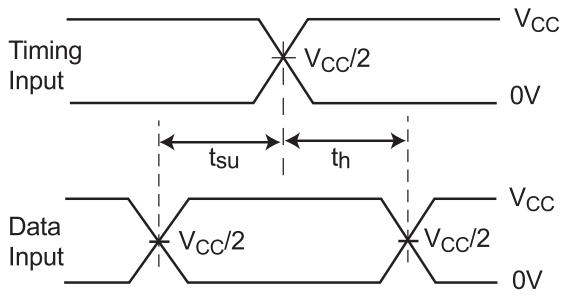
Parameter Measurement Information
V_{CC} = 2.5V ±0.2V

Load Circuit

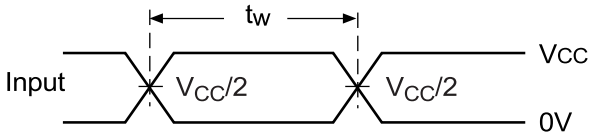


Test	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	2 x V_{CC}
t_{PHZ}/t_{PZH}	GND

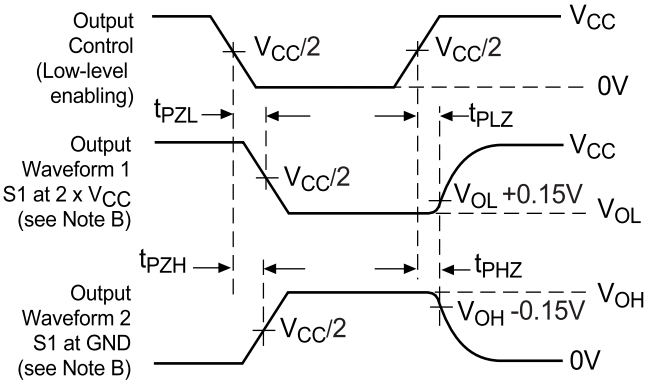
Voltage Waveforms Setup and Hold Times



Voltage Waveforms Pulse Duration



Voltage Waveforms Enable and Disable Times



Voltage Waveforms Propagation Delay Times

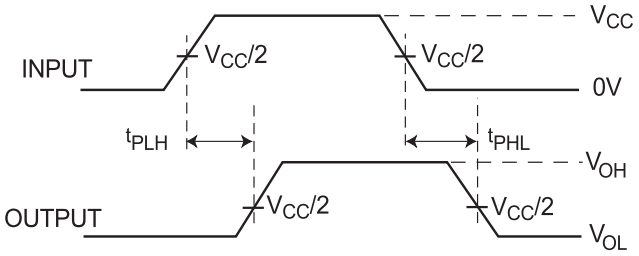


Figure 1. Load Circuit and Voltage Waveforms

Notes:

A. CL includes probe and jig capacitance.

B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

C. All inputs pulses are supplied by generators having the following characteristics: PRR ≤10 MHz, Z_O = 50Ω, $t_r \leq$ 2ns, $t_f \leq$ 2ns.

D. The outputs are measured one at a time with one transition per measurement.

E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.

F. t_{PZL} and t_{PZH} are the same as t_{ten}.

G. t_{PLH} and t_{PHL} are the same as t_{pd}.

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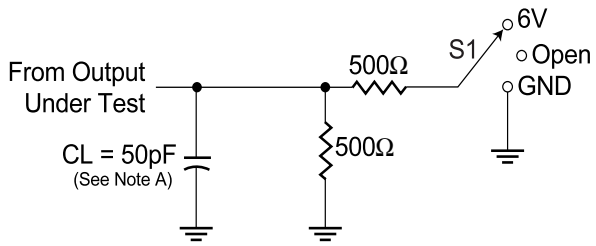
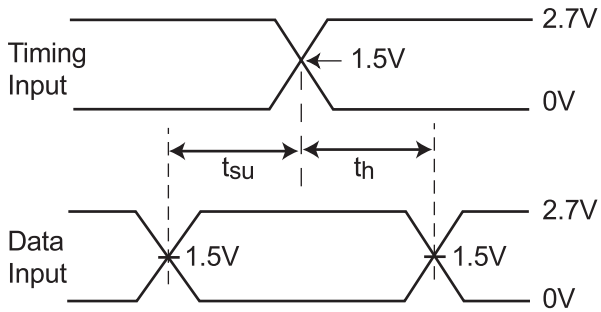
Parameter Measurement Information
V_{CC} = 2.7V and 3.3V ±0.3V

Load Circuit

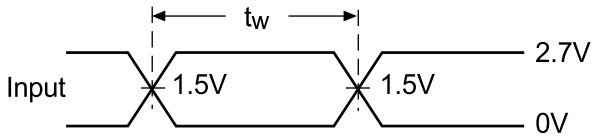


Test	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	6V
t_{PHZ}/t_{PZH}	GND

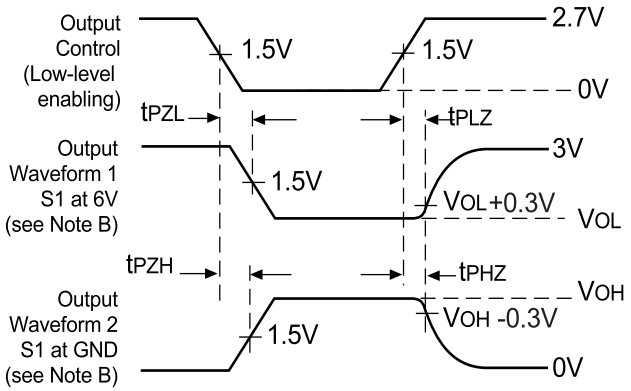
Voltage Waveforms Setup and Hold Times



Voltage Waveforms Pulse Duration



Voltage Waveforms Enable and Disable Times



Voltage Waveforms Propagation Delay Times

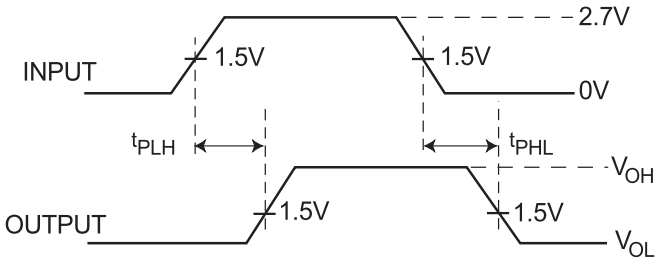


Figure 2. Load Circuit and Voltage Waveforms

Notes:

A. CL includes probe and jig capacitance.

B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

C. All inputs pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50Ω, t_r ≤ 2 ns, t_f ≤ 2 ns.

D. The outputs are measured one at a time with one transition per measurement.

E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.

F. t_{PZL} and t_{PZH} are the same as t_{ten}.

G. t_{PLH} and t_{PHL} are the same as t_{pd}.

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