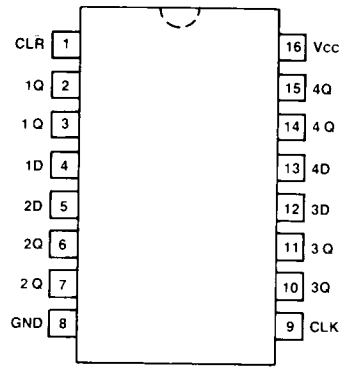## Quad D-Type Flip-Flop with Complementary Outputs/Common Direct Clear

The LS175 is a bipolar, NPN, sealed-junction, silicon integrated circuit. It is manufactured in low-power Schottky technology and is available in a wire-bonded, 16-pin plastic DIP or surface mount package.

CLR	1	16	Vcc
1Q	2	15	4Q
1 Q̄	3	14	4 Q̄
1D	4	13	4D
2D	5	12	3D
2Q	6	11	3 Q̄
2 Q̄	7	10	3Q
GND	8	9	CLK

Truth Table (Each Flip-Flop)

Inputs			Outputs	
Clear	Clock	D	Q	$\overline{Q}$
L	X	X	L	H
H	↑	H	H	L
H	↑	L	L	H
H	L	X	Q_0	$\overline{Q}_0$

H = High level (steady state)
L = Low level (steady state)
X = Irrelevant
↑ = Transition from low to high level
Q_0= The level of Q before the indicated steady state input conditions were established
$\overline{Q}_0$ = Complement of Q_0 or level of $\overline{Q}$ before the indicated steady-state input conditions were established

Logic Diagram
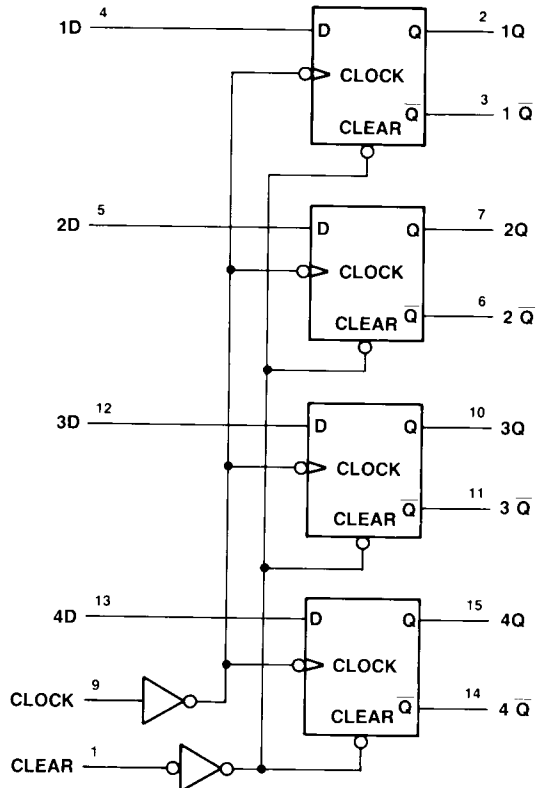
Electrical Characteristics

Vcc = 5.0 ±0.5 V, TA = −55 to +125°C (WA-LS)
Vcc = 5.0 ±0.25 V, TA = 0 to 70°C (WP90350L1)
Vcc = 5.0 ±0.5 V, TA = −40 to +85°C (WA-LSD, WP91399L2)

Parameter	Symbol	WA-LS		WP, WA-LSD		Units
		Min	Max	Min	Max	
Output Voltage, Vcc = 4.5 V (WA-LS), 4.75 V (WP, WA-LSD)						
Low, IOL = 4.0 mA	VOL	—	0.4	—	0.4	V
IOL = 8.0 mA	VOL	—	0.5	—	0.5	V
High, IOH = −0.4 mA	VOH	2.5	—	2.7	—	V
Input Voltage, Vcc = 4.5 V (WA-LS), 4.75 V (WP, WA-LSD)						
Low	VIL	—	0.7	—	0.8*	V
High	VIH	2.0	7.5	2.0	5.5	V
Clamp, IIN = −18.0 mA	VIK	—	−1.5	—	−1.5	V
Input Current, Vcc = 5.5 V (WA-LS), 5.25 V (WP, WA-LSD)						
Low, VIL = 0.4 V	IIL	—	−0.4	—	−0.4	mA
High, VIH = 2.7 V	IIH	—	20.0	—	20.0	μA
@ VI max, VI = 7.0 V (WA-LS), 5.5 V (WP, WA-LSD)	II	—	0.1	—	0.1	mA
Output Current, Vcc = 5.5 V (WA-LS), 5.25 V (WP, WA-LSD)						
Short-Circuit	IOS	−20.0	−100.0	−20.0	−100.0	mA
Supply Current, Vcc = 5.5 V (Outputs Open, Data and Clear High, Clock Momentary Ground; then High)	ICC	—	18.0	—	18.0	mA

* WA-LSD, WP91399L2: VIL = 0.7 V

Timing Characteristics

Vcc = 5.0 V, TA = 25°C, CL = 15 pF

Parameter	Symbol	WA-LS		WP, WA-LSD		Units
		Min	Max	Min	Max	
Propagation Delay						
Clear-to-Output						
Low-to-High	tPLH	—	25.0	—	30.0	ns
High-to-Low	tPHL	—	28.0	—	30.0	ns
Clock-to-Output						
Low-to-High	tPLH	—	20.0	—	25.0	ns
High-to-Low	tPHL	—	22.0	—	25.0	ns
Operating Conditions						
Width of Clock Pulse	tw	20.0	—	20.0	—	ns
Setup Time						
Data, Low	tDSL	5.0	—	20.0	—	ns
High	tDSH	0	—	20.0	—	ns
Clear Inactive State, Low	tDSL	25.0	—	25.0	—	ns
High	tDSH	25.0	—	25.0	—	ns
Data Hold Time, Low	tDHL	10.0	—	5.0	—	ns
High	tDHH	10.0	—	5.0	—	ns
Maximum Clock Frequency	fmax	30.0	—	30.0	—	MHz

Maximum Ratings

Power supply voltage (VCC)... 7.0 V
Operating temperature (TA)... WA-LS: −55 to +125°C
WP90350L1: 0 to 70°C
WA-LSD, WP91399L2: −40 to +85°C
Storage temperature (Tstg).. −65 to +150°C

Maximum ratings are defined as the limiting conditions that the user can apply to the device under all variations of circuit and environmental conditions. If any rating is exceeded, permanent damage to the device may result.

Bonding or soldering of the external leads of this device can be performed safely at temperatures up to 300°C.

Timing Diagrams
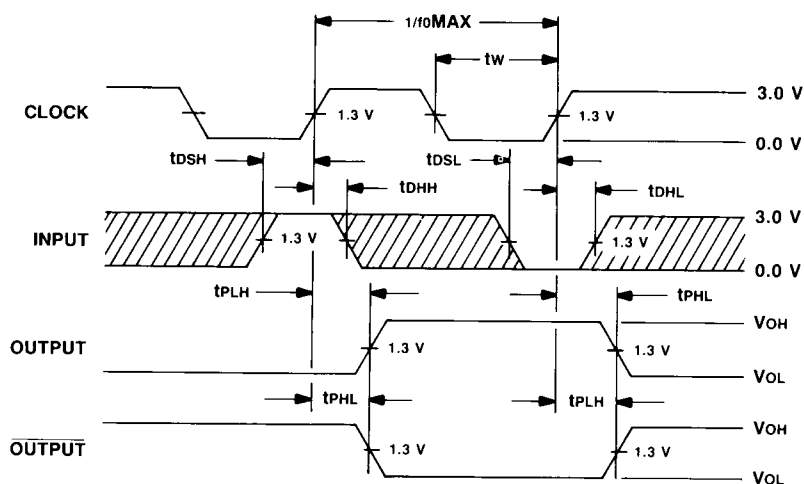
THE SHADED AREAS INDICATE WHEN THE INPUT IS PERMITTED
TO CHANGE FOR PREDICTABLE OUTPUT PERFORMANCE

Figure 1. Clear to Output Delay, Clear Pulse Width, and Clearing Time
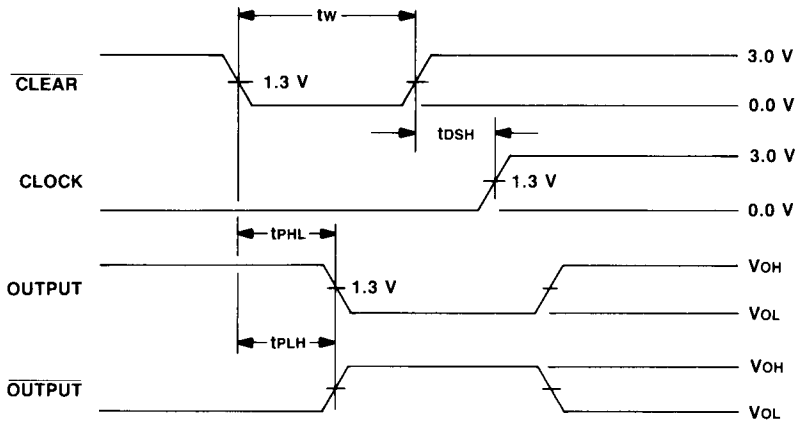
Figure 2. Clock to Output Delays, Clock Pulse Width, Frequency,
Set-Up and Hold Times Data to Clock