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April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (<http://www.renesas.com>)

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Not recommended
for new design

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HD74BC573A

Octal D Type Transparent Latches With 3 State Outputs

REJ03D0287-0300Z
 (Previous ADE-205-021A (Z))
 Rev.3.00
 Jul.16.2004

Description

The HD74BC573A provides high drivability and operation equal to or better than high speed bipolar standard logic IC by using Bi-CMOS process. The device features low power dissipation that is about 1/5 of high speed bipolar logic IC, when the frequency is 10 MHz. The device has eight D type latches with three state outputs in a 20 pin package. When the latch enable input is high, the Q outputs will follow the D inputs. When the latch enable goes low, data at the D inputs will be retained at the outputs until latch enable returns high again. When a high logic level is applied to the output control input, all outputs go to a high impedance state, regardless of what signals are present at the other inputs and the state of the storage elements.

Features

- Input/Output are at high impedance state when power supply is off.
- Built in input pull up circuit can make input pins be open, when not used.
- TTL level input
- Wide operating temperature range
 $T_a = -40$ to $+85^\circ\text{C}$
- Ordering Information

Part Name	Package Type	Package Code	Package Abbreviation	Taping Abbreviation (Quantity)
HD74BC573AP	DILP-20 pin	DP-20N, -20NEV	P	—
HD74BC573AFPEL	SOP-20 pin (JEITA)	FP-20DAV	FP	EL (2,000 pcs/reel)

Note: Please consults the sales office for the above package availability.

Function Table

Output Control	Latch Enable	Data	Output Q
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

H : High level

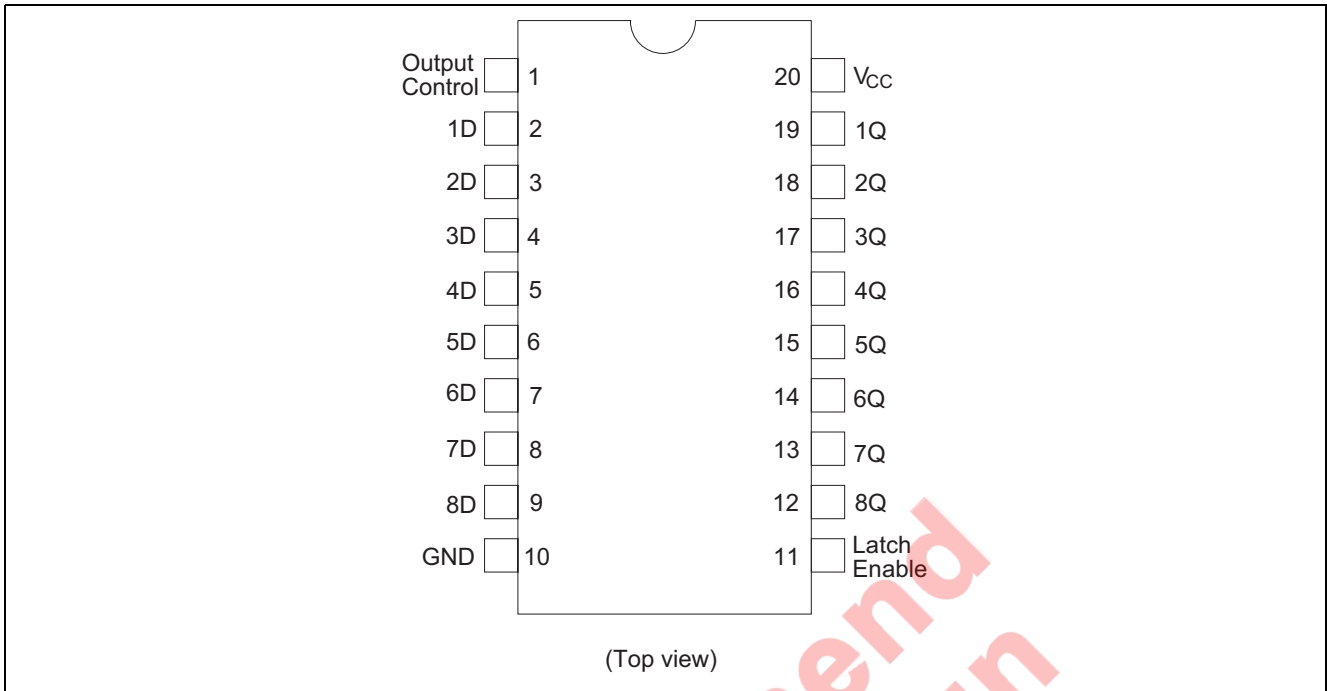
L : Low level

X : Immaterial

Z : High impedance

Q_0 : Level of Q before the indicated steady input conditions were established

Pin Arrangement



Absolute Maximum Ratings

Item	Symbol	Rating	Unit
Supply voltage	V_{CC}	-0.5 to +7.0	V
Input diode current	I_{IK}	± 30	mA
Input voltage	V_{IN}	-0.5 to +7.5	V
Output voltage	V_{OUT}	-0.5 to +7.5	V
Off state output voltage	$V_{OUT(off)}$	-0.5 to +5.5	V
Storage temperature	T_{stg}	-65 to +150	°C

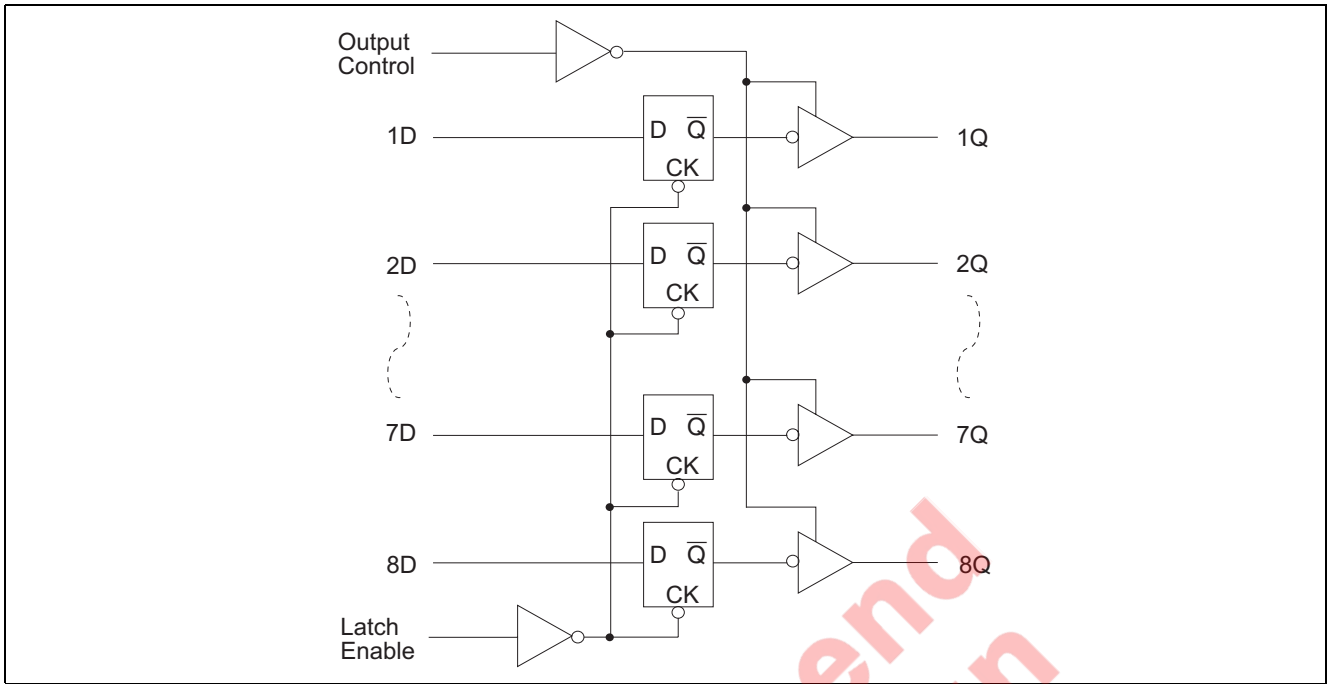
Note: 1. The absolute maximum ratings are values which must not individually be exceeded, and furthermore, no two of which may be realized at the same time.

Recommended Operating Conditions

Item	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input voltage	V_{IN}	0	—	V_{CC}	V
Output voltage	V_{OUT}	0	—	V_{CC}	V
Operating temperature	T_{opr}	-40	—	85	°C
Input rise/fall time*1	t_r, t_f	0	—	8	ns/V

Note: 1. This item guarantees maximum limit when one input switches.
 Waveform: Refer to test circuit of switching characteristics.

Logic Diagram



Electrical Characteristics (Ta = -40°C to +85°C)

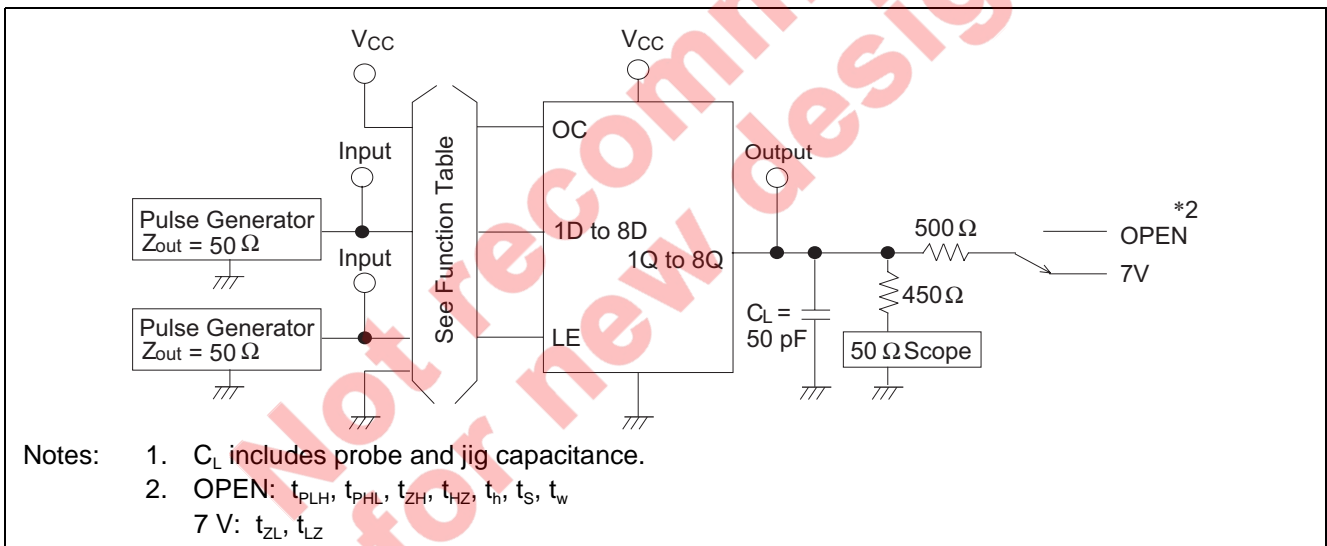
Item	Symbol	V _{CC} (V)	Min	Max	Unit	Test Conditions
Input voltage	V _{IH}		2.0	—	V	
	V _{IL}		—	0.8	V	
Output voltage	V _{OH}	4.5	2.4	—	V	I _{OH} = -3 mA
		4.5	2.0	—	V	I _{OH} = -15 mA
	V _{OL}	4.5	—	0.4	V	I _{OL} = 24 mA
		4.5	—	0.5	V	I _{OL} = 48 mA
Input diode voltage	V _{IK}	4.5	—	-1.2	V	I _{IN} = -18 mA
Input current	I _I	5.5	—	-250	μA	V _{IN} = 0 V
		5.5	—	1.0	μA	V _{IN} = 5.5 V
		5.5	—	100	μA	V _{IN} = 7.0 V
Short circuit output current*1	I _{OS}	5.5	-100	-225	mA	V _{IN} = 0 or 5.5 V
Off state output current	I _{OZH}	5.5	—	50	μA	V _O = 2.7 V
	I _{OZL}	5.5	—	-50	μA	V _O = 0.5 V
Supply current	I _{CCL}	5.5	—	29.5	mA	V _{IN} = 0 or 5.5 V All outputs is "L"
						V _{IN} = 0 or 5.5 V All outputs is "H"
	I _{CCZ}	5.5	—	2.5	mA	V _{IN} = 0 or 5.5 V All outputs is "Z"
						V _{IN} = 3.4 or 0.5 V
I _{CCT} *2	5.5	—	1.5	mA		

- Notes: 1. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
 2. When input by the TTL level, it shows I_{CC} increase at per one input pin.

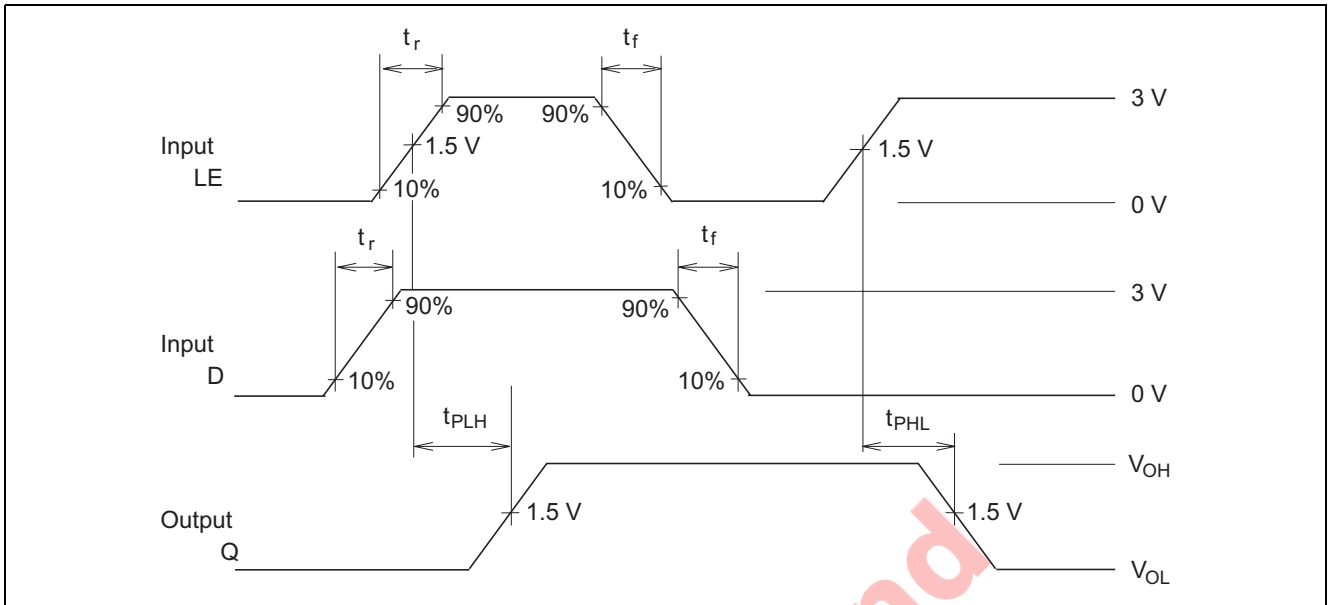
Switching Test Method ($C_L = 50 \text{ pF}$)

Item	Symbol	$T_a = 25^\circ\text{C}$ $V_{CC} = 5.0 \text{ V}$		$T_a = -40 \text{ to } 85^\circ\text{C}$ $V_{CC} = 5.0 \text{ V} \pm 10\%$		Unit	Test conditions	
		Min	Max	Min	Max			
Propagation delay time	D → Q	t_{PLH}	3.0	8.0	3.0	10.0	ns	See under figure
		t_{PHL}	3.0	8.0	3.0	10.0		
	LE → Q	t_{PLH}	3.0	8.0	3.0	10.0		
		t_{PHL}	3.0	8.0	3.0	10.0		
Output enable time	t_{ZH}	3.0	9.0	3.0	11.0	ns		
	t_{ZL}	3.0	9.0	3.0	11.0			
Output disable time	t_{HZ}	3.0	8.0	3.0	10.0	ns		
	t_{LZ}	3.0	8.0	3.0	10.0			
Setup time	$t_s(H)$	2.0	—	2.0	—	ns		
	$t_s(L)$	2.0	—	2.0	—			
Hold time	$t_h(H)$	2.0	—	2.0	—	ns		
	$t_h(L)$	2.0	—	2.0	—			
Pulse width	t_w	6.0	—	6.0	—	ns		
Input capacitance	C_{IN}	3.0 (Typ)		—		pF	$V_{IN} = V_{CC} \text{ or GND}$	
Output capacitance	C_O	15.0 (Typ)		—		pF	$V_O = V_{CC} \text{ or GND}$	

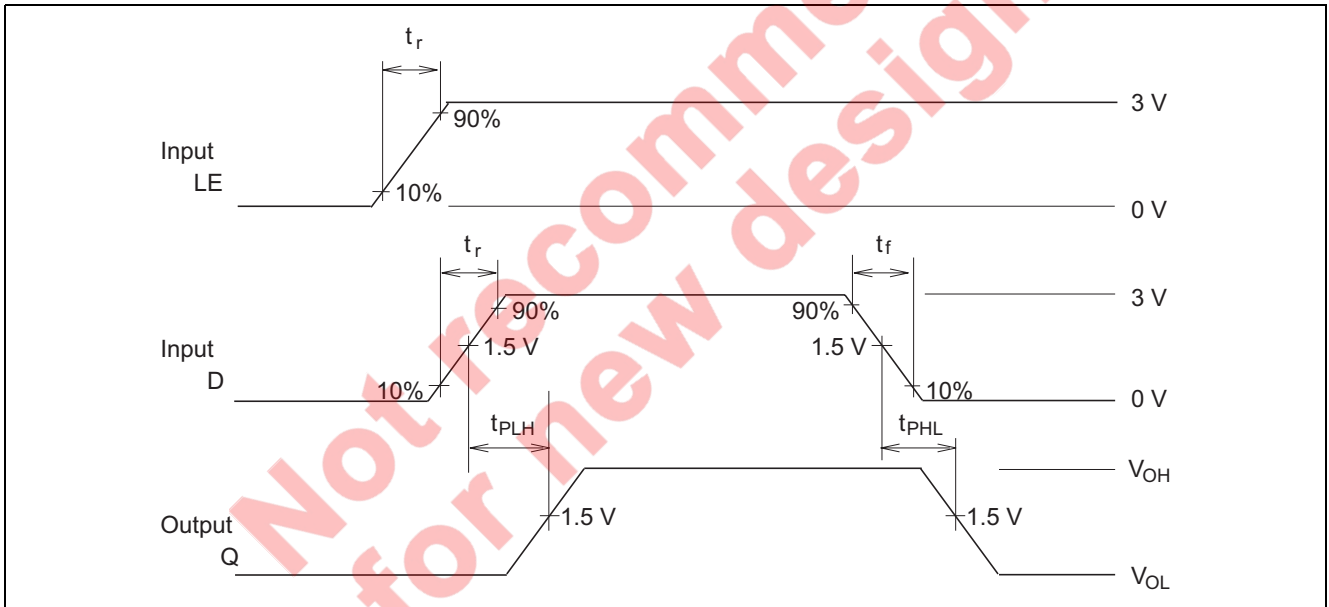
Test Circuit



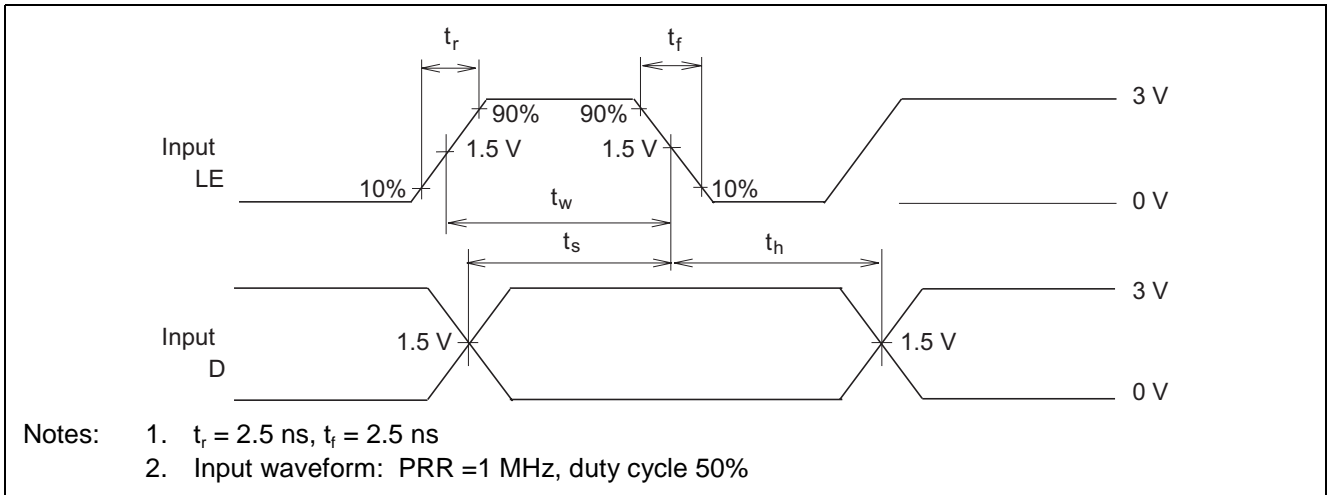
Waveforms-1



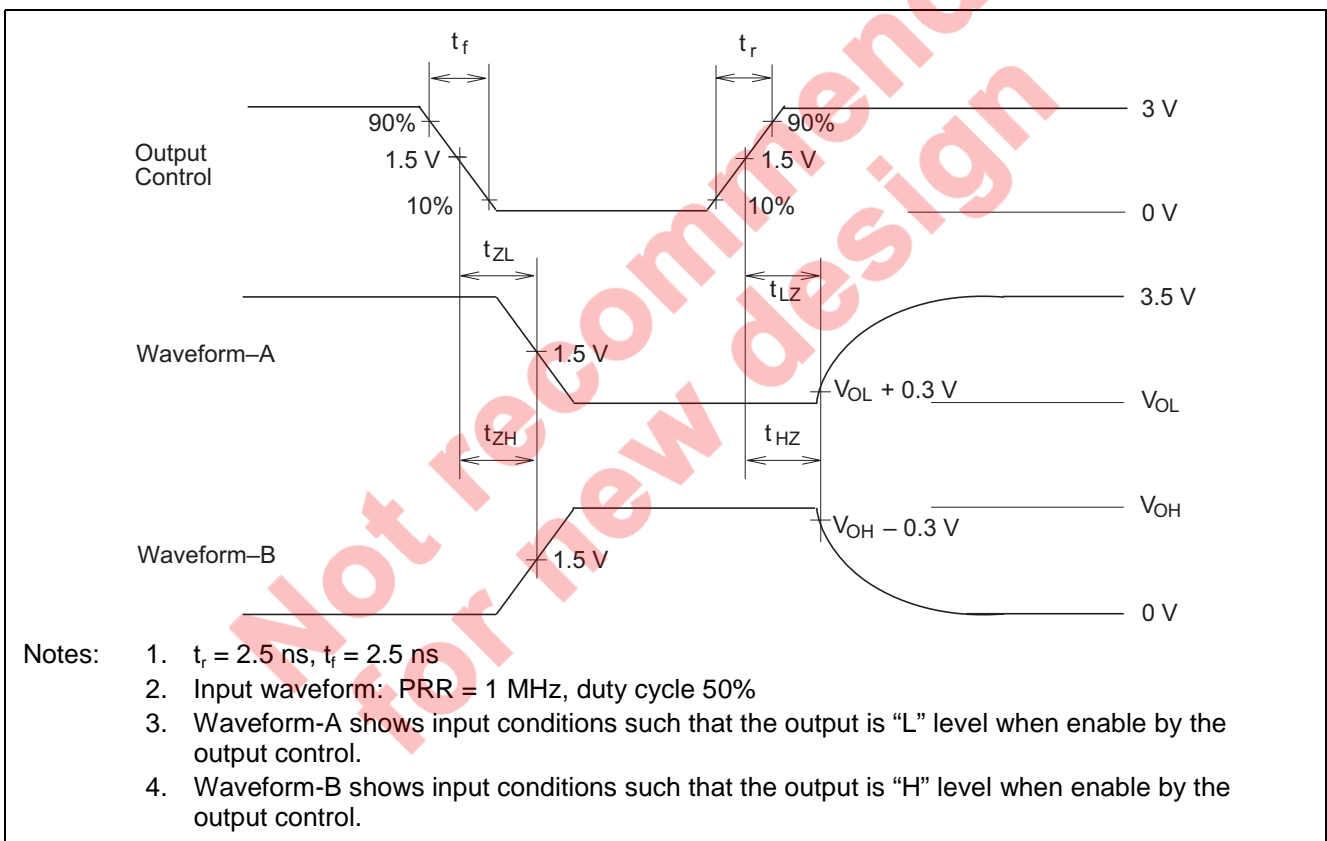
Waveforms-2



Waveforms-3

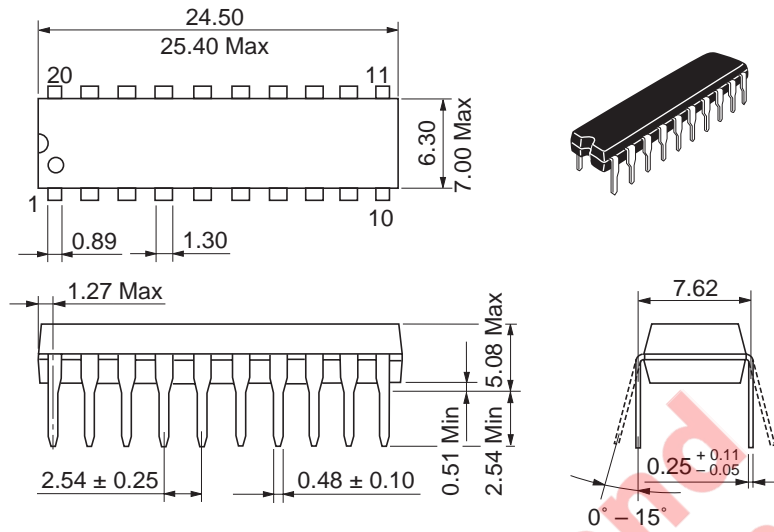


Waveforms-4



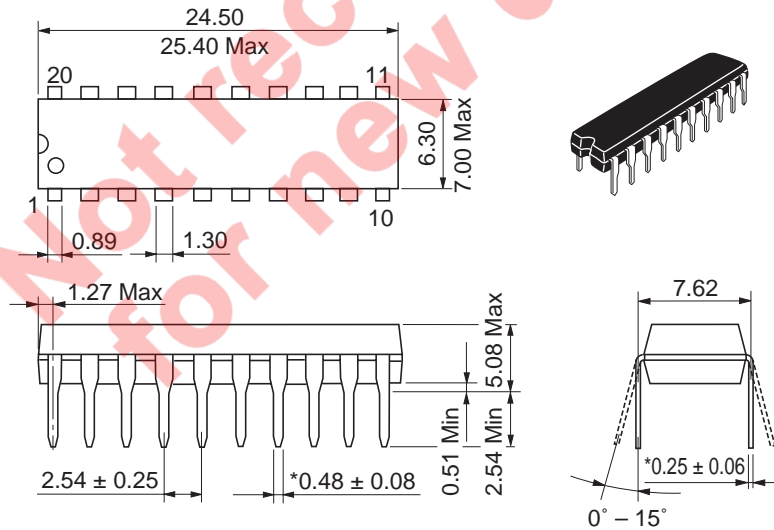
Package Dimensions

As of January, 2003
Unit: mm



Package Code	DP-20N
JEDEC	—
JEITA	Conforms
Mass (reference value)	1.26 g

Unit: mm

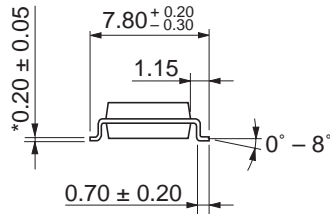
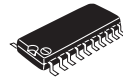
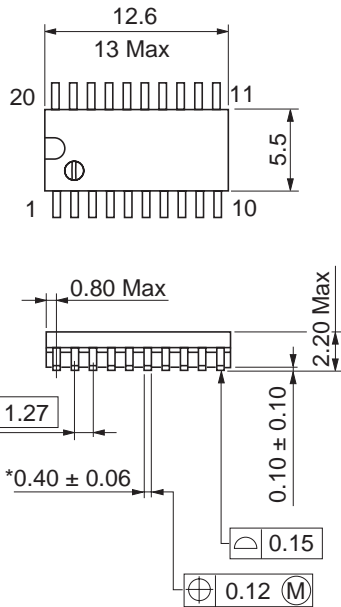


*Ni/Pd/AU Plating

Package Code	DP-20NEV
JEDEC	—
JEITA	Conforms
Mass (reference value)	1.26 g

As of January, 2003

Unit: mm



*Ni/Pd/Au plating

Package Code	FP-20DAV
JEDEC	—
JEITA	Conforms
Mass (reference value)	0.31 g

Not recommended for new designs

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