

DATA SHEET

CBT3245 Octal bus switch

Product specification
Supersedes data of 1998 Dec 8

2000 Jun 19

Octal bus switch

CBT3245

FEATURES

- Standard '245-type pinout
- 5 Ω switch connection between two ports
- TTL compatible control input levels
- Package options include plastic small outline (D), shrink small outline (DB), thin shrink small outline (TSSOP)
- Latch-up protection exceeds 500 mA per JESD78
- ESD protection exceeds 2000 V HBM per JESD22-A114, 200 V MM per JESD22-A115 and 1000 V CDM per JESD22-C101

DESCRIPTION

The CBT3245 provides eight bits of high-speed TTL-compatible bus switching in a standard '245 device pinout. The low on-state resistance of the switch allows connections to be made with minimal propagation delay.

The CBT3245 device is organized as one 8-bit switch. When enable (\overline{OE}) is low, the switch is on and port A is connected to port B. When \overline{OE} is high, the switch is open and a high-impedance state exists between the two ports.

The CBT3245 is characterized for operation from -40°C to 85°C .

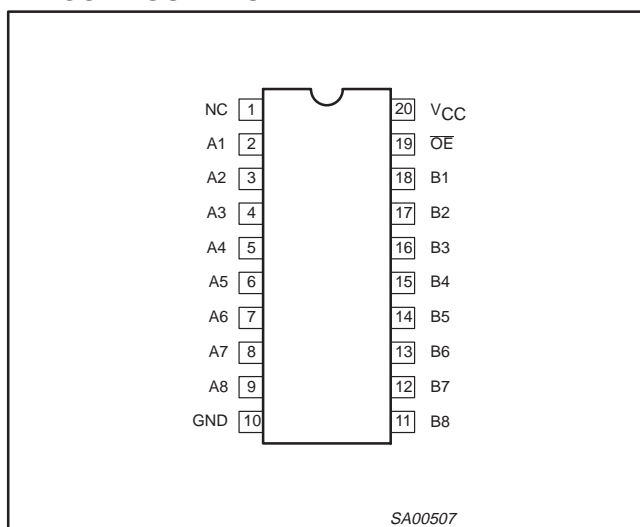
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS $T_{\text{amb}} = 25^{\circ}\text{C}; \text{GND} = 0\text{V}$	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay An to Yn	$C_L = 50\text{pF}; V_{\text{CC}} = 5\text{V}$		ns
$C_{\text{IO(OFF)}}$	Pin capacitance (OFF state)	$V_O = 3\text{V or }0\text{V}$	6	pF
I_{CCZ}	Total supply current	Outputs disabled; $V_{\text{CC}} = 5.5\text{V}$		μA

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE	DWG NUMBER
20-Pin Plastic TSSOP Type I	-40°C to 85°C	CBT3245 PW DH	SOT360-1
20-Pin Plastic SSOP Type I	-40°C to 85°C	CBT3245 PW DH	SOT360-1
20-Pin Plastic SOP Type I	-40°C to 85°C	CBT3245 PW DH	SOT360-1

PIN CONFIGURATION



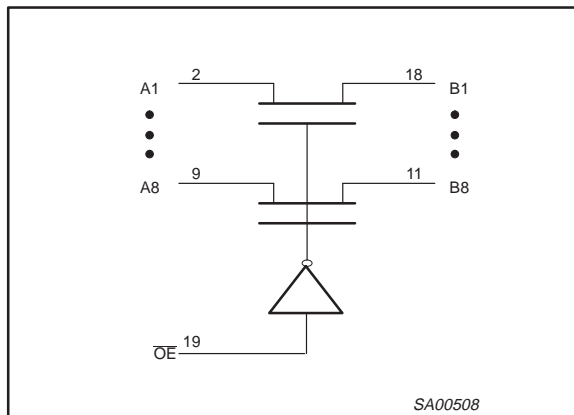
PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1	NC	No internal connection
19	\overline{OE}	Output enable input
2, 3, 4, 5, 6, 7, 8, 9	A1–A8	Inputs
18, 17, 16, 15, 14, 13, 12, 11	B1–B8	Outputs
10	GND	Ground (0V)
20	V_{CC}	Positive supply voltage

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LOGIC SYMBOL



FUNCTION TABLE

INPUT	INPUTS/OUTPUTS
\overline{OE}	A, B
L	A = B
H	Z

H = High voltage level
 L = Low voltage level
 Z = High impedance "off" state

ABSOLUTE MAXIMUM RATINGS^{1, 2}

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to +7.0	V
I_{IK}	DC input diode current	$V_I < 0$	-50	mA
V_I	DC input voltage ³		-0.5 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	-50	mA
V_{OUT}	DC output voltage ³	output in Off or High state	-0.5 to +7	V
I_{OUT}	DC output current	output in Low state	128	mA
T_{stg}	Storage temperature range		-65 to 150	°C

NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		Min	Max	
V_{CC}	DC supply voltage	4.0	5.5	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Low-level Input voltage		0.8	V
T_{amb}	Operating free-air temperature range	-40	+85	°C

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DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			$T_{amb} = -40^{\circ}\text{C to } +85^{\circ}\text{C}$			
			Min	Typ ¹	Max	
V_{IK}	Input clamp voltage	$V_{CC} = 4.5\text{V}; I_I = -18\text{mA}$			-1.2	V
I_I	Input leakage current	$V_{CC} = 5.5\text{V}; V_I = \text{GND or } 5.5\text{V}$			± 5	μA
I_{CC}	Quiescent supply current ²	$V_{CC} = 5.5\text{V}; I_O = 0, V_I = V_{CC} \text{ or } \text{GND}$			50	μA
ΔI_{CC}	Additional supply current per input pin ²	$V_{CC} = 5.5\text{V}$, one input at 3.4V, other inputs at V_{CC} or GND			3.5	mA
C_I	Control pins	$V_I = 3\text{V or } 0, \overline{OE} = V_{CC}$		3		pF
$C_{IO(OFF)}$	Power-off leakage current	$V_O = 3\text{V or } 0$		6		pF
r_{on}^3	On-resistance	$V_{CC} = 4.5\text{V}; V_I = 0\text{V}; I_I = 64\text{mA}$		5	7	Ω
		$V_{CC} = 4.5\text{V}; V_I = 0\text{V}; I_I = 30\text{mA}$		5	7	
		$V_{CC} = 4.5\text{V}; V_I = 2.4\text{V}; I_I = 15\text{mA}$		10	15	

NOTES:

- All typical values are at $V_{CC} = 5\text{V}$, $T_A = 25^{\circ}\text{C}$
- This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND
- Measured by the voltage drop between the A and the B terminals at the indicated current through the switch.
On-state resistance is determined by the lowest voltage of the two (A or B) terminals.

AC CHARACTERISTICS

GND = 0V; t_R ; $C_L = 50\text{pF}$

SYMBOL	PARAMETER	FROM (INPUT)	TO (OUTPUT)	74CBT3245		UNIT
				$T_{amb} = -40^{\circ}\text{C to } +85^{\circ}\text{C}$ $V_{CC} = +5.0\text{V} \pm 0.5\text{V}$		
				Min	Max	
t_{pd}	Propagation delay ¹	A or B	B or A		0.25	ns
t_{en}	Output enable time to High and Low level	\overline{OE}	A or B			ns
t_{dis}	Output disable time from High and Low level	\overline{OE}	A or B			ns

NOTES:

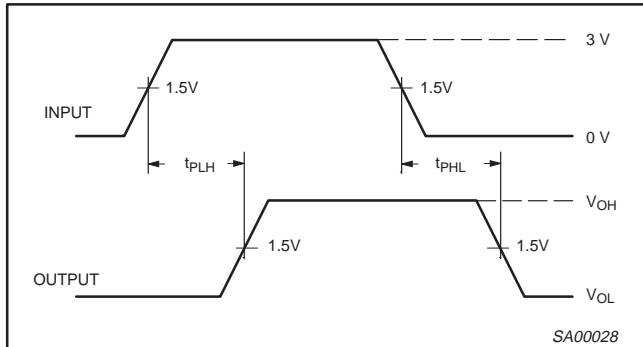
- This parameter is warranted but not production tested. The propagation delay is based on the RC time constant of the typical on-state resistance of the switch and a load capacitance of 50 pF, when driven by an ideal voltage source (zero output impedance).

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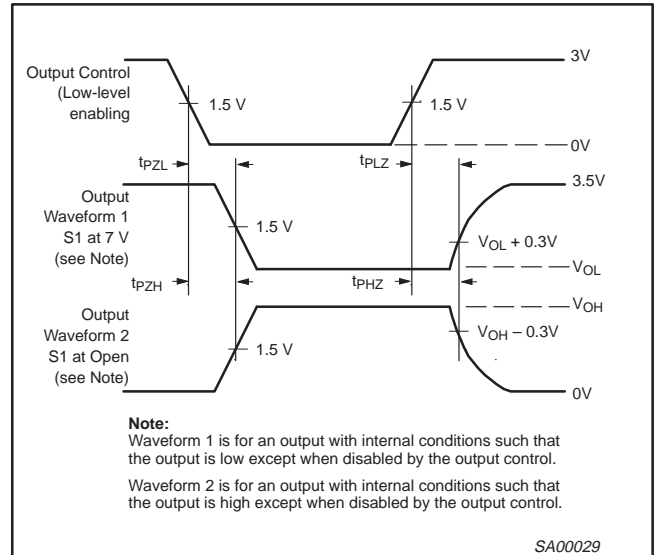
CBT3245

AC WAVEFORMS

$V_M = 1.5V, V_{IN} = GND \text{ to } 3.0V$



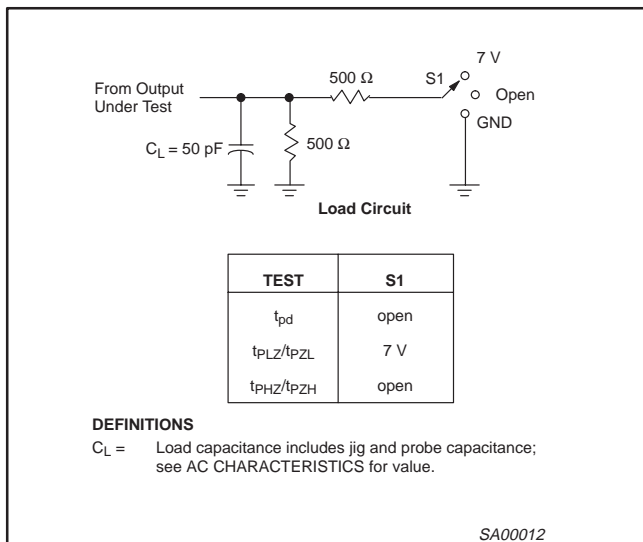
Waveform 1. Input to Output Propagation Delays



Note:
Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

Waveform 2. 3-State Output Enable and Disable Times

TEST CIRCUIT AND WAVEFORMS



NOTES:

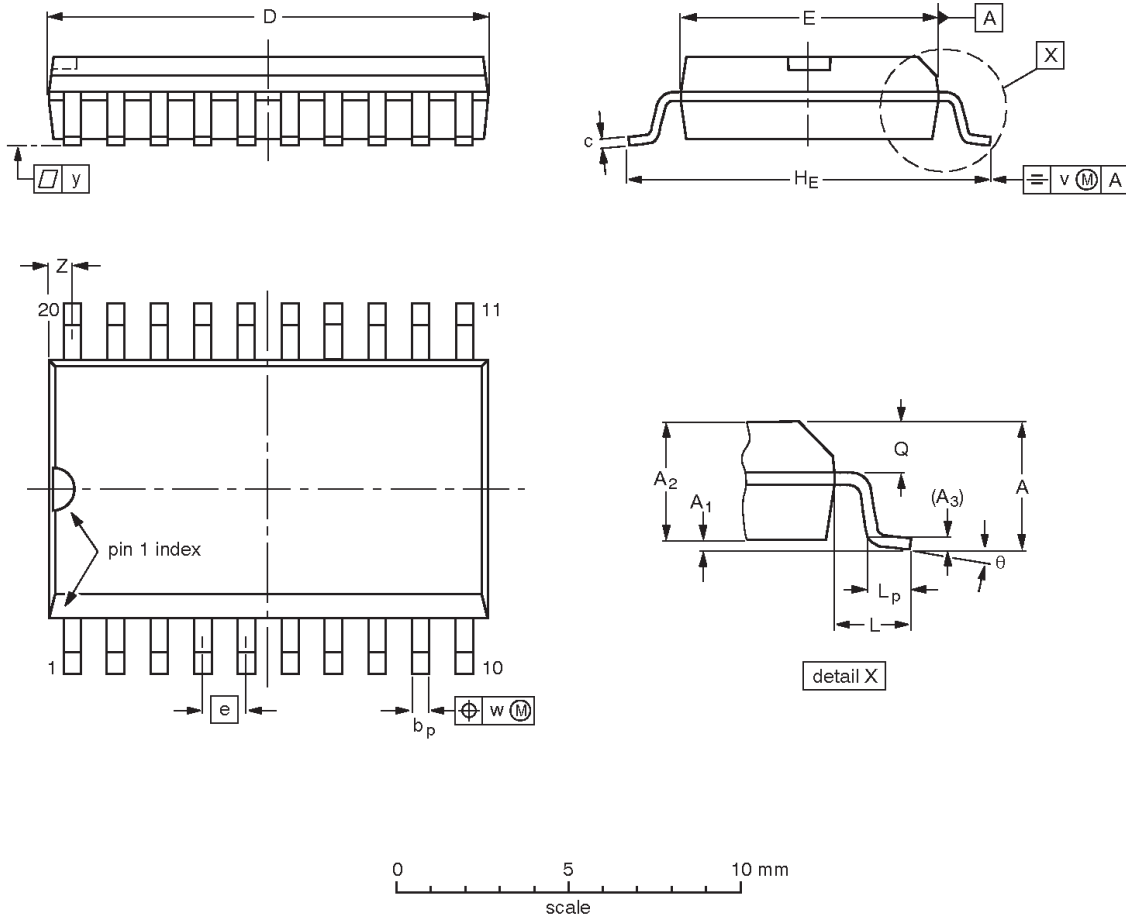
1. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}, Z_O = 50 \Omega, t_r \leq 2.5 \text{ ns}, t_f \leq 2.5 \text{ ns}$.
2. The outputs are measured one at a time with one transition per measurement.

Octal bus switch

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SO20: plastic small outline package; 20 leads; body width 7.5 mm

SOT163-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽¹⁾	e	H _E	L	L _p	Q	v	w	y	z ⁽¹⁾	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	13.0 12.6	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8° 0°
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.51 0.49	0.30 0.29	0.050	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

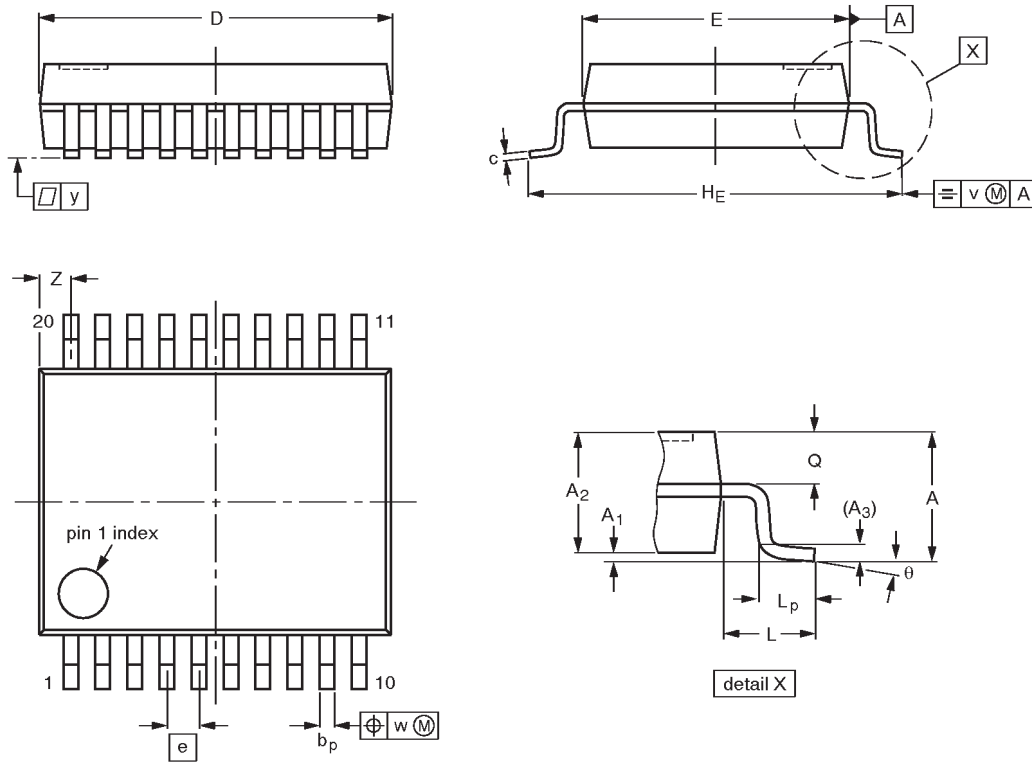
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT163-1	075E04	MS-013AC				95-01-24 97-05-22

Octal bus switch

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SSOP20: plastic shrink small outline package; 20 leads; body width 5.3 mm

SOT339-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽¹⁾	e	H _E	L	L _p	Q	v	w	y	Z ⁽¹⁾	θ
mm	2.0	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	7.4 7.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	0.9 0.5	8° 0°

Note

1. Plastic or metal protrusions of 0.20 mm maximum per side are not included.

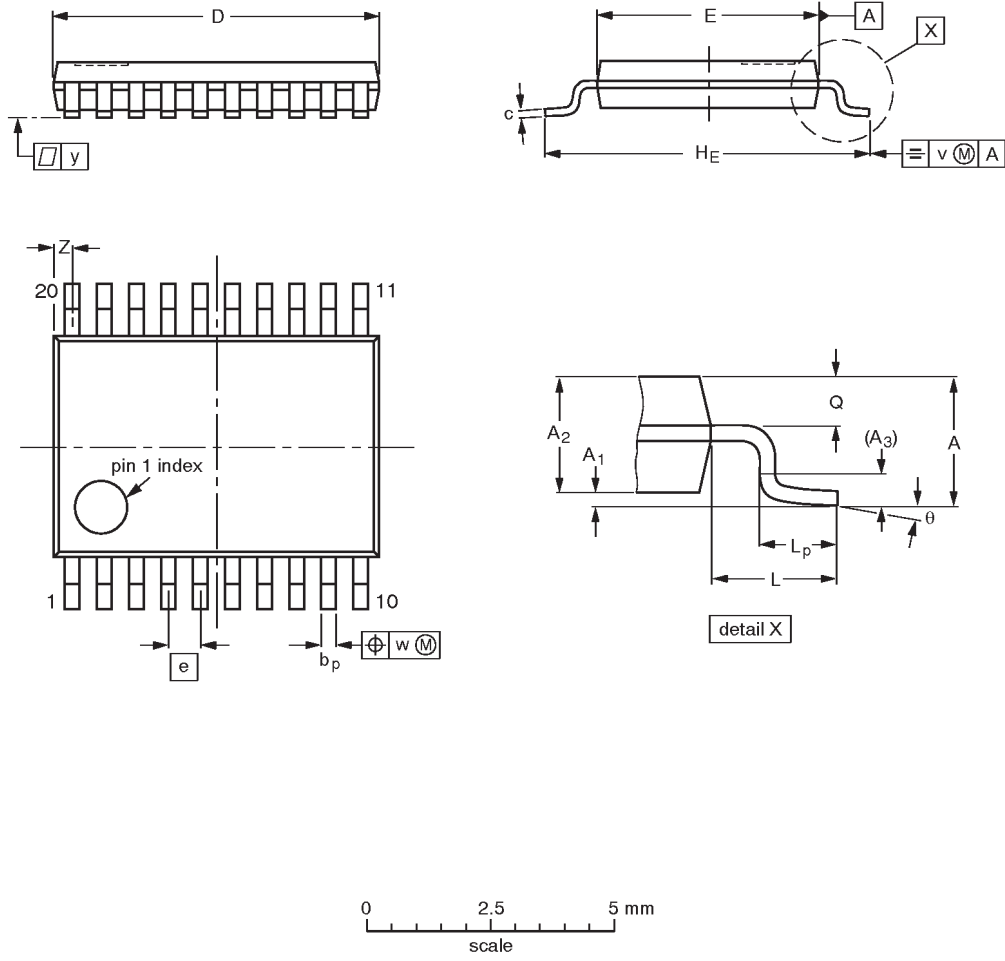
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT339-1		MO-150AE				93-09-08 95-02-04

Octal bus switch

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TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm

SOT360-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽²⁾	e	H _E	L	L _p	Q	v	w	y	Z ⁽¹⁾	θ
mm	1.10	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	6.6 6.4	4.5 4.3	0.65	6.6 6.2	1.0	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.5 0.2	8° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT360-1		MO-153AC				-93-06-16- 95-02-04

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NOTES

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Data sheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
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Description

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Cross reference

Models

Packages

Application notes

Selection guides

Other technical documentation

End of Life information

Datahandbook system

The CBT3245 is characterized for operation from -40 Cel to 85 Cel.

Features

- Standard '245-type pinout
- 5 Ohm switch connection between two ports
- TTL compatible control input levels
- Package options include plastic small outline (D), shrink small outline (DB), thin shrink small outline (TSSOP)
- Latch-up protection exceeds 500 mA per JESD78
- ESD protection exceeds 2000 V HBM per JESD22-A114, 200 V MM per JESD22-A115 and 1000 V CDM per JESD22-C101

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		9352 655 00118	Standard Marking * Reel Pack, SMD, 13"	SOT163	Full production	-
CBT3245DB		9352 655 01112	Standard Marking * Tube	SOT339	Full production	-
		9352 655 01118	Standard Marking * Reel Pack, SMD, 13"	SOT339	Full production	-
CBT3245PW		9352 655 02112	Standard Marking * Tube	SOT360	Full production	-
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