



3.3V CMOS 16-BIT REGISTERED TRANSCEIVER WITH 3-STATE OUTPUTS, 5 VOLT TOLERANT I/O

IDT74LVC16543A

FEATURES:

- Typical $t_{sk(o)}$ (Output Skew) < 250ps
- ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
- $V_{cc} = 3.3V \pm 0.3V$, Normal Range
- $V_{cc} = 2.7V$ to $3.6V$, Extended Range
- CMOS power levels (0.4 μ W typ. static)
- All inputs, outputs, and I/O are 5V tolerant
- Supports hot insertion
- Available in SSOP, TSSOP, and TVSOP packages

DRIVE FEATURES:

- High Output Drivers: $\pm 24mA$
- Reduced system switching noise

APPLICATIONS:

- 5V and 3.3V mixed voltage systems
- Data communication and telecommunication systems

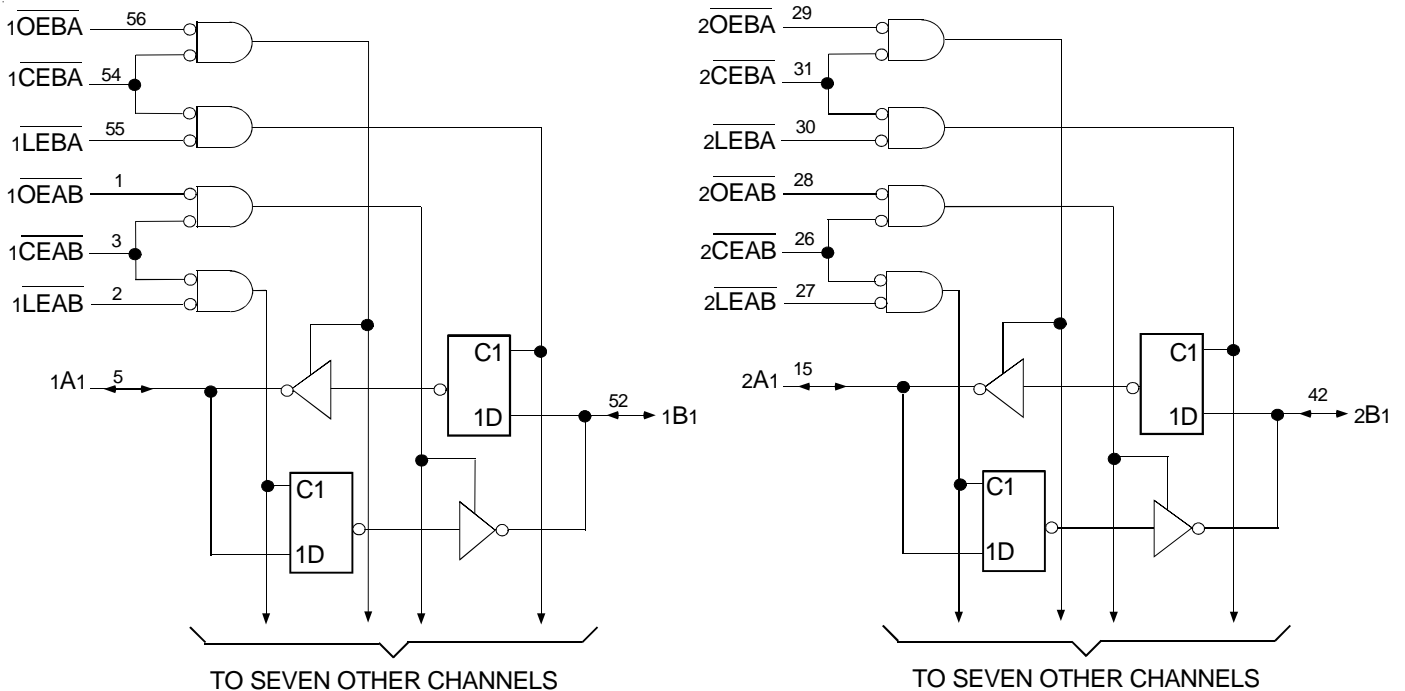
DESCRIPTION:

The LVC16543A 16-bit registered transceiver is built using advanced dual metal CMOS technology. This high-speed, low-power device can be used as two 8-bit transceivers or one 16-bit transceiver. Separate latch-enable (\overline{LEAB} or \overline{LEBA}) and output-enable (\overline{OEAB} or \overline{OEBA}) inputs are provided for each register to permit independent control in either direction of data flow. For example, the A-to-B enable (\overline{CEAB}) must be low to enter data from the A port or to output data from the B port. \overline{LEAB} controls the latch function. When \overline{LEAB} is low, the latches are transparent. A subsequent low-to-high transition of \overline{LEAB} signal puts the A latches in the storage mode. \overline{OEAB} performs the output enable function on the B port. Data flow from the B port to the A port is similar but requires using \overline{CEBA} , \overline{LEBA} , and \overline{OEBA} inputs. Flow-through organization of signal pins simplifies layout. All inputs are designed with hysteresis for improved noise margin.

All pins of this 16-bit latched transceiver can be driven from either 3.3V or 5V devices. This feature allows the use of this device as a translator in a mixed 3.3V/5V supply system.

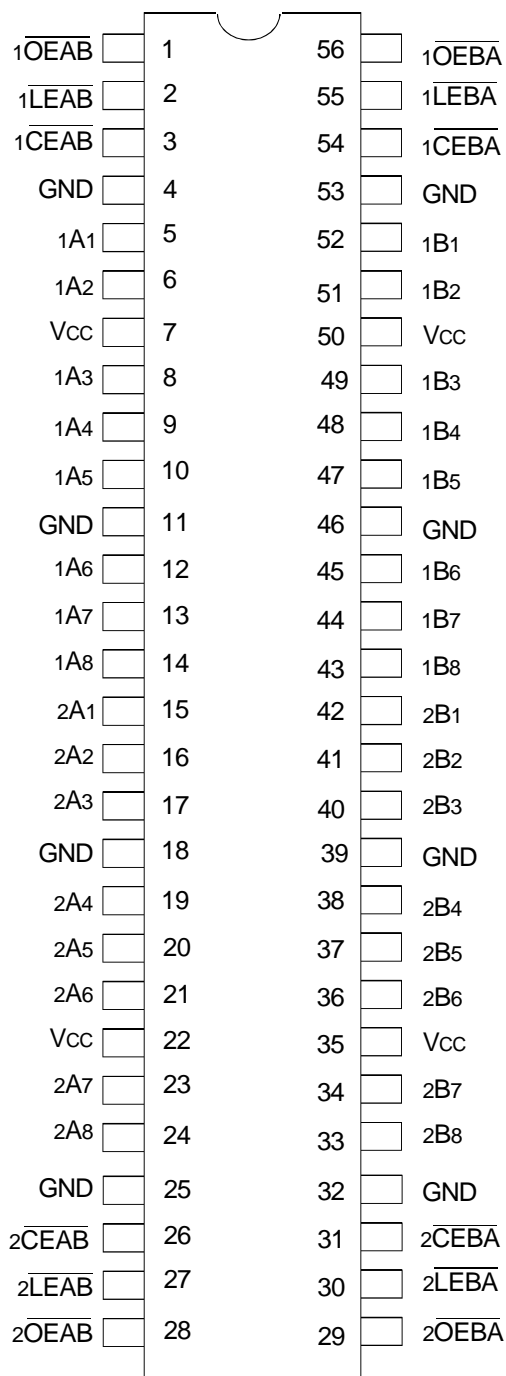
The LVC16543A has been designed with a $\pm 24mA$ output driver. This driver is capable of driving a moderate to heavy load while maintaining speed performance.

FUNCTIONAL BLOCK DIAGRAM



The IDT logo is a registered trademark of Integrated Device Technology, Inc.

PIN CONFIGURATION



SSOP/ TSSOP/ TVSOP
TOP VIEW

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Description	Max	Unit
VTERM	Terminal Voltage with Respect to GND	-0.5 to +6.5	V
TSTG	Storage Temperature	-65 to +150	°C
I _{OUT}	DC Output Current	-50 to +50	mA
I _{IK} I _{OK}	Continuous Clamp Current, V _I < 0 or V _O < 0	-50	mA
I _{CC} I _{SS}	Continuous Current through each V _{CC} or GND	±100	mA

NOTE:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (T_A = +25°C, F = 1.0MHz)

Symbol	Parameter ⁽¹⁾	Conditions	Typ.	Max.	Unit
C _{IN}	Input Capacitance	V _{IN} = 0V	4.5	6	pF
C _{OUT}	Output Capacitance	V _{OUT} = 0V	6.5	8	pF
C _{I/O}	I/O Port Capacitance	V _{IN} = 0V	6.5	8	pF

NOTE:

- As applicable to the device type.

PIN DESCRIPTION

Pin Names	Description
x \overline{OEAB}	A-to-B Output Enable Input (Active LOW)
x \overline{OEBA}	B-to-A Output Enable Input (Active LOW)
x \overline{CEAB}	A-to-B Enable Input (Active LOW)
x \overline{CEBA}	B-to-A Enable Input (Active LOW)
x \overline{LEAB}	A-to-B Latch Enable Input (Active LOW)
x \overline{LEBA}	B-to-A Latch Enable Input (Active LOW)
xAx	A-to-B Data Inputs or B-to-A 3-State Outputs
xBx	B-to-A Data Inputs or A-to-B 3-State Outputs

FUNCTION TABLE (EACH 8-BIT SECTION)^(1,2)

Inputs				Outputs
x \overline{CEAB}	x \overline{LEAB}	x \overline{OEAB}	xAx	xBx
H	X	X	X	Z
X	X	H	X	Z
L	H	L	X	B ⁽³⁾
L	L	L	L	L
L	L	L	H	H

NOTES:

- H = HIGH Voltage Level
X = Don't Care
L = LOW Voltage Level
Z = High-Impedance
- A-to-B data flow is shown. B-to-A data flow is similar but uses \overline{CEBA} , \overline{LEBA} , and \overline{OEBA} .
- Output level before the indicated steady-state input conditions were established.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Operating Condition: $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$

Symbol	Parameter	Test Conditions		Min.	Typ. ⁽¹⁾	Max.	Unit
V _{IH}	Input HIGH Voltage Level	V _{CC} = 2.3V to 2.7V		1.7	—	—	V
		V _{CC} = 2.7V to 3.6V		2	—	—	
V _{IL}	Input LOW Voltage Level	V _{CC} = 2.3V to 2.7V		—	—	0.7	V
		V _{CC} = 2.7V to 3.6V		—	—	0.8	
I _{IH} I _{IL}	Input Leakage Current	V _{CC} = 3.6V	V _I = 0 to 5.5V	—	—	±5	μA
I _{OZH} I _{OZL}	High Impedance Output Current (3-State Output pins)	V _{CC} = 3.6V	V _O = 0 to 5.5V	—	—	±10	μA
I _{OFF}	Input/Output Power Off Leakage	V _{CC} = 0V, V _{IN} or V _O ≤ 5.5V		—	—	±50	μA
V _{IK}	Clamp Diode Voltage	V _{CC} = 2.3V, I _{IN} = -18mA		—	-0.7	-1.2	V
V _H	Input Hysteresis	V _{CC} = 3.3V		—	100	—	mV
I _{CCL} I _{CCH} I _{CCZ}	Quiescent Power Supply Current	V _{CC} = 3.6V	V _{IN} = GND or V _{CC}	—	—	10	μA
			$3.6 \leq V_{IN} \leq 5.5V^{(2)}$	—	—	10	
ΔI _{CC}	Quiescent Power Supply Current Variation	One input at V _{CC} - 0.6V, other inputs at V _{CC} or GND		—	—	500	μA

NOTES:

1. Typical values are at V_{CC} = 3.3V, +25°C ambient.
2. This applies in the disabled state only.

OUTPUT DRIVE CHARACTERISTICS

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Max.	Unit
V _{OH}	Output HIGH Voltage	V _{CC} = 2.3V to 3.6V	I _{OH} = -0.1mA	V _{CC} - 0.2	—	V
		V _{CC} = 2.3V	I _{OH} = -6mA	2	—	
		V _{CC} = 2.3V	I _{OH} = -12mA	1.7	—	
		V _{CC} = 2.7V		2.2	—	
		V _{CC} = 3V		2.4	—	
		V _{CC} = 3V		2.2	—	
V _{OL}	Output LOW Voltage	V _{CC} = 2.3V to 3.6V	I _{OL} = 0.1mA	—	0.2	V
		V _{CC} = 2.3V	I _{OL} = 6mA	—	0.4	
			I _{OL} = 12mA	—	0.7	
		V _{CC} = 2.7V	I _{OL} = 12mA	—	0.4	
		V _{CC} = 3V	I _{OL} = 24mA	—	0.55	

NOTE:

1. V_{IH} and V_{IL} must be within the min. or max. range shown in the DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE table for the appropriate V_{CC} range. T_A = -40°C to +85°C.

OPERATING CHARACTERISTICS, $V_{CC} = 3.3V \pm 0.3V$, $T_A = 25^\circ C$

Symbol	Parameter	Test Conditions	Typical	Unit
CPD	Power Dissipation Capacitance per Transceiver Outputs enabled	$C_L = 0pF$, $f = 10MHz$	44	pF
CPD	Power Dissipation Capacitance per Transceiver Outputs disabled		4	

SWITCHING CHARACTERISTICS⁽¹⁾

Symbol	Parameter	$V_{CC} = 2.7V$		$V_{CC} = 3.3V \pm 0.3V$		Unit
		Min.	Max.	Min.	Max.	
t _{PLH} t _{PHL}	Propagation Delay xAx to xBx or xBx to xAx	—	6.1	1.2	5.4	ns
t _{PLH} t _{PHL}	Propagation Delay \overline{xLEBA} or \overline{xLEAB} to xAx or xBx	—	7.4	1.5	6.1	ns
t _{PZH} t _{PZL}	Output Enable Time \overline{xCEBA} or \overline{xCEAB} to xAx or xBx	—	7.9	1.2	6.6	ns
t _{PZH} t _{PZL}	Output Enable Time \overline{xOEBA} or \overline{xOEAB} to xAx or xBx	—	7.6	1	6.3	ns
t _{PHZ} t _{PLZ}	Output Disable Time \overline{xCEBA} or \overline{xCEAB} to xAx or xBx	—	7.1	1.5	6.6	ns
t _{PHZ} t _{PLZ}	Output Disable Time \overline{xOEBA} or \overline{xOEAB} to xAx or xBx	—	6.9	1.5	6.3	ns
t _{SU}	Set-up Time, data before $\overline{CE} \uparrow$	1.1	—	1.1	—	ns
t _{SU}	Set-up Time, data before $\overline{LE} \uparrow$, \overline{CE} LOW	1.1	—	1.1	—	ns
t _H	Hold Time, data after $\overline{CE} \uparrow$	1.9	—	1.9	—	ns
t _H	Hold Time, data after $\overline{LE} \uparrow$, \overline{CE} LOW	1.9	—	1.9	—	ns
t _W	Pulse Duration, \overline{xLEBA} or \overline{xLEAB} , \overline{xCEBA} or \overline{xCEAB} LOW	3.3	—	3.3	—	ns
t _{SK(O)}	Output Skew ⁽²⁾	—	—	—	500	ps

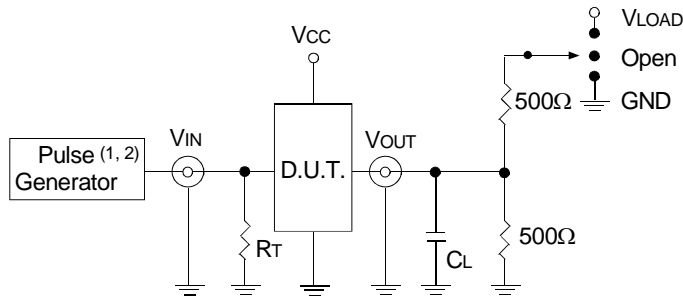
NOTES:

1. See TEST CIRCUITS AND WAVEFORMS. $T_A = -40^\circ C$ to $+85^\circ C$.
2. Skew between any two outputs of the same package and switching in the same direction.

TEST CIRCUITS AND WAVEFORMS

TEST CONDITIONS

Symbol	V _{CC} ⁽¹⁾ =3.3V±0.3V	V _{CC} ⁽¹⁾ =2.7V	V _{CC} ⁽²⁾ =2.5V±0.2V	Unit
V _{LOAD}	6	6	2 x V _{CC}	V
V _{IH}	2.7	2.7	V _{CC}	V
V _T	1.5	1.5	V _{CC} / 2	V
V _{LZ}	300	300	150	mV
V _{HZ}	300	300	150	mV
C _L	50	50	30	pF



Test Circuit for All Outputs

DEFINITIONS:

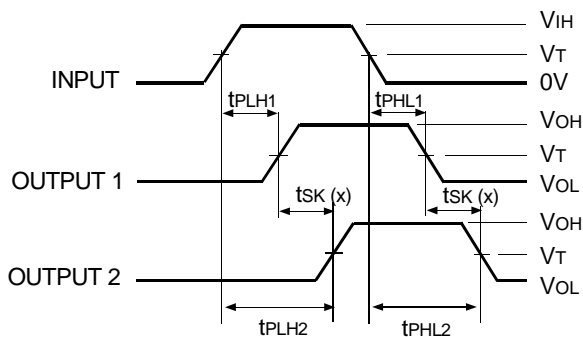
C_L = Load capacitance: includes jig and probe capacitance.
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

NOTES:

1. Pulse Generator for All Pulses: Rate ≤ 10MHz; t_F ≤ 2.5ns; t_R ≤ 2.5ns.
2. Pulse Generator for All Pulses: Rate ≤ 10MHz; t_F ≤ 2ns; t_R ≤ 2ns.

SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	V _{LOAD}
Disable High Enable High	GND
All Other Tests	Open

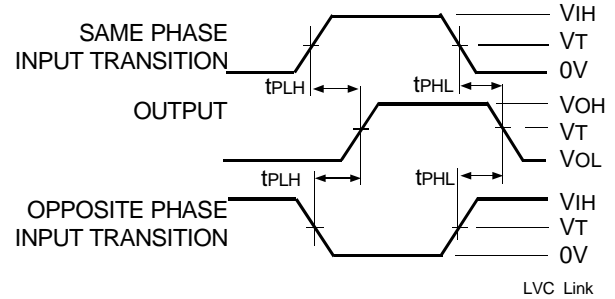


$$tsk(x) = |t_{PLH2} - t_{PLH1}| \text{ or } |t_{PHL2} - t_{PHL1}|$$

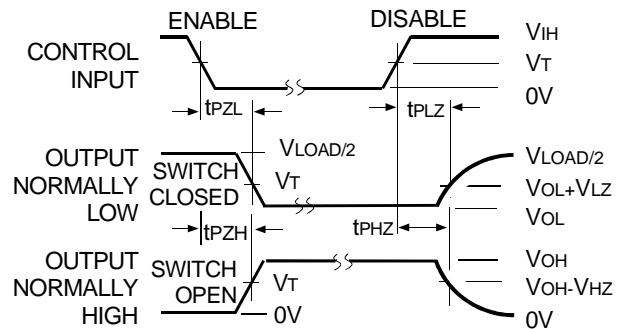
Output Skew - tsk(x)

NOTES:

1. For tsk(o) OUTPUT1 and OUTPUT2 are any two outputs.
2. For tsk(b) OUTPUT1 and OUTPUT2 are in the same bank.



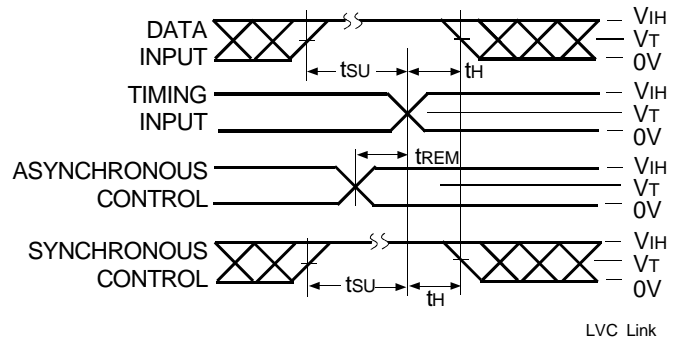
Propagation Delay



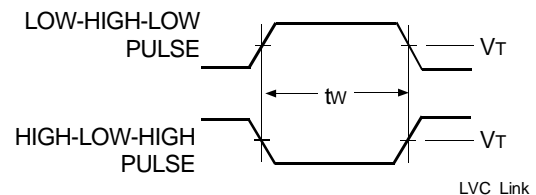
Enable and Disable Times

NOTE:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.

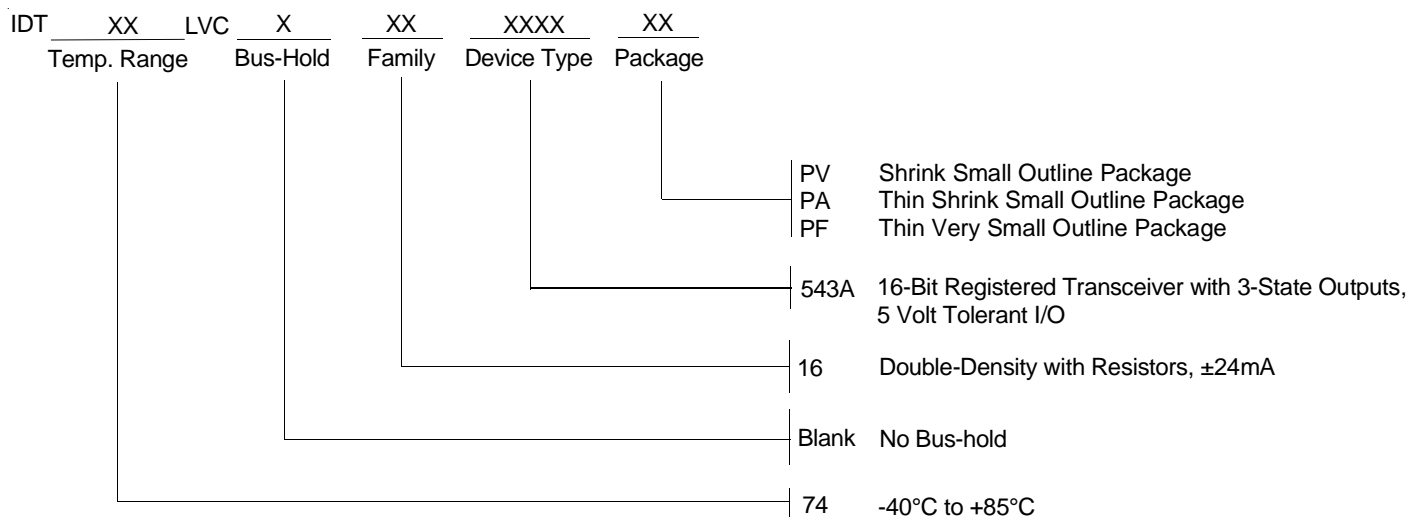


Set-up, Hold, and Release Times



Pulse Width

ORDERING INFORMATION



CORPORATE HEADQUARTERS
 2975 Stender Way
 Santa Clara, CA 95054

for SALES:
 800-345-7015 or 408-727-6116
 fax: 408-492-8674
 www.idt.com

for Tech Support:
 logichelp@idt.com
 (408) 654-6459