National Semiconductor

MM54HCT157/MM74HCT157 Quad 2-Input Multiplexer
MM54HCT158/MM74HCT158 Quad 2-Input Multiplexer (Inverted Output)

General Description

These high speed QUAD 2-to-1 line data selector/multiplexers utilize advanced silicon-gate CMOS technology. They possess the high noise immunity and low power consumption of standard CMOS integrated circuits, as well as the ability to drive 10 LS-TTL loads.

These devices each consist of four 2-input digital multiplexers with common select and OUTPUT ENABLE inputs. On the MM54HCT157/MM74HCT157, when the OUTPUT ENABLE input is at logical "0" the four outputs assume the values as selected from the inputs. When the OUTPUT ENABLE input is at a logical "1" the outputs assume logical "0". The MM54HCT158/MM74HCT158 operates in the same manner, except that its outputs are inverted. Select decoding is done internally resulting in a single select input only. If enabled, the select input determines whether the A or B inputs get routed to their corresponding Y outputs.

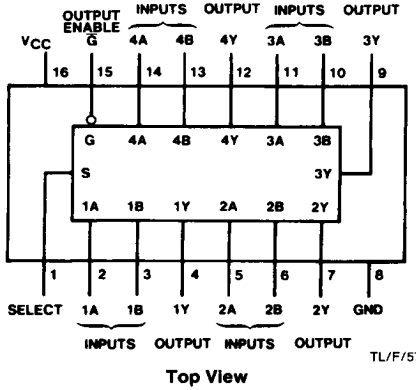
The 54HCT/74HCT logic family is functionally as well as pin-out compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical propagation delay: 14 ns data to any output
- Power supply range: 5V ± 10%
- Low power supply quiescent current: 80 μA maximum (74HCT Series)
- Low input current: 1 μA maximum
- Completely TTL compatible
- High output drive current: 60 mA minimum

Connection Diagrams

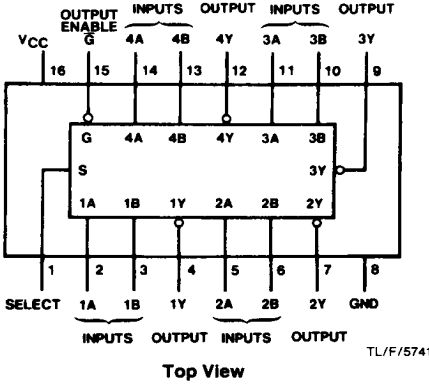
Dual-In-Line Package



TL/F/5741–1

Top View

Dual-In-Line Package



TL/F/5741–2

Top View

Order Number MM54HCT157/158* or MM74HCT157/158*

*Please look into Section 8, Appendix D for availability of various package types.

Function Table

Inputs				Output Y	
Strobe	Select	A	B	HCT157	HCT158
H	X	X	X	L	H
L	L	L	X	L	H
L	L	H	X	H	L
L	H	X	L	L	H
L	H	X	H	H	L

H = High Level, L = Low Level, X = Irrelevant

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC} +1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC} +0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D)	
(Note 3)	600 mW
S.O. Package only	500 mW
Lead Temperature (T_L)	
(Soldering, 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	4.5	5.5	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)			
MM74HCT	−40	+85	°C
MM54HCT	−55	+125	°C
Input Rise or Fall Times (t_r, t_f)		500	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A = 25°C	74HCT T_A = −40 to 85°C	54HCT T_A = −55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage				2.0	2.0	2.0	V
V_{IL}	Maximum Low Level Input Voltage				0.8	0.8	0.8	V
V_{OH}	Minimum High Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 20\ \mu A$	4.5V		4.4	4.4	4.4	V
		V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 6.0$ mA $\|I_{OUT}\| \leq 7.2$ mA	4.5V 5.5V	4.2 5.2	3.98 4.98	3.84 4.84	3.7 4.7	V V
V_{OL}	Maximum Low Level Voltage	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| = 20\ \mu A$ $\|I_{OUT}\| = 6.0$ mA $\|I_{OUT}\| = 7.2$ mA	 4.5V 5.5V	0 0.2 0.2	0.1 0.26 0.26	0.1 0.33 0.33	0.1 0.4 0.4	V V V
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND $I_{OUT} = 0\ \mu A$			8.0	80	160	μA
		V_{IN} = 2.4V or 0.5V (Note 4)			1.2	1.4	1.5	mA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HCT at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC} = 5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics $V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Data to Output		14	20	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Select to Output		14	20	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Strobe to Output		12	18	ns

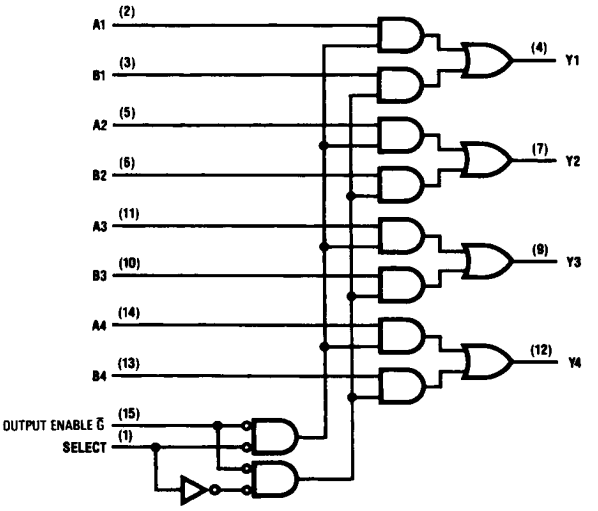
AC Electrical Characteristics $V_{CC}=5V\pm10\%$, $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	$T_A=25°C$		74HCT $T_A=-40$ to $85°C$	54HCT $T_A=-55$ to $125°C$	Units
			Typ	Guaranteed Limits			
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Data to Output		13	22	28	33	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Select to Output		15	27	34	41	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, OUTPUT ENABLE to Output		14	25	31	38	ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time		8	15	19	22	ns
C_{IN}	Maximum Input Capacitance		5	10	10	10	pF
C_{PD}	Power Dissipation Capacitance (Note 5)		48				pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}V_{CC}^2f+I_{CC}V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}V_{CC}f+I_{CC}$.

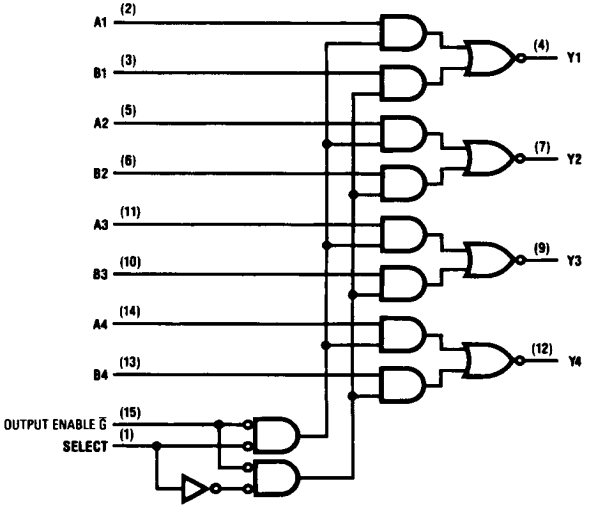
Logic Diagrams

'HCT157



TL/F/5741–3

'HCT158



TL/F/5741–4