

December 1997

Fast CMOS 3.3V 16-Bit Register (Three-State)

Features

- Advanced 0.6 micron CMOS Technology
- 5V Tolerant Inputs and Outputs
- Supports Live Insertion of PCBs
- 2.0V to 3.6V V_{CC} Supply Range
- Balanced 24mA Output Drive
- Low Ground Bounce Outputs
- ESD Protection Exceeds 2000V, HBM; 200V, MM
- Functionally Compatible with FCT3, LVC, LVT, and 74 Series Logic Families

Ordering Information

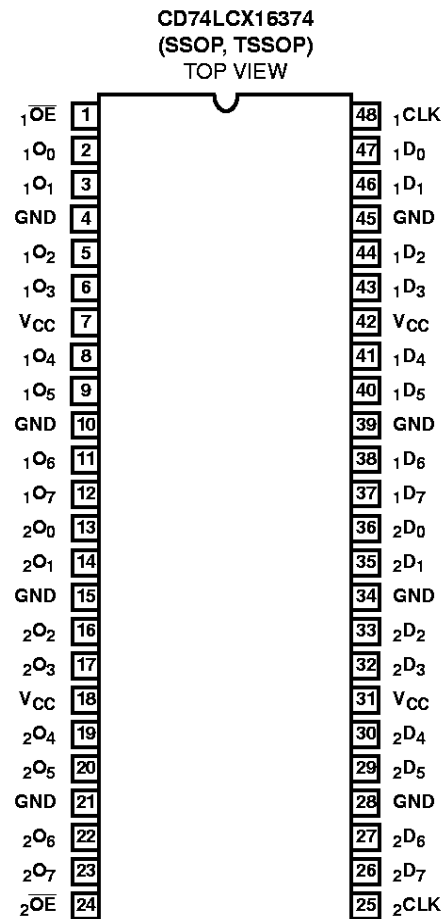
PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CD74LCX16374MT	-40 to 85	48 Ld TSSOP	M48.240-P
CD74LCX16374SM	-40 to 85	48 Ld SSOP	M48.300-P

Description

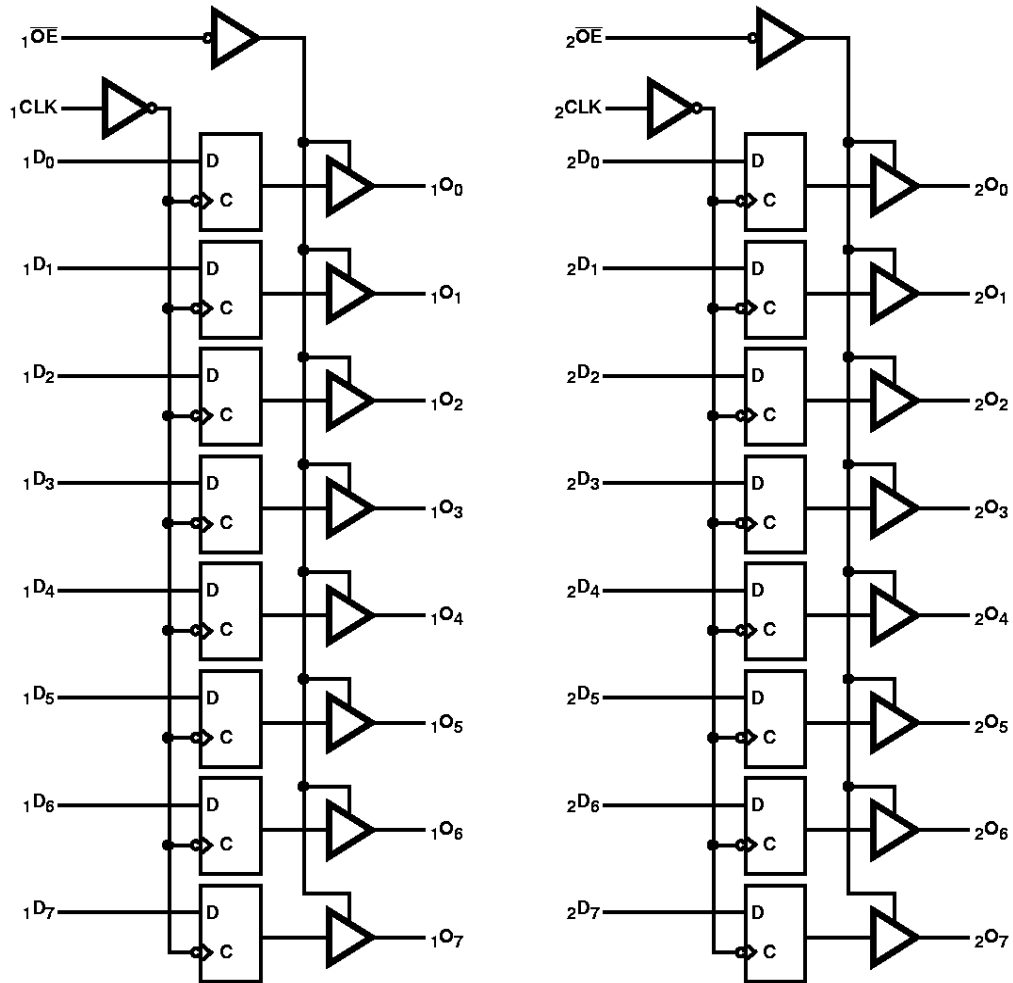
The CD74LCX16374 is a 16-bit octal register designed with 16 D-type flip-flops with a buffered common clock and three-state outputs. The Output Enable ($\overline{O\!E}$) and clock (\overline{CLK}) controls are organized to operate as two 8-bit registers or one 16-bit register. When $\overline{O\!E}$ is HIGH, the outputs are in the high impedance state. Input data meeting the setup and hold time requirements of the D inputs is transferred to the O outputs on the LOW-to-HIGH transition of the clock input.

The CD74LCX16374 can be driven from either 3.3V or 5.0V devices allowing this device to be used as a translator in a mixed 3.3/5.0V system.

Pinout



Functional Block Diagram



TRUTH TABLE (NOTE 1)

FUNCTION	INPUTS			OUTPUTS
	$x\overline{D}_x$	$x\overline{CLK}$	$x\overline{OE}$	xO_x
High-Z	X	L	H	Z
	X	H	H	Z
Load Register	L	↑	L	L
	H	↑	L	H
	L	↑	H	Z
	H	↑	H	Z

NOTE:

- 1. H = High Voltage Level
- L = Low Voltage Level
- X = Don't Care
- Z = High Impedance
- ↑ = LOW-to-HIGH Transition

Pin Descriptions

PIN NAME	DESCRIPTION
$x\overline{OE}$	Three-State Output Enable Inputs (Active LOW)
$x\overline{CLK}$	Clock Inputs
$x\overline{D}_x$	Data Inputs
xO_x	Three-State Outputs
GND	Ground
V_{CC}	Power

CD74LCX16374

Absolute Maximum Ratings

DC Input Voltage -0.5V to 7.0V
 DC Output Current 120mA

Operating Conditions

Temperature Range -40°C to 85°C
 Supply Voltage to Ground Potential
 Inputs and V_{CC} Only -0.5V to 7.0V
 Supply Voltage, V_{CC}
 Operating 2.0V (Min), 3.6V (Max)
 Data Retention 1.5V (Min), 3.6V (Max)
 Supply Voltage to Ground Potential
 Outputs and D/O Only -0.5V to 7.0V

Thermal Information

Thermal Resistance (Typical, Note 2) θ_{JA} (°C/W)
 TSSOP Package 94
 SSOP Package 76
 Maximum Junction Temperature 150°C
 Maximum Storage Temperature Range -65°C to 150°C
 Maximum Lead Temperature (Soldering 10s) 300°C
 (Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

- θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

PARAMETER	SYMBOL	(NOTE 3) TEST CONDITIONS		MIN	(NOTE 4) TYP	MAX	UNITS
DC ELECTRICAL SPECIFICATIONS Over the Operating Range, T _A = -40°C to 85°C, V _{CC} = 2.7V to 3.6V							
Input HIGH Voltage	V _{IH}	Guaranteed Logic HIGH Level		2.0	-	-	V
Input LOW Voltage (Input and I/O Pins)	V _{IL}	Guaranteed Logic LOW Level		-	-	0.8	V
Output HIGH Voltage	V _{OH}	V _{CC} = 2.7V to 3.6V	I _{OH} = -0.1mA	V _{CC} - 0.2	-	-	V
		V _{CC} = 2.7V	I _{OH} = -12mA	2.2	-	-	V
		V _{CC} = 3.0V	I _{OH} = -18mA	2.4	-	-	V
			I _{OH} = -24mA	2.2	-	-	V
Output LOW Voltage	V _{OL}	V _{CC} = 2.7V to 3.6V	I _{OL} = 0.1mA	-	-	0.2	V
		V _{CC} = 2.7V	I _{OL} = 12mA	-	-	0.4	V
		V _{CC} = 3V	I _{OL} = 16mA	-	-	0.4	V
			I _{OL} = 24mA	-	-	0.55	V
Clamp Diode Voltage	V _{IK}	V _{CC} = Min, I _{IN} = -18mA		-	-0.7	-1.2	V
Input Current	I _I	V _{CC} = 2.7V to 3.6V	0 ≤ V _I ≤ 5.5V	-	-	±5	μA
High Impedance Output Current (Three-State)	I _{OZ}	V _{CC} = 2.7V to 3.6V	0 ≤ V _O ≤ 5.5V V _I = V _{IH} or V _{IL}	-	-	±5	μA
Power Down Disable	I _{OFF}	V _{CC} = 0V	V _{IN} or V _{OUT} ≤ 5.5V	-	-	10	μA
Quiescent Power Supply Current	I _{CC}	V _{CC} = Max	V _{IN} = GND or V _{CC}	-	0.1	10	μA
Quiescent Power Supply Current TTL Inputs HIGH	ΔI _{CC}	V _{CC} = Max	V _{IN} = V _{CC} - 0.6V (Note 5)	-	-	500	μA
CAPACITANCE							
Input Capacitance (Note 6)	C _{IN}	V _{CC} = Open, V _{IN} = 0V or V _{CC}		-	7	-	pF
Output Capacitance (Note 6)	C _{OUT}	V _{CC} = 3.3V, V _{IN} = 0V or V _{CC}		-	8	-	pF
Power Dissipation Capacitance (Note 7)	C _{PD}	V _{CC} = 3.3V, V _{IN} = 0V or V _{CC} , f = 10MHz		-	20	-	pF

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Switching Specifications Over Operating Range

PARAMETER	SYMBOL	TEST CONDITIONS	V _{CC} = 3.3V ±0.3V		V _{CC} = 2.7V		UNITS
			MIN	MAX	MIN	MAX	
Maximum Clock Frequency	f _{MAX}	C _L = 50pF, R _L = 500Ω	170	-	-	-	MHz
Propagation Delay, CP to ON	t _{PHL} , t _{PLH}	C _L = 50pF, R _L = 500Ω	1.5	6.2	1.5	6.5	ns
Output Enable Time	t _{PZL} , t _{PZH}	C _L = 50pF, R _L = 500Ω	1.5	6.1	1.5	6.3	ns
Output Disable Time (Note 10)	t _{PLZ} , t _{PHZ}	C _L = 50pF, R _L = 500Ω	1.5	6.0	1.5	6.2	ns
Setup Time	t _S	C _L = 50pF, R _L = 500Ω	2.5	-	2.5	-	ns
Hold Time	t _H	C _L = 50pF, R _L = 500Ω	1.5	-	1.5	-	ns
Pulse Width (Note 10)	t _W	C _L = 50pF, R _L = 500Ω	3.0	-	3.0	-	ns
Output to Output Skew (Note 11)	t _{SK(O)}	C _L = 50pF, R _L = 500Ω	-	1.0	-	-	ns

Dynamic Switching Characteristics T_A = 25°C

PARAMETER	SYMBOL	(NOTE 12) TEST CONDITIONS	TYP	UNITS
Dynamic LOW Peak Voltage	V _{OLP}	V _{CC} = 3.3V, C _L = 50pF, V _{IH} = 3.3V, V _{IL} = 0V	0.8	V
Dynamic LOW Valley Voltage	V _{OLV}	V _{CC} = 3.3V, C _L = 50pF, V _{IH} = 3.3V, V _{IL} = 0V	0.8	V

NOTES:

3. For conditions shown as Max or Min, use appropriate value specified under Electrical Specifications for the applicable device type.
4. Typical values are at V_{CC} = 3.3V, 25°C ambient and maximum loading.
5. Per TTL driven input; all other inputs at V_{CC} or GND.
6. This parameter is determined by device characterization but is not production tested.
7. C_{PD} determines the no-load dynamic power consumption per latch. It is obtained by the following relationship:
P_D (total power per latch) = V_{CC}² f_i (C_{PD} + C_L) where f_i = input frequency, C_L = output load capacitance, V_{CC} = supply range.
8. See test circuit and waveforms.
9. Minimum limits are guaranteed but not tested on Propagation Delays.
10. This parameter is guaranteed but not production tested.
11. Skew between any two outputs, of the same package, switching in the same direction. This parameter is guaranteed by design.
12. Measured with n-1 outputs switching from High-to-Low or Low-to-High. The remaining output is measured in the LOW state.