

Quad 3-State D Flip-Flop with Common Clock and Reset

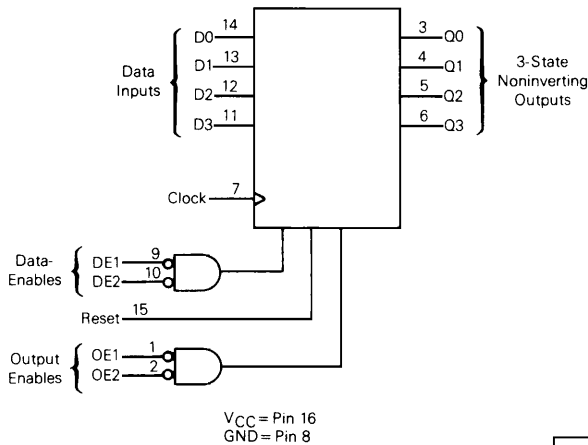
High-Performance Silicon-Gate CMOS

The MC54/74HC173 is identical in pinout to the LS173. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

Data, when enabled, are clocked into the four D flip-flops with the rising edge of the common Clock. When either or both of the Output Enable Controls is high, the outputs are in a high-impedance state. This feature allows the HC173 to be used in bus-oriented systems. The Reset feature is asynchronous and active-high.

- Output Drive Capability: 15 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 208 FETs or 52 Equivalent Gates

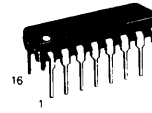
LOGIC DIAGRAM



MC54/74HC173



J SUFFIX
CERAMIC
CASE 620-09



N SUFFIX
PLASTIC
CASE 648-06



D SUFFIX
SOIC
CASE 751B-03

ORDERING INFORMATION

MC74HCXXXN	Plastic
MC54HCXXXJ	Ceramic
MC74HCXXXD	SOIC

T_A = -55° to 125°C for all packages.
 Dimensions in Chapter 6.

PIN ASSIGNMENT

OE1	1	16	V _{CC}
OE2	2	15	Reset
Q0	3	14	D0
Q1	4	13	D1
Q2	5	12	D2
Q3	6	11	D3
Clock	7	10	DE2
GND	8	9	DE1

FUNCTION TABLE

Output Enables		Inputs					Output
OE1	OE2	Reset	Clock	Data Enables		Data D	Q
OE1	OE2	Reset	Clock	DE1	DE2	Data D	Q
L	L	H	X	X	X	X	L
L	L	L	L	X	X	X	no change
L	L	L	H	X	X	X	no change
L	L	L	↗	H	X	X	no change
L	L	L	↘	X	H	X	no change
L	L	L	↗	L	L	L	L
L	L	L	↘	L	L	H	H
L	L	L	↔	X	X	X	no change
L	H	X	X	X	X	X	high impedance
H	L	X	X	X	X	X	high impedance
H	H	X	X	X	X	X	high impedance

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MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V _{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V _{in}	DC Input Voltage (Referenced to GND)	-1.5 to V _{CC} +1.5	V
V _{out}	DC Output Voltage (Referenced to GND)	-0.5 to V _{CC} +0.5	V
I _{in}	DC Input Current, per Pin	±20	mA
I _{out}	DC Output Current, per Pin	±35	mA
I _{CC}	DC Supply Current, V _{CC} and GND Pins	±75	mA
P _D	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T _{stg}	Storage Temperature	-65 to +150	°C
T _L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: -10 mW/°C from 65° to 125°C

Ceramic DIP: -10 mW/°C from 100° to 125°C

SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit	
V _{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V	
V _{in} , V _{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V _{CC}	V	
T _A	Operating Temperature, All Package Types	-55	+125	°C	
t _r , t _f	Input Rise and Fall Time (Figure 1)	V _{CC} = 2.0 V V _{CC} = 4.5 V V _{CC} = 6.0 V	0 0 0	1000 500 400	ns

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V _{CC} V	Guaranteed Limit			Unit				
				25°C to -55°C	≤85°C	≤125°C					
V _{IH}	Minimum High-Level Input Voltage	V _{out} = 0.1 V or V _{CC} - 0.1 V I _{out} ≤ 20 μA	2.0	1.5	1.5	1.5	V				
			4.5	3.15	3.15	3.15					
			6.0	4.2	4.2	4.2					
V _{IL}	Maximum Low-Level Input Voltage	V _{out} = 0.1 V or V _{CC} - 0.1 V I _{out} ≤ 20 μA	2.0	0.3	0.3	0.3	V				
			4.5	0.9	0.9	0.9					
			6.0	1.2	1.2	1.2					
V _{OH}	Minimum High-Level Output Voltage	V _{in} = V _{IH} or V _{IL} I _{out} ≤ 20 μA	2.0	1.9	1.9	1.9	V				
			4.5	4.4	4.4	4.4					
			6.0	5.9	5.9	5.9					
V _{OL}	Maximum Low-Level Output Voltage	V _{in} = V _{IH} or V _{IL} I _{out} ≤ 20 μA	2.0	0.1	0.1	0.1	V				
			4.5	0.1	0.1	0.1					
			6.0	0.1	0.1	0.1					
I _{in}	Maximum Input Leakage Current	V _{in} = V _{CC} or GND	6.0	±0.1	±1.0	±1.0	μA				
			I _{OZ}	Maximum Three-State Leakage Current	Output in High-Impedance State V _{in} = V _{IL} or V _{IH} V _{out} = V _{CC} or GND	6.0		±0.5	±5.0	±10.0	μA
			I _{CC}			Maximum Quiescent Supply Current (per Package)		V _{in} = V _{CC} or GND I _{out} = 0 μA	6.0	8	

NOTE: Information on typical parametric values can be found in Chapter 4.

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AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input t_r = t_f = 6 ns)

Symbol	Parameter	V _{CC} V	Guaranteed Limit			Unit
			25°C to -55°C	≤ 85°C	≤ 125°C	
f _{max}	Maximum Clock Frequency (50% Duty Cycle) (Figures 1 and 5)	2.0	6.0	4.8	4.0	MHz
		4.5	30	24	20	
		6.0	35	28	24	
t _{PLH} , t _{PHL}	Maximum Propagation Delay, Clock to Q (Figures 1 and 5)	2.0	175	220	265	ns
		4.5	35	44	53	
		6.0	30	37	45	
t _{PHL}	Maximum Propagation Delay, Reset to Q (Figures 2 and 5)	2.0	150	190	225	ns
		4.5	30	38	45	
		6.0	26	33	38	
t _{PLZ} , t _{PHZ}	Maximum Propagation Delay, Output Enable to Q (Figures 3 and 6)	2.0	150	190	225	ns
		4.5	30	38	45	
		6.0	26	33	38	
t _{PZL} , t _{PZH}	Maximum Propagation Delay, Output Enable to Q (Figures 3 and 6)	2.0	150	190	225	ns
		4.5	30	38	45	
		6.0	26	33	38	
t _{TLH} , t _{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 5)	2.0	60	75	90	ns
		4.5	12	15	18	
		6.0	10	13	15	
C _{in}	Maximum Input Capacitance	—	10	10	10	pF
C _{out}	Maximum Three-State Output Capacitance (Output in High-Impedance State)	—	15	15	15	pF

NOTES:

1. For propagation delays with loads other than 50 pF, see Chapter 4.
2. Information on typical parametric values can be found in Chapter 4.

C _{PD}	Power Dissipation Capacitance (Per Flip-Flop) Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ For load considerations, see Chapter 4.	Typical @ 25°C, V _{CC} = 5.0 V	pF
		35	

TIMING REQUIREMENTS (Input t_r = t_f = 6 ns)

Symbol	Parameter	V _{CC} V	Guaranteed Limit			Unit
			25°C to -55°C	≤ 85°C	≤ 125°C	
t _{su}	Minimum Setup Time, Input D or DE to Clock (Figure 4)	2.0	100	125	150	ns
		4.5	20	25	30	
		6.0	17	21	26	
t _h	Minimum Hold Time, Clock to Input D or DE (Figure 4)	2.0	3	3	3	ns
		4.5	3	3	3	
		6.0	3	3	3	
t _{rec}	Minimum Recovery Time, Reset Inactive to Clock (Figure 2)	2.0	90	115	135	ns
		4.5	18	23	27	
		6.0	15	20	23	
t _w	Minimum Pulse Width, Clock (Figure 1)	2.0	80	100	120	ns
		4.5	16	20	24	
		6.0	14	17	20	
t _w	Minimum Pulse Width, Reset (Figure 2)	2.0	80	100	120	ns
		4.5	16	20	24	
		6.0	14	17	20	
t _r , t _f	Maximum Input Rise and Fall Times (Figure 1)	2.0	1000	1000	1000	ns
		4.5	500	500	500	
		6.0	400	400	400	

NOTE: Information on typical parametric values can be found in Chapter 4.

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PIN DESCRIPTIONS

INPUTS

D0, D1, D2, D3 (PINS 14, 13, 12, 11) – 4-bit data inputs. Data on these pins, when enabled by the Data-Enable Controls, are entered into the flip-flops on the rising edge of the clock.

CLOCK (PIN 7) – Clock input.

OUTPUTS

Q0, Q1, Q2, Q3 (PINS 3, 4, 5, 6) – 3-state register outputs. During normal operation of the device, the outputs of the D flip-flops appear at these pins. During 3-state operation, these outputs assume a high-impedance state.

CONTROL INPUTS

RESET (PIN 15) – Asynchronous reset input. A high level

on this pin resets all flip-flops and forces the Q outputs low, if they are not already in high-impedance state.

DE1, DE2 (Pins 9, 10) – Active-low Data Enable Control inputs. When both Data Enable Controls are low, data at the D inputs are loaded into the flip-flops with the rising edge of the Clock input. When either or both of these controls are high, there is no change in the state of the flip-flops, regardless of any changes at the D or Clock inputs.

OE1, OE2 (Pins 1, 2) – Output Enable Control inputs. When either or both of the Output Enable Controls are high, the Q outputs of the device are in the high-impedance state. When both controls are low, the device outputs display the data in the flip-flops.

SWITCHING WAVEFORMS

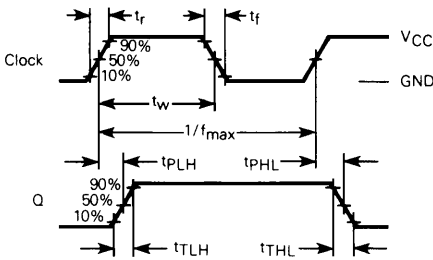


Figure 1.

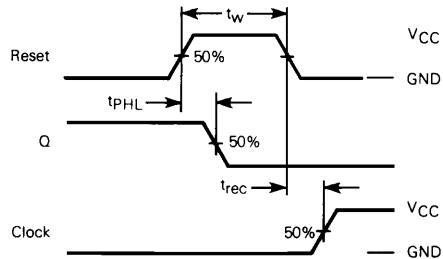


Figure 2.

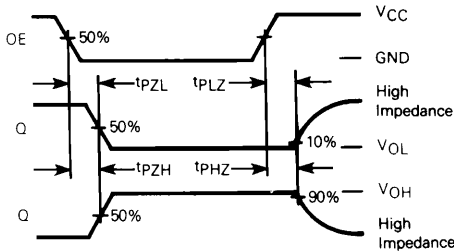


Figure 3.

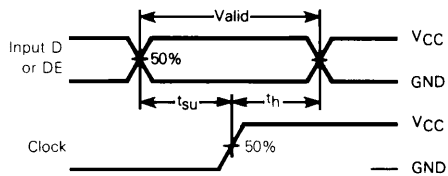
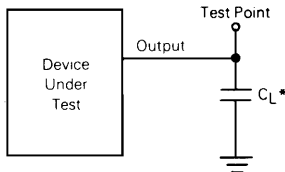


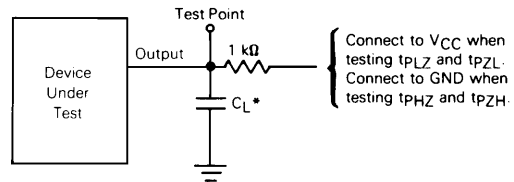
Figure 4.

TEST CIRCUITS



* Includes all probe and jig capacitance.

Figure 5.

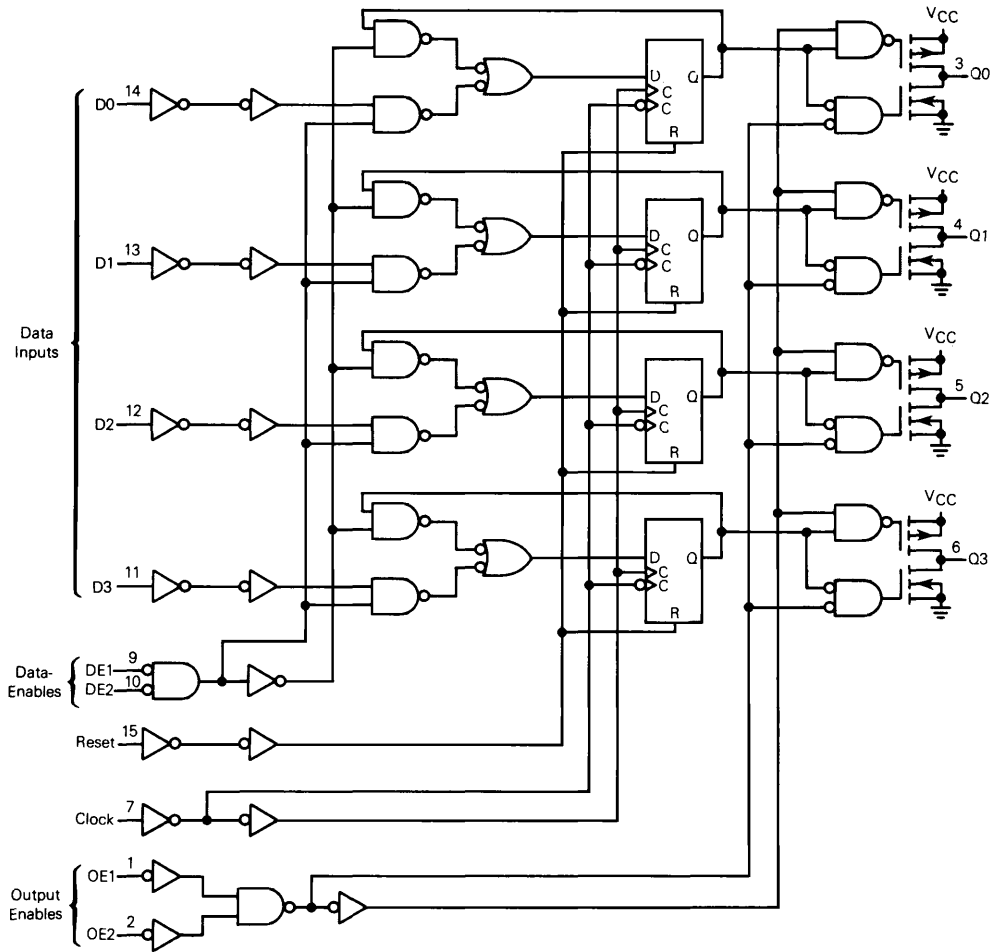


* Includes all probe and jig capacitance.

Figure 6.

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LOGIC DETAIL



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