MOTOROLA

MC14551B

QUAD 2-CHANNEL ANALOG MULTIPLEXER/DEMULTIPLEXER

The MC14551B is a digitally-controlled analog switch. This device implements a 4PDT solid state switch with low ON impedance and very low OFF Leakage current. Control of analog signals up to the complete supply voltage range can be achieved.

- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Analog Voltage Range (V_{DD}-V_{EE}) = 3 to 18 V
  Note: V_{EE} must be ≤ V_{SS}
- Linearized Transfer Characteristics
- Low Noise — 12 nV/ $\sqrt{Cycle}$, $f \geq 1$ kHz typical
- For Lower R_{ON}, Use The HC4051, HC4052, or HC4053 High-Speed CMOS Devices

MAXIMUM RATINGS*

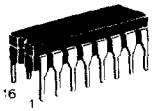
Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage (Referenced to V_{EE}. $V_{SS} \geq V_{EE}$)	−0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage (DC or Transient) (Referenced to V_{SS} for Control Input & V_{EE} for Switch I/O)	−0.5 to V_{DD} +0.5	V
I_{in}	Input Current (DC or Transient), per Control Pin	±10	mA
I_{sw}	Switch Through Current	±25	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature (8-Second Soldering)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
†Temperature Derating: Plastic "P" Package: −12mW/°C from 65°C to 85°C
Ceramic "L" Package: −12mW/°C from 100°C to 125°C

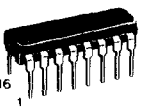
CMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

ANALOG MULTIPLEXER/ DEMULTIPLEXER



CASE 620
L SUFFIX
CERAMIC PACKAGE

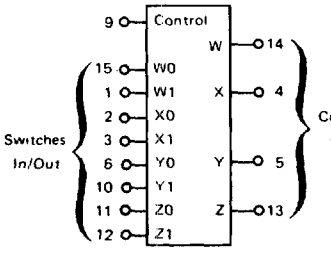


CASE 648
P SUFFIX
PLASTIC PACKAGE

ORDERING INFORMATION

A Series: −55°C to +125°C
MC14XXXBAL (Ceramic Package Only)

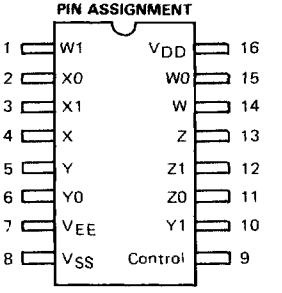
C Series: −40°C to +85°C
MC14XXXBCP (Plastic Package)
MC14XXXBCL (Ceramic Package)



Control	ON
0	W0 X0 Y0 Z0
1	W1 X1 Y1 Z1

V_{DD} = Pin 16
V_{SS} = Pin 8
V_{EE} = Pin 7

PIN ASSIGNMENT



Note: Control Input referenced to V_{SS}, Analog Inputs and Outputs reference to V_{EE}. V_{EE} must be ≤ V_{SS}

6

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD}	Test Conditions	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ#	25°C Max	T_{high}* Min	T_{high}* Max	Unit
SUPPLY REQUIREMENTS (Voltages Referenced to V_{EE})											
Power Supply Voltage Range	V_{DD}	—	$V_{DD} - 3 \geq V_{SS} \geq V_{EE}$	3	18	3	—	18	3	18	V
Quiescent Current Per Package (AL Device)	I_{DD}	5	Control Inputs: $V_{in} = V_{SS}$ or V_{DD},	—	5	—	0.005	5	—	150	µA
		10	Switch I/O: $V_{EE} \leq V_{I/O} \leq V_{DD}$,	—	10	—	0.010	10	—	300	
		15	and $\Delta V_{switch} \leq 500$ mV**	—	20	—	0.015	20	—	600	
Quiescent Current Per Package (CL/CP Device)	I_{DD}	5	Control Inputs: $V_{in} = V_{SS}$ or V_{DD},	—	20	—	0.005	20	—	150	µA
		10	Switch I/O: $V_{EE} \leq V_{I/O} \leq V_{DD}$,	—	40	—	0.010	40	—	300	
		15	and $\Delta V_{switch} \leq 500$ mV**	—	80	—	0.015	80	—	600	
Total Supply Current (Dynamic Plus Quiescent, Per Package)	$I_{D(AV)}$	5	$T_A = 25°C$ only	Typical			(0.07 µA/kHz)f + I_{DD}				µA
		10	(The channel component,				(0.20 µA/kHz)f + I_{DD}				
		15	$(V_{in} - V_{out})/R_{on}$, is not included.)				(0.36 µA/kHz)f - I_{DD}				
CONTROL INPUT (Voltages Referenced to V_{SS})											
Low-Level Input Voltage	V_{IL}	5	R_{on} = per spec,	—	1.5	—	2.25	1.5	—	1.5	V
		10	I_{off} = per spec	—	3.0	—	4.50	3.0	—	3.0	
		15		—	4.0	—	6.75	4.0	—	4.0	
High-Level Input Voltage	V_{IH}	5	R_{on} = per spec,	3.5	—	3.5	2.75	—	3.5	—	V
		10	I_{off} = per spec	7.0	—	7.0	5.50	—	7.0	—	
		15		11.0	—	11.0	8.25	—	11.0	—	
Input Leakage Current (AL Device)	I_{in}	15	$V_{in} = 0$ or V_{DD}	—	±0.1	—	±0.00001	±0.1	—	±1.0	µA
Input Leakage Current (CL/CP Device)	I_{in}	15	$V_{in} = 0$ or V_{DD}	—	±0.3	—	±0.00001	±0.3	—	±1.0	µA
Input Capacitance	C_{in}	—		—	—	—	5.0	7.5	—	—	pF
SWITCHES IN/OUT AND COMMONS OUT/IN - W, X, Y, Z (Voltages Referenced to V_{EE})											
Recommended Peak-to-Peak Voltage Into or Out of the Switch	$V_{I/O}$	—	Channel On or Off	0	V_{DD}	0	—	V_{DD}	0	V_{DD}	V_{p-p}
Recommended Static or Dynamic Voltage Across the Switch** (Figure 3)	ΔV_{switch}	—	Channel On	0	600	0	—	600	0	300	mV
Output Offset Voltage	V_{OO}	—	$V_{in} = 0$ V, No load	—	—	—	10	—	—	—	µV
ON Resistance (AL Device)	R_{on}	5	$\Delta V_{switch} \leq 500$ mV**,	—	800	—	250	1050	—	1300	Ω
		10	$V_{in} = V_{IL}$ or V_{IH} (Control),	—	400	—	120	500	—	550	
		15	and $V_{in} = 0$ to V_{DD} (Switch)	—	220	—	80	280	—	320	
ON Resistance (CL/CP Device)	R_{on}	5	$\Delta V_{switch} \leq 500$ mV**,	—	880	—	250	1050	—	1200	Ω
		10	$V_{in} = V_{IL}$ or V_{IH} (Control),	—	450	—	120	500	—	520	
		15	and $V_{in} = 0$ to V_{DD} (Switch)	—	250	—	80	280	—	300	
Δ ON Resistance Between Any Two Channels in the Same Package	ΔR_{on}	5		—	70	—	25	70	—	135	Ω
		10		—	50	—	10	50	—	95	
		15		—	45	—	10	45	—	65	
Off-Channel Leakage Current (AL Device) (Figure 8)	I_{off}	15	$V_{in} = V_{IL}$ or V_{IH} (Control) Channel to Channel or Any One Channel	—	±100	—	±0.05	±100	—	±1000	nA
Off-Channel Leakage Current (CL/CP Device) (Figure 8)	I_{off}	15	$V_{in} = V_{IL}$ or V_{IH} (Control) Channel to Channel or Any One Channel	—	±300	—	±0.05	±300	—	±1000	nA
Capacitance, Switch I/O	$C_{I/O}$	—	Switch Off	—	—	—	10	—	—	—	pF
Capacitance, Common O/I	$C_{O/I}$	—		—	—	—	17	—	—	—	pF
Capacitance, Feedthrough (Channel Off)	$C_{I/O}$	—	Pins Not Adjacent	—	—	—	0.15	—	—	—	pF
		—	Pins Adjacent	—	—	—	0.47	—	—	—	

* T_{low} = −55°C for AL Device, −40° for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.

 # Data labeled "Typ" is not to be used for design purposes, but is intended as an indication of the IC's potential performance.

**For voltage drops across the switch (ΔV_{switch}) >600 mV (>300 mV at high temperature), excessive V_{DD} current may be drawn; i.e. the current out of the switch may contain both V_{DD} and switch input components. The reliability of the device will be unaffected unless the Maximum Ratings are exceeded. (See first page of this data sheet.)

ELECTRICAL CHARACTERISTICS ($C_L = 50$ pF, $T_A = 25°C$, $V_{EE} \leq V_{SS}$)

Characteristic	Symbol	$V_{DD} - V_{EE}$ Vdc	Min	Typ #	Max	Unit
Propagation Delay Times Switch Input to Switch Output (R_L = 10 kΩ) t_{PLH}, t_{PHL} = (0.17 ns/pF) C_L + 26.5 ns t_{PLH}, t_{PHL} = (0.08 ns/pF) C_L + 11 ns t_{PLH}, t_{PHL} = (0.06 ns/pF) C_L + 9.0 ns	t_{PLH}, t_{PHL}	 5.0 10 15	 — — —	 35 15 12	 90 40 30	ns
Control Input to Output (R_L = 10 kΩ) $V_{EE} = V_{SS}$ (Figure 4)	t_{PLH}, t_{PHL}	 5.0 10 15	 — — —	 350 140 100	 875 350 250	ns
Second Harmonic Distortion R_L = 10 kΩ, f = 1 kHz, V_{in} = 5 V_{p-p}	—	10	—	0.07	—	%
Bandwidth (Figure 5) R_L = 1 kΩ, V_{in} = 1/2 ($V_{DD} - V_{EE}$) p-p, 20 Log $\frac{V_{out}}{V_{in}}$ = −3 dB, C_L = 50 pF	BW	10	—	17	—	MHz
Off Channel Feedthrough Attenuation, Figure 5 R_L = 1 kΩ, V_{in} = 1/2 ($V_{DD} - V_{EE}$) p-p, f_{in} = 55 MHz	—	10	—	−50	—	dB
Channel Separation (Figure 6) R_L = 1 kΩ, V_{in} = 1/2 ($V_{DD} - V_{EE}$) p-p, f_{in} = 3 MHz	—	10	—	−50	—	dB
Crosstalk, Control Input to Common O/I, Figure 7 R1 = 1 kΩ, R_L = 10 kΩ, Control $t_r = t_f$ = 20 ns	—	10	—	75	—	mV

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$ for control inputs and $V_{EE} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$ for Switch I/O.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS}, V_{EE}, or V_{DD}). Unused outputs must be left open.

FIGURE 1 – SWITCH CIRCUIT SCHEMATIC

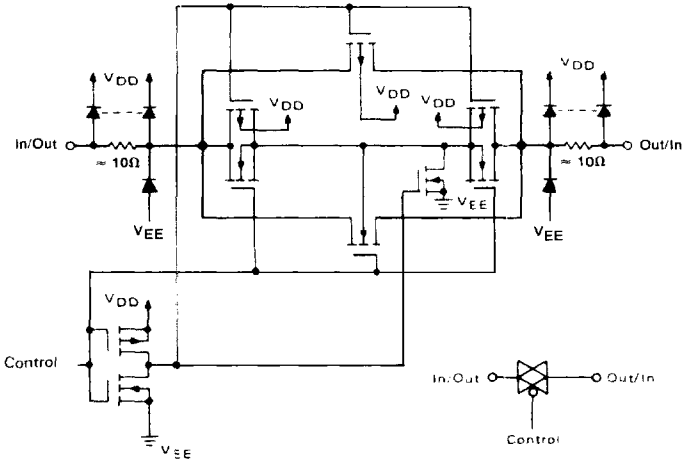
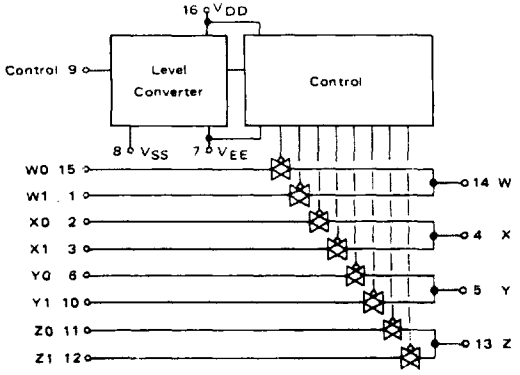


FIGURE 2 – MC14551B FUNCTIONAL DIAGRAM



6

TEST CIRCUITS

FIGURE 3 — ΔV ACROSS SWITCH

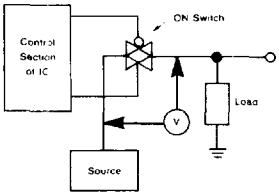


FIGURE 4 — PROPAGATION DELAY TIMES, CONTROL TO OUTPUT

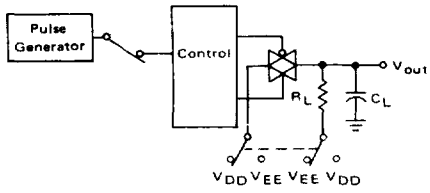


FIGURE 5 — BANDWIDTH AND OFF-CHANNEL FEEDTHROUGH ATTENUATION

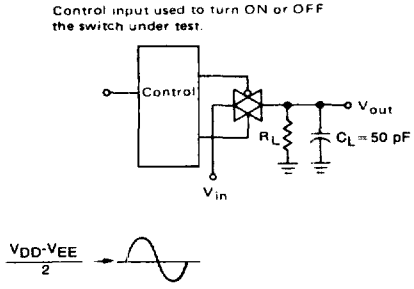


FIGURE 6 — CHANNEL SEPARATION (Adjacent Channels Used for Setup)

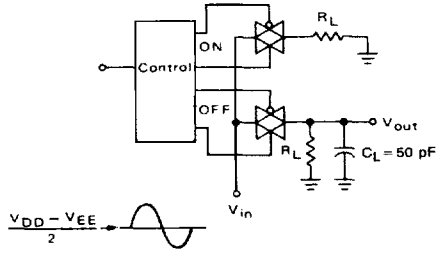


FIGURE 7 — CROSSTALK, CONTROL INPUT TO COMMON O/I

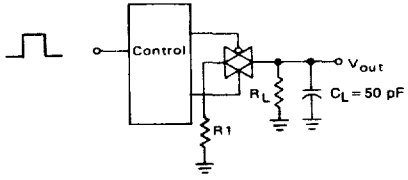
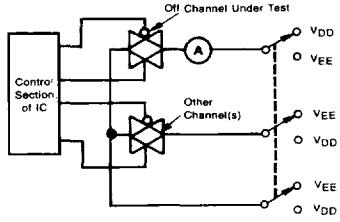
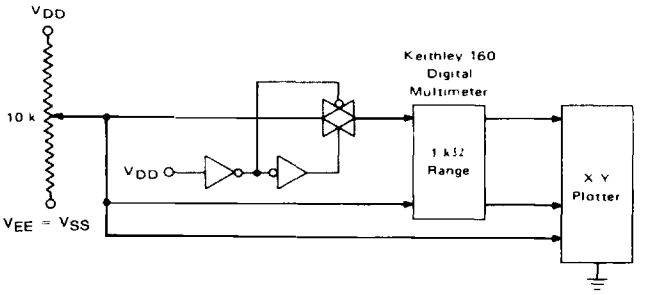


FIGURE 8 — OFF CHANNEL LEAKAGE



6

FIGURE 9 – CHANNEL RESISTANCE (R_{ON}) TEST CIRCUIT



TYPICAL RESISTANCE CHARACTERISTICS

FIGURE 10 – V_{DD} @ 7.5 V, V_{EE} @ –7.5V

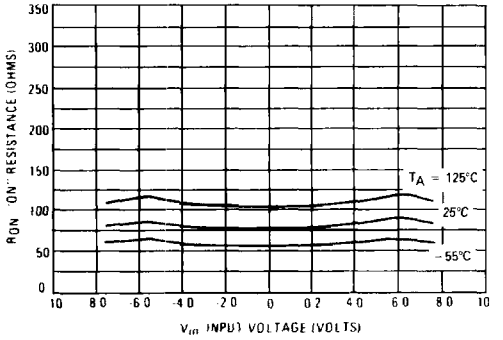


FIGURE 11 – V_{DD} @ 5.0V, V_{EE} @ –5.0 V

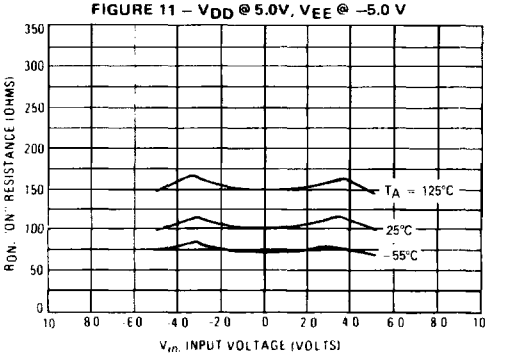


FIGURE 12 – V_{DD} @ 2.5 V, V_{EE} @ –2.5 V

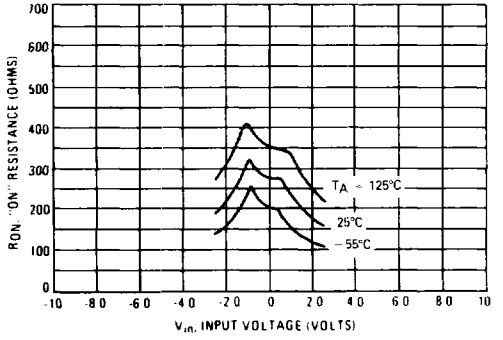
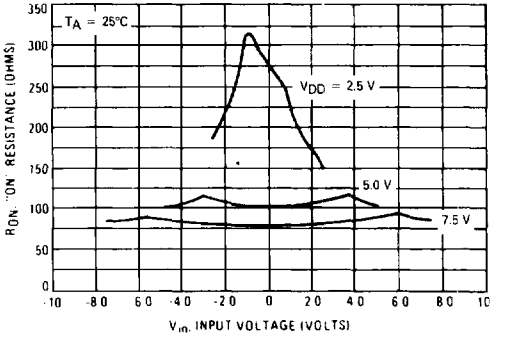


FIGURE 13 – COMPARISON at 25°C, V_{DD} @ $-V_{EE}$



6

APPLICATIONS INFORMATION

Figure A illustrates use of the on-chip level converter detailed in Figure 2. The 0-to-5 volt Digital Control signal is used to directly control a 9 V_{p-p} analog signal.

The digital control logic levels are determined by V_{DD} and V_{SS}. The V_{DD} voltage is the logic high voltage; the V_{SS} voltage is logic low. For the example, V_{DD} = +5 V = logic high at the control inputs; V_{SS} = GND = 0 V = logic low.

The maximum analog signal level is determined by V_{DD} and V_{EE}. The V_{DD} voltage determines the maximum recommended peak above V_{SS}. The V_{EE} voltage determines the maximum swing below V_{SS}. For the example, $V_{DD} - V_{SS}$ = 5 volt maximum swing above V_{SS}; $V_{SS} - V_{EE}$ = 5 volt maximum swing below V_{SS}. The example shows a ±4.5 volt signal which allows a 1/2 volt margin at each peak. If voltage transients above V_{DD} and/or below V_{EE} are anticipated on the analog channels, external diodes (D_X) are recommended as shown in Figure B. These diodes should be small signal types able to absorb the maximum anticipated current surges during clipping.

The absolute maximum potential difference between V_{DD} and V_{EE} is 18.0 volts. Most parameters are specified up to 15 volts which is the recommended maximum difference between V_{DD} and V_{EE}.

Balanced supplies are not required. However, V_{SS} must be greater than or equal to V_{EE}. For example, V_{DD} = +10 volts, V_{SS} = +5 volts, and V_{EE} = −3 volts is acceptable. See the table below.

FIGURE A — APPLICATION EXAMPLE

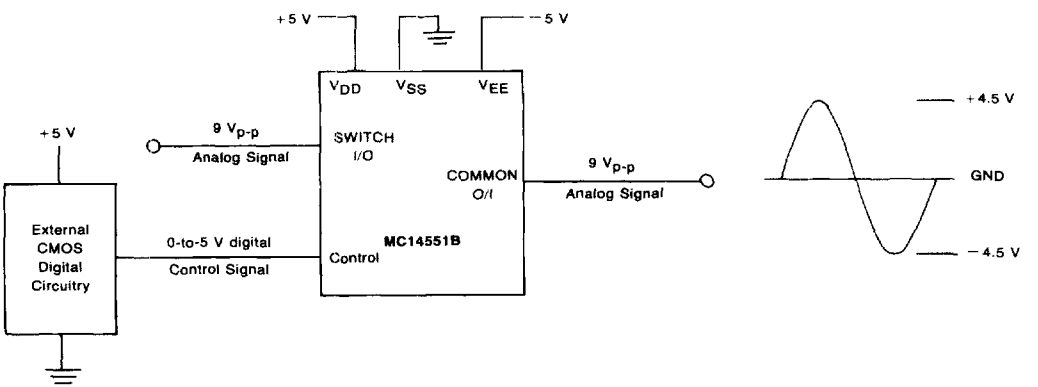
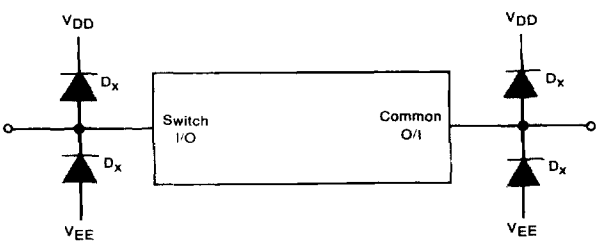


FIGURE B — EXTERNAL SCHOTTKY OR GERMANIUM CLIPPING DIODES



POSSIBLE SUPPLY CONNECTIONS

V_{DD} In Volts	V_{SS} In Volts	V_{EE} In Volts	Control Inputs Logic High/Logic Low In Volts	Maximum Analog Signal Range In Volts
+8	0	−8	+8/0	+8 to −8 = 16 V_{p-p}
+5	0	−12	+5/0	+5 to −12 = 17 V_{p-p}
+5	0	0	+5/0	+5 to 0 = 5 V_{p-p}
+5	0	−5	+5/0	+5 to −5 = 10 V_{p-p}
+10	+5	−5	+10/+5	+10 to −5 = 15 V_{p-p}