TEXAS INSTRUMENTS
Data sheet acquired from Harris Semiconductor
SCHS058A – Revised March 2002

CD4076B Types

CMOS 4-Bit D-Type Registers

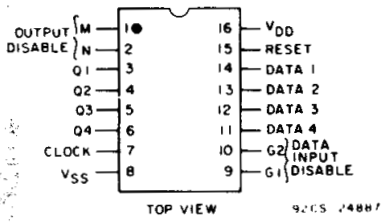
High-Voltage Types (20-Volt Rating)

■ CD4076B types are four-bit registers consisting of D-type flip-flops that feature three-state outputs. Data Disable inputs are provided to control the entry of data into the flip-flops. When both Data Disable inputs are low, data at the D inputs are loaded into their respective flip-flops on the next positive transition of the clock input. Output Disable inputs are also provided. When the Output Disable inputs are both low, the normal logic states of the four outputs are available to the load. The outputs are disabled independently of the clock by a high logic level at either Output Disable input, and present a high impedance.

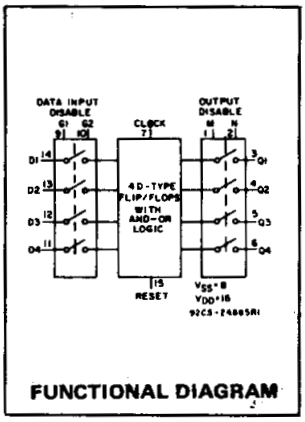
The CD4076B types are supplied in 16-lead ceramic dual-in-line packages (D and F suffixes), 16-lead dual-in-line plastic packages (E suffix), 16-lead small-outline package (NSR suffix), and in chip form (H suffix).

Features:

- Three-state outputs
- Input disabled without gating the clock
- Gated output control lines for enabling or disabling the outputs
- Standardized, symmetrical output characteristics
- 100% tested for quiescent current at 20 V
- Maximum input current of 1 μA at 18 V over full package temperature range; 100 nA at 18 V and 25°C
- Noise margin over full package temperature range:
  - 1 V at V_{DD} = 5 V
  - 2 V at V_{DD} = 10 V
  - 2.5 V at V_{DD} = 15 V
- 5-V, 10-V, and 15-V parametric ratings
- Meets all requirements of JEDEC Tentative **Standard No. 13B,** "Standard Specifications for Description of 'B' Series CMOS Devices"



TERMINAL ASSIGNMENT



FUNCTIONAL DIAGRAM

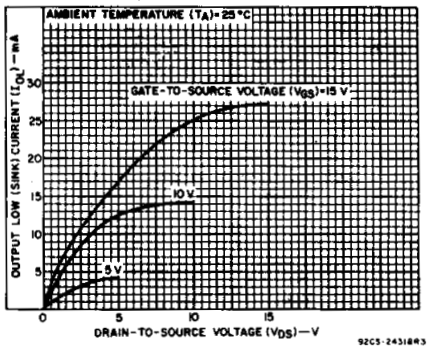


Fig. 1 — Typical output low (sink) current characteristics.

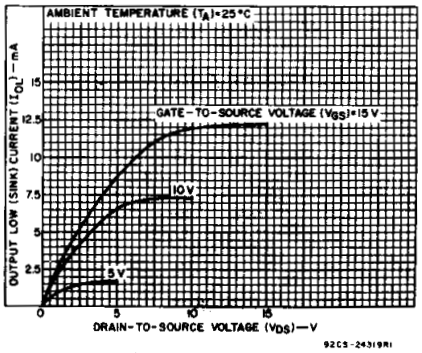


Fig. 2 — Minimum output low (sink) current characteristics.

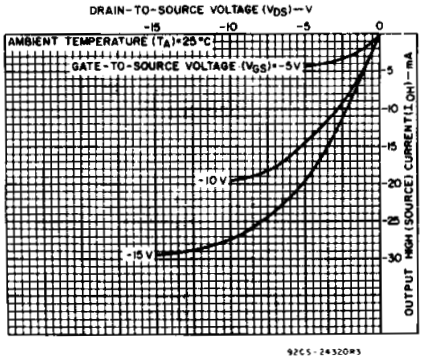


Fig. 3 — Typical output high (source) current characteristics.

RECOMMENDED OPERATING CONDITIONS at T_A = 25°C, Except as Noted.
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	V_{DD} (V)	LIMITS Min.	LIMITS Max.	UNITS
Supply-Voltage Range (For T_A = Full Package Temperature Range)		3	18	V
Data Setup Time, t_S	5	200	–	ns
	10	80	–	
	15	60	–	
Clock Pulse Width, t_W	5	200	–	ns
	10	100	–	
	15	80	–	
Clock Input Frequency, f_{CL}	5	dc	3	MHz
	10		6	
	15		8	
Clock Input Rise or Fall Time, t_rCL, t_fCL	5	–	15	μs
	10	–	5	
	15	–	5	
Reset Pulse Width, t_W	5	120	–	ns
	10	50	–	
	15	40	–	
Data Input Disable Setup Time, t_S	5	180	–	ns
	10	100	–	
	15	70	–	

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
Voltages referenced to V_{SS} Terminal) ..... -0.5V to +20V
INPUT VOLTAGE RANGE, ALL INPUTS ..... -0.5V to V_{DD} +0.5V
DC INPUT CURRENT, ANY ONE INPUT ..... ±10mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -55°C to +100°C 500mW
For T_A = +100°C to +125°C ..... Derate Linearity at 12mW/°C to 200mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) 100mW
OPERATING-TEMPERATURE RANGE (T_A) ..... -55°C to +125°C
STORAGE TEMPERATURE RANGE (T_{stg}) ..... -65°C to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm) from case for 10s max ..... +265°C

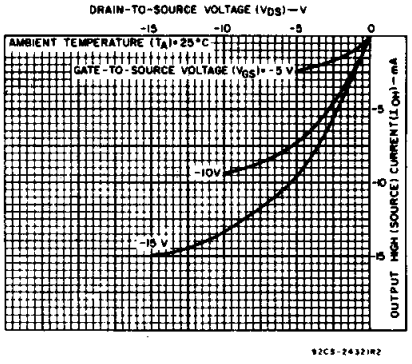
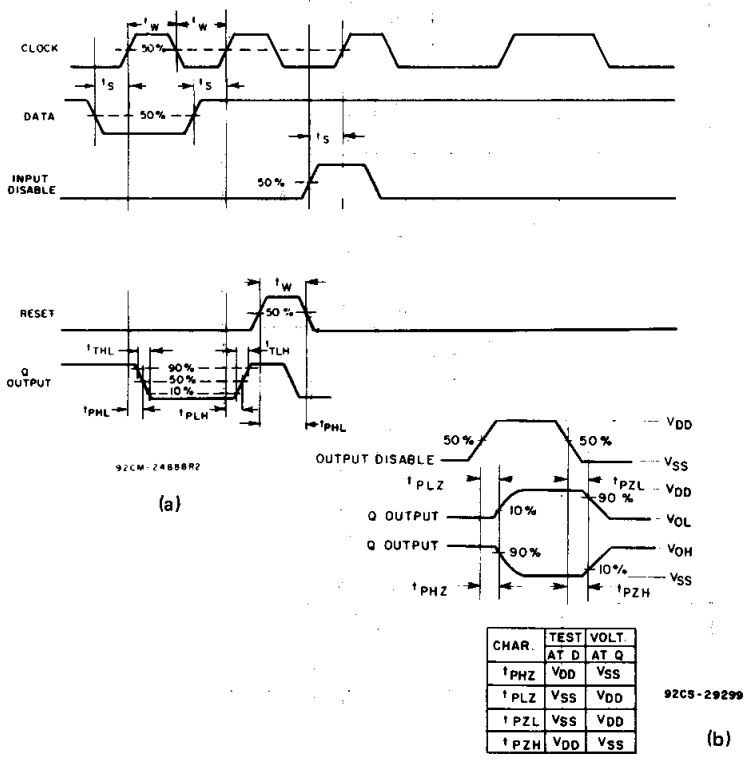


Fig.4 — Minimum output high (source) current characteristics.



CHAR.	TEST AT D	TEST AT Q
t_{PHZ}	V_{DD}	V_{SS}
t_{PLZ}	V_{SS}	V_{DD}
t_{PZL}	V_{SS}	V_{DD}
t_{PZH}	V_{DD}	V_{SS}

Fig.5 — Functional waveforms for CD4076B.

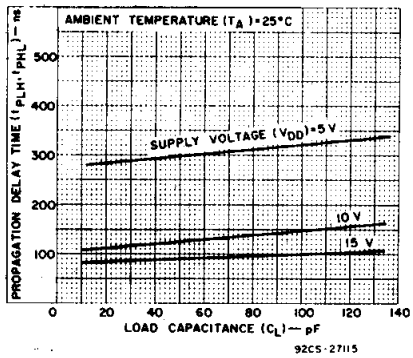


Fig.6 — Typical propagation delay time vs. load capacitance (clock to Q).

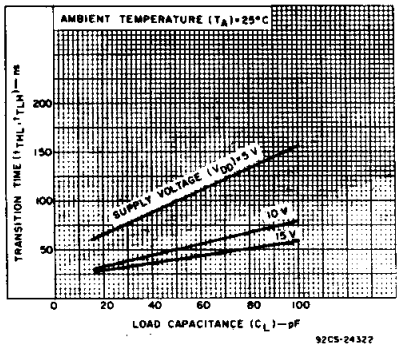


Fig.7 — Typical transition time vs. load capacitance.

Truth Table

Reset	Clock	Data Input Disable G1	Data Input Disable G2	Data D	Next State Output Q	
↑	X	X	X	X	0	
0	0	X	X	X	Q	NC
0	⌐	1	X	X	Q	NC
0	⌐	X	1	X	Q	NC
0	⌐	0	0	1	↑	
0	⌐	0	0	0	0	
0	1	X	X	X	Q	NC
0	⌐	X	X	X	Q	NC

When either Output Disable M or N is high, the outputs are disabled (high impedance state), however sequential operation of the flip flops is not affected.
1 = High Level
0 = Low Level
X = Don't Care
NC = No Change

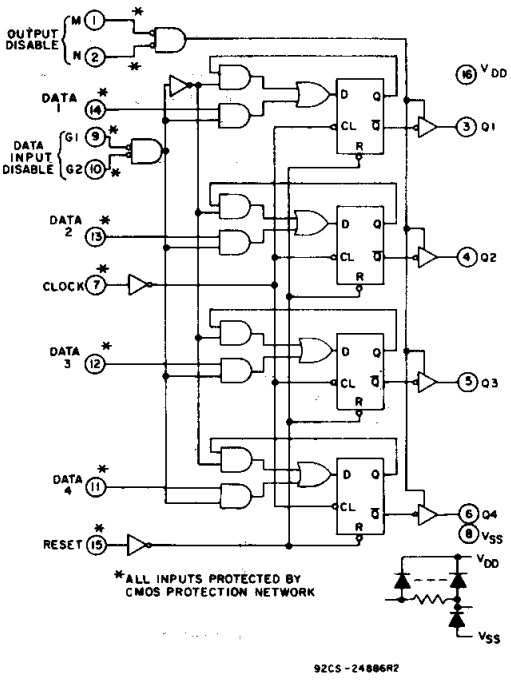


Fig.8 — CD4076B logic diagram.

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C, Input t_r,t_f = 20 ns, C_L = 50 pF, R_L = 200 kΩ (Unless otherwise noted)

CHARACTERISTIC	TEST CONDITIONS	V_{DD} V	LIMITS Min.	Typ.	Max.	UNITS
Propagation Delay Time: Clock to Q Output, t_{PHL}, t_{PLH}		5		300	600	ns
		10		125	250	
		15		90	180	
Reset, t_{PHL}		5		230	460	
		10		100	200	
		15		75	150	
3-State Output 1 or 0 to High Impedance, t_{PHZ}, t_{PLZ}	R_L = 1 kΩ	5		150	300	
		10		75	150	
		15		60	120	
3-State High Impedance to 1 or 0 Output, t_{PZH}, t_{PZL}	R_L = 1 kΩ	5		150	300	
		10		75	150	
		15		60	120	
Transition Time, t_{THL}, t_{TLH}		5		100	200	ns
		10		50	100	
		15		40	80	
Maximum Clock Input Frequency, f_{CL}		5	3	6		MHz
		10	6	12		
		15	8	16		
Minimum Clock Pulse Width, t_W		5		100	200	ns
		10		50	100	
		15		40	80	
Maximum Clock Input Rise or Fall Time, t_{rcl}, t_{fcl}		5	15	–	–	μs
		10	5	–	–	
		15	5	–	–	
Minimum Reset Pulse With, t_W		5		60	120	ns
		10		25	50	
		15		20	40	
Minimum Data Setup Time, t_S		5		100	200	ns
		10		40	80	
		15		30	60	
Minimum Data Input Disable Setup Time, t_S		5		90	180	ns
		10		50	100	
		15		35	70	
Input Capacitance, C_{IN}	Any Input	–		5	7.5	pF

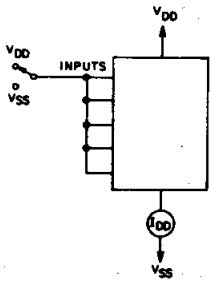


Fig.11 – Quiescent device current test circuit.

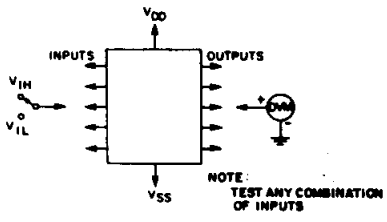


Fig.12 – Input voltage test circuit.

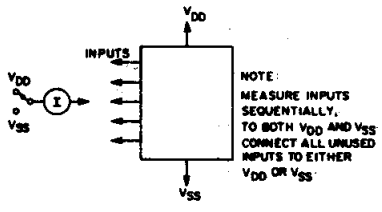


Fig. 13 – Input current test circuit.

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C)							UNITS
								+25			
	V_O (V)	V_{IN} (V)	V_{DD} (V)	−55	−40	+85	+125	Min.	Typ.	Max.	
Quiescent Device Current, I_{DD} Max.	–	0,5	5	5	5	150	150	–	0.04	5	μA
	–	0,10	10	10	10	300	300	–	0.04	10	
	–	0,15	15	20	20	600	600	–	0.04	20	
	–	0,20	20	100	100	3000	3000	–	0.08	100	
Output Low (Sink) Current I_{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	–	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	–	
	1.5	0,15	15	4.2	4	2.8	2.4	3 4	6.8	–	
Output High (Source) Current, I_{OH} Min.	4.6	0,5	5	−0.64	−0.61	−0.42	−0.36	−0.51	−1	–	
	2.5	0,5	5	−2	−1.8	−1.3	−1.15	−1.6	−3.2	–	
	9.5	0,10	10	−1.6	−1.5	−1.1	−0.9	−1.3	−2.6	–	
	13.5	0,15	15	−4.2	−4	−2.8	−2.4	−3.4	−6.8	–	
Output Voltage: Low-Level, V_{OL} Max.	–	0,5	5	0.05				–	0	0.05	V
	–	0,10	10	0.05				–	0	0.05	
	–	0,15	15	0.05				–	0	0.05	
Output Voltage: High-Level, V_{OH} Min.	–	0,5	5	4.95				4.95	5	–	
	–	0,10	10	9.95				9.95	10	–	
	–	0,15	15	14.95				14.95	15	–	
Input Low Voltage, V_{IL} Max.	0.5, 4.5	–	5	1.5				—	—	1.5	V
	1, 9	–	10	3				—	—	3	
	1.5,13.5	–	15	4				–	—	4	
Input High Voltage, V_{IH} Min.	0.5, 4.5	–	5	3.5				3.5	—	—	
	1, 9	–	10	7				7	—	—	
	1.5,13.5	–	15	11				11	—	—	
Input Current I_{IN} Max.	–	0,18	18	±0.1	±0.1	±1	±1	–	$\pm 10^{-5}$	±0.1	μA
3-State Output Leakage Current I_{OUT} Max.	0,18	0,18	18	±0.4	±0.4	±12	±12	–	$\pm 10^{-4}$	±0.4	μA

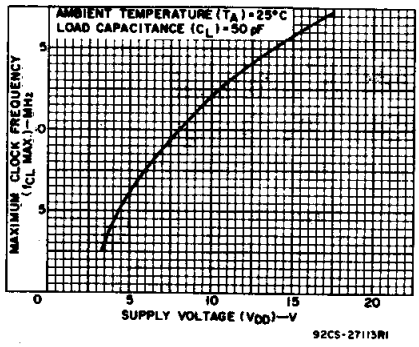


Fig.9 – Typical maximum clock input frequency vs. supply voltage.

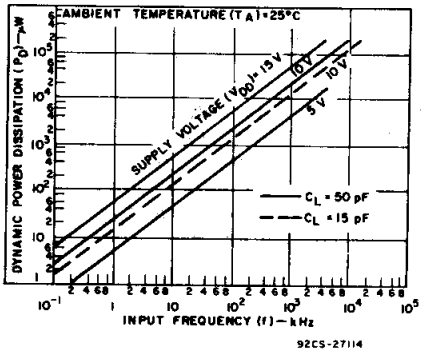
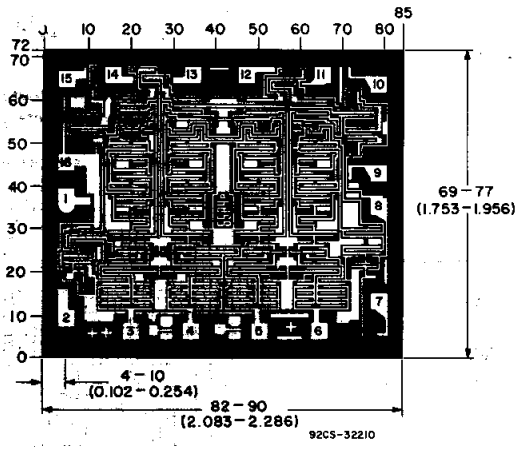


Fig.10 – Typical dynamic power dissipation vs. frequency.



Dimensions and pad layout for CD4076BH

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third–party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Mailing Address:

Texas Instruments
Post Office Box 655303
Dallas, Texas 75265

CD4076B, CMOS 4-Bit D-Type Registers

DEVICE STATUS: **ACTIVE**

PARAMETER NAME	CD4076B
Voltage Nodes (V)	5, 10, 15

FEATURES

Back to Top

- Three-state outputs
- Input disabled without gating the clock
- Gated output control lines for enabling or disabling the outputs
- Standardized, symmetrical output characteristics
- 100% tested for quiescent current at 20 V
- Maximum input current of 1 uA at 18 V over full package temperature range; 100 nA at 18 V and 25°C
- Noise margin over full package temperature range:
  - 1 V at V_{DD} = 5 V
  - 2 V at V_{DD} = 10 V
  - 2.5 V at V_{DD} = 15 V
- 5-V, 10-V, and 15-V parametric ratings
- Meets all requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"

DESCRIPTION

Back to Top

CD4076B types are four-bit registers consisting of D-type flip-flops that feature three-state outputs. Data Disable inputs are provided to control the entry of data into the flip-flops. When both Data Disable inputs are low, data at the D inputs are loaded into their respective flip-flops on the next positive transition of the clock input. Output Disable inputs are also provided. When the Output Disable inputs are both low, the normal logic states of the four outputs are available ot the load. The outputs are disabled independently of the clock by a high logic level at either Output Disable input, and present a high impedance.

The CD4076B types are supplied in 16-lead ceramic dual-in-line packages (D and F suffixes), 16-lead dual-in-line plastic packages (E suffix), 16-lead small-outline package (NSR suffix), and in chip form (H suffix).

TECHNICAL RESOURCES

Back to Top

To view the following documents, Acrobat Reader 4.0 is required.

To download a document to your hard drive, right-click on the link and choose 'Save'.

DATASHEET

Back to Top

Full datasheet in Acrobat PDF: cd4076b.pdf (209 KB,Rev.A) (Updated: 03/15/2002)

APPLICATION NOTES

Back to Top

View Application Reports for Digital Logic

- Evaluation of Nickel/Palladium/Gold-Finished Surface-Mount Integrated Circuits (SZZA026 - Updated: 06/20/2001)

Product Folder: CD4076B, CMOS 4-Bit D-Type Registers

RELATED DOCUMENTS

Back to Top

- Advanced Bus Interface Logic Selection Guide (SCYT126, 448 KB - Updated: 01/09/2001)
- Documentation Rules (SAP) And Ordering Information (Rev. B) (SZZU001B, 13 KB - Updated: 05/06/1999)
- Logic Selection Guide First Half 2002 (Rev. Q) (SDYU001Q, 3368 KB - Updated: 12/17/2001)
- MicroStar Junior BGA Design Summary (SCET004, 167 KB - Updated: 07/28/2000)
- More Power In Less Space - Technical Article (Rev. A) (SCAU001A, 850 KB - Updated: 03/01/1996)
- Overview of IEEE Std 91-1984, Explanation of Logic Symbols Training Booklet (Rev. A) (SDYZ001A, 138 KB - Updated: 07/01/1996)

PRICING/AVAILABILITY/PKG

Back to Top

ORDERABLE DEVICE	PACKAGE	PINS	TEMP (°C)	STATUS	BUDGETARY PRICE US$/UNIT QTY=1000+	PACK QTY	DSCC NUMBER	PRICING/AVAILABILITY/PKG
CD4076BE	N	16	-55 TO 125	ACTIVE	0.42	25		Check stock or order
CD4076BF	J	16	-55 TO 125	ACTIVE	2.75	1		Check stock or order
CD4076BF3A	J	16	-55 TO 125	ACTIVE	3.23	1		Check stock or order
CD4076BNSR	NS	16	-55 TO 125	ACTIVE	0.56	2000		Check stock or order
CD4076BPW	PW	16	-55 TO 125	OBSOLETE				
CD4076BPWR	PW	16	-55 TO 125	ACTIVE	0.42	2000		Check stock or order

Table Data Updated on: 4/28/2002