

CMOS STROBED HEX INVERTER/BUFFER

FEATURES

- ◆ 3-State Outputs with Separate Disable Control
- ◆ Common Input Inhibit Line
- ◆ TTL Output Drive Guaranteed Over Temperature Range
- ◆ Output Impedance $< 200 \Omega$ @ 5Vdc Guaranteed Over Temperature Range

DESCRIPTION

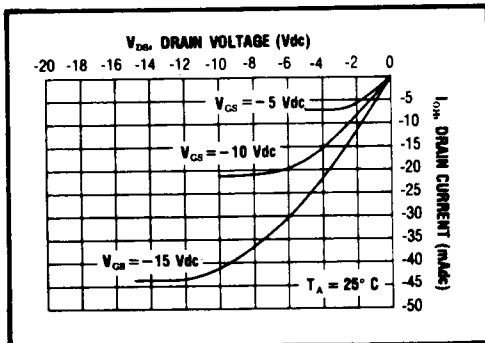
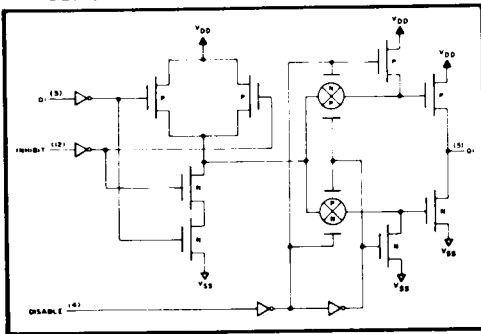
The 4502B is a Strobed Hex Inverter/Buffer with a common Data Input Inhibit Control and a common Output Disable Control. The 3-state output allows common bus configurations.

TRUTH TABLE

D_n	Inhibit	Disable	Q_n
0	0	0	1
1	0	0	0
X	1	0	0
X	X	1	High Impedance

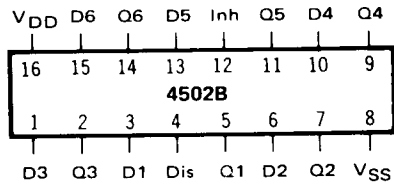
X = Don't Care

SCHEMATIC DIAGRAM (1 of 6 buffers)



Typical P-Channel Source Current Characteristics

CONNECTION DIAGRAM (all packages)



Add suffix for package:

- C 16-pin Cerdip F 16-pin Flat
- D 16-pin Ceramic H Chip
- E 16-pin Epoxy

RECOMMENDED OPERATING CONDITIONS

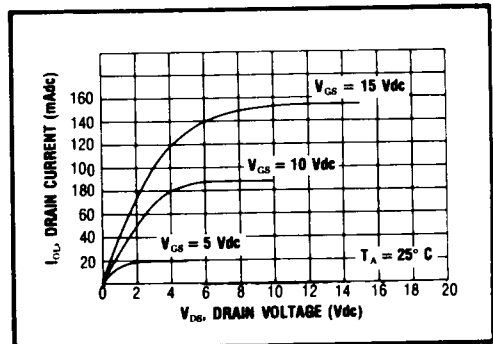
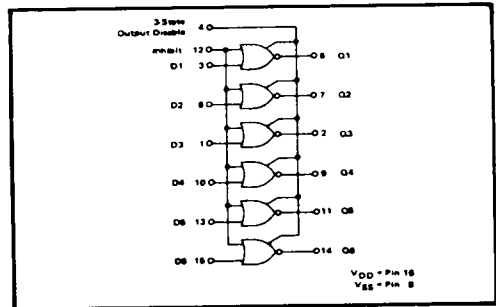
For maximum reliability:

DC Supply Voltage $V_{DD} - V_{SS}$ 3 to 15 Vdc

Operating Temperature T_A

- C, D, F, H Device -55 to +125 °C
- E Device -40 to +85 °C

LOGIC DIAGRAM



Typical N-Channel Sink Current Characteristics

ELECTRICAL CHARACTERISTICS

STATIC CHARACTERISTICS¹

PARAMETER	V _{DD} (Vdc)	CONDITIONS	T _{LOW} ²		+25°C			T _{HIGH} ²		Units
			Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
QUIESCENT DEVICE CURRENT	I _{DD}	V _{IN} = V _{SS} or V _{DD} All valid input combinations	—	1.0	—	0.005	1.0	—	30	μAdc
			—	2.0	—	0.01	2.0	—	60	
			—	4.0	—	0.02	4.0	—	120	
OUTPUT LOW (SINK) CURRENT	I _{OL}	V _{OL} = 0.4V V _{OL} = 0.5V V _{OL} = 1.5V V _{IN} = V _{SS} or V _{DD}	3.5	—	2.8	5.7	—	2.0	—	mAdc
			7.8	—	6.3	12.5	—	4.4	—	
			29	—	24.0	49	—	16	—	
3-STATE OUTPUT LEAKAGE CURRENT	I _{ZL}		—	±0.1	—	±10 ⁻⁴	±0.1	—	±1.0	μAdc

NOTES: ¹ Remaining Static Electrical Characteristics are listed under "4000B Series Family Specifications".

² T_{LOW} = -55°C for C, D, F, H device.

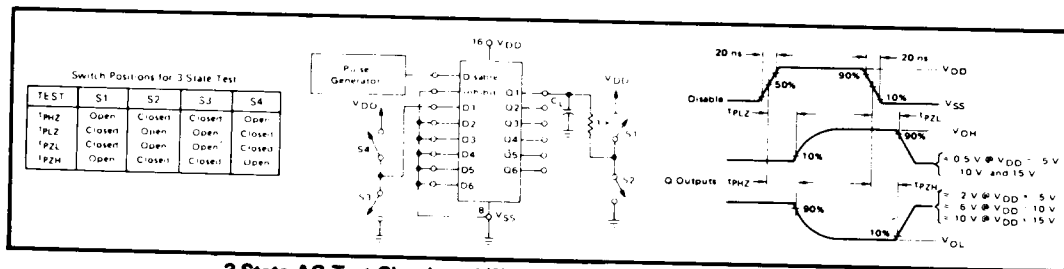
= -40°C for E device.

T_{HIGH} = +125°C for C, D, F, H device.

= + 85°C for E device.

DYNAMIC CHARACTERISTICS (C_L = 50pF, T_A = 25°C)

PARAMETER	V _{DD} (Vdc)	Min.	Typ.	Max.	Units		
PROPAGATION DELAY TIME From Data Inputs	t _{PLH}	5	—	125	250	ns	
		10	—	60	120		
		15	—	45	90		
	From Disable	t _{PHL}	5	—	100	200	ns
			10	—	50	100	
			15	—	40	80	
From Disable	t _{PHZ} , t _{PLZ} t _{PZH} , t _{PZL}	5	—	65	130	ns	
		10	—	30	60		
		15	—	25	50		
OUTPUT TRANSITION TIME	t _{TLH}	5	—	100	200	ns	
		10	—	50	100		
		15	—	40	80		
	t _{THL}	5	—	60	120	ns	
		10	—	30	60		
		15	—	20	40		



3-State AC Test Circuit and Waveforms (t_{PHZ}, t_{PZH}, t_{PLZ}, t_{PZL})