AS-5040/AS-5051 Family High Level CMOS Analog Gates

FEATURES

- Switches Greater Than 20Vpp Signals With ±15V Supplies
- Quiescent Current Less Than 1μA
- Overvoltage Protection to ±25V
- Break-Before-Make Switching t_{OFF} 200nsec, t_{ON} 300nsec Typical
- T²L, DTL, CMOS, PMOS Compatible
- Non-Latching With Supply Turn-Off
- Low r_{DS} (ON) – 35Ω
- New DPDT & 4PST Configurations
- Complete Monolithic Construction AS-5040 through AS-5047

CMOS ANALOG GATE PRODUCT CONDITIONING

The following processes are performed 100% in accordance with MIL-STD-883.

Precap Visual – Method 2010, Cond. B.
Stabilization Bake – Method 1008
Temperature Cycle – Method 1010
Centrifuge – Method 2001, Cond. E
Hermeticity – Method 1014, Cond. A, C.
(Leak Rate $< 5 \times 10^{-7}$ atm cc/s)

GENERAL DESCRIPTION

The AS-5040 family of solid state analog gates are designed using an improved, high voltage CMOS monolithic technology. These devices provide ease-of-use and performance advantages not previously available from solid state switches. This improved CMOS technology provides input overvoltage capability to ±25 volts without damage to the device, and destructive latch-up of solid state analog gates has been eliminated. Early CMOS gates were destroyed when power supplies were removed with an input signal present. The AS-5040 CMOS technology has eliminated this serious systems problem.

Key performance advantages of the 5040 series are TTL compatibility and ultra low-power operation. The quiescent current requirement is less than 1μA. Also designed into the 5040 is guaranteed Break-Before-Make switching, which is accomplished by extending the t_{ON} time (300 nsec TYP.) so that it exceeds t_{OFF} time (200 nsec TYP.). This insures that an ON channel will be turned OFF before an OFF channel can turn ON. This eliminates the need for external logic required to avoid channel to channel shorting during switching.

Many of the 5040 series improve upon and are pin-for-pin and electrical replacements for other solid state switches.

FUNCTIONAL DIAGRAM

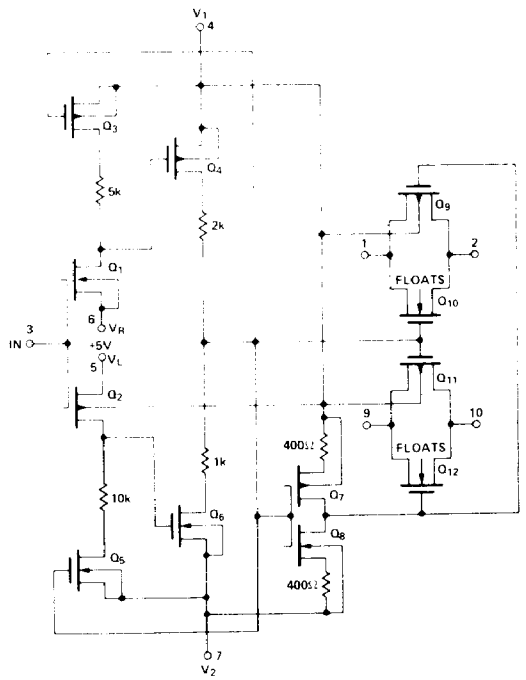


FIGURE 1. TYPICAL DRIVER, GATE – AS-5042

FUNCTIONAL DESCRIPTION

PART NO.	TYPE		R_{ON}	FUNCTIONAL EQUIVALENT
AS-5040		SPST	75Ω	
AS-5041	Dual	SPST	75Ω	
AS-5042		SPDT	75Ω	DG 188AA/BA
AS-5043	Dual	SPDT	75Ω	DG 191AP/BP
AS-5044		DPST	75Ω	
AS-5045	Dual	DPST	75Ω	DG 185AP/BP
AS-5046		DPDT	75Ω	
AS-5047		4PST	75Ω	
AS-5048 (hybrid)	Dual	SPST	35Ω	
AS-5049 (hybrid)	Dual	DPST	35Ω	DG 184AP/BP
AS-5050 (hybrid)		SPDT	35Ω	DG 187AA/BA
AS-5051 (hybrid)	Dual	SPDT	35Ω	DG 190AP/BP

MAXIMUM RATINGS

Current (Any Terminal)	< 30mA
Storage Temperature	−65°C to +150°C
Operating Temperature	−55°C to +125°C
Power Dissipation	450mW
(All Leads Soldered to a P. C. Board)	
Derate 6mW/°C Above 70°C	
Lead Temperature (Soldering, 10 sec)	300°C

$V_1 - V_2$	< 33V
$V_1 - V_D$	< 30V
$V_D - V_2$	< 30V
$V_D - V_S$	< +22V
$V_L - V_2$	< 33V
$V_L - V_{IN}$	< 30V
$V_L - V_R$	< 20V
$V_{IN} - V_R$	< 20V

ELECTRICAL CHARACTERISTICS (@ 25°C, V_1 = +15 V, V_2 = −15 V, V_L = +5 V, V_R = 0 V)

PER CHANNEL		MIN./MAX. LIMITS							
		MILITARY			COMMERCIAL				
SYMBOL	CHARACTERISTIC	-55 C	+25 C	+125 C	0	+25 C	+70 C	UNITS	TEST CONDITIONS
$I_{IN(ON)}$	Input Logic Current	1	1	1	1	1	1	µA	V_{in} = 2.4 V Note 1
$I_{IN(OFF)}$	Input Logic Current	1	1	1	1	1	1	µA	V_{in} = 0.8 V Note 1
$r_{DS(ON)}$	Drain Source On Resistance	75(35)	75(35)	150(60)	80(45)	80(45)	130(45)	Ω	(5048 Thru 5051) I_S = 1mA V_{ANALOG} = −10 V to +10 V
$\Delta r_{DS(ON)}$	Channel to Channel $R_{DS(ON)}$ Match	25(15)	25(15)	25(15)	30(15)	30(15)	30(15)	Ω	(5048 thru 5051) I_S (Each Channel) = 1 mA
V_{ANALOG}	Min. Analog Signal Handling Capability	+11(+10)	+11(+10)	+11(+10)	+10(+10)	+10(+10)	+10(+10)	V	I_S = 10 mA (5048 thru 5051)
$I_{D(OFF)}$	Switch OFF Leakage Current	1(1)	1(1)	100(100)	5(5)	5(5)	100(100)	nA	V_{ANALOG} = −10 V to +10 V (5048 thru 5051)
$I_{D(ON)}$ + $I_{S(ON)}$	Switch On Leakage Current	2(2)	2(2)	200(200)	10(10)	10(10)	100(200)	nA	V_D = V_S = −10 V to +10 V (5048 thru 5051)
t_{ON}	Switch "ON" Time		500(250)			500(300)		ns	R_L = 1 kΩ, V_{ANALOG} = −10V to +10 V See Fig. A
t_{OFF}	Switch "OFF" Time		250(150)			250(150)		ns	R_L = 1 kΩ, V_{ANALOG} = −10 V to +10 V See Fig. A (5048 thru 5051)
$Q_{(INJ)}$	Charge Injection		15 (10)			20 (10)		mV	See Fig. B (5048 thru 5051)
OIRR	Min. Off Isolation Rejection Ratio		54			50		dB	f = 1 MHz, R_L = 100Ω, C_L = 5 pF See Fig. C
I_{V1}	+ Power Supply Quiescent Current	1	1	10	10	10	100	µA	
I_{V2}	− Power Supply Quiescent Current	1	1	10	10	10	100	µA	V_1 = +15 V, V_2 = −15 V, V_L = +5 V
I_{VL}	+5 V Supply Quiescent Current	1	1	10	10	10	100	µA	V_L = +5 V, V_{in} = 0 Switch Duty Cycle = 10%
I_{VR}	Gnd Supply Quiescent Current	1	1	10	10	10	100	µA	
CCRR	Min. Channel to Channel Cross Coupling Rejection Ratio		54			50		dB	One Channel Off, Any Other Channel Switches as per Fig. E

TEST CIRCUITS

FIG. A

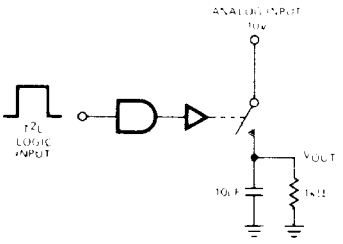


FIG. B

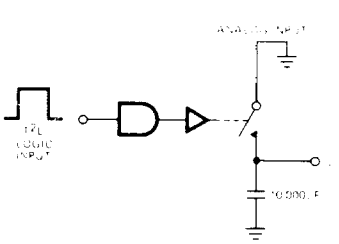
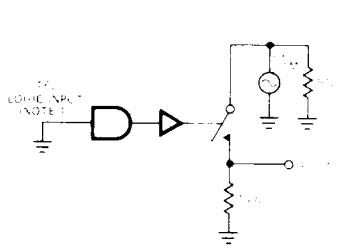


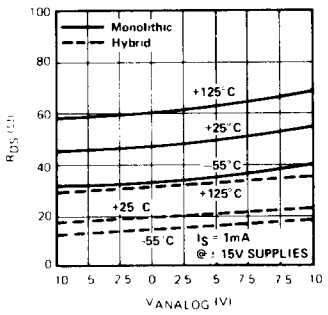
FIG. C



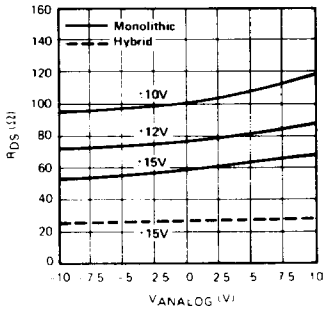
NOTE 1: Some channels are turned on by high "1" logic inputs and other channels are turned on by low "0" inputs; however 0.8V to 2.4V describes the min. range for switching properly. Refer to logic diagrams to see absolute value of logic input required to produce "ON" or "OFF" state.

TYPICAL ELECTRICAL CHARACTERISTICS (Per Channel)

R_{DS} (ON) vs V_{ANALOG} SIGNAL



R_{DS} (ON) vs POWER SUPPLY VOLTAGE



CHARGE INJECTION vs V_{ANALOG} (SEE FIG. B) C_L = 10,000pF

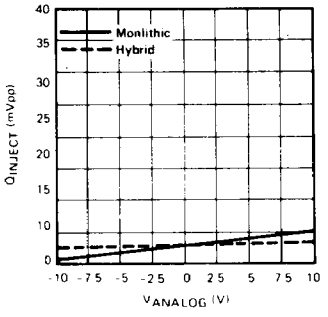
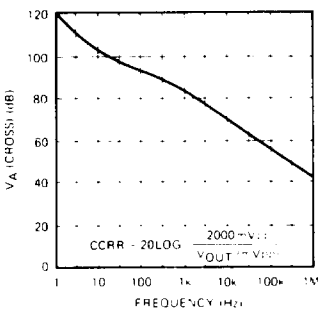


FIGURE D

CROSS COUPLING REJECTION vs FREQUENCY



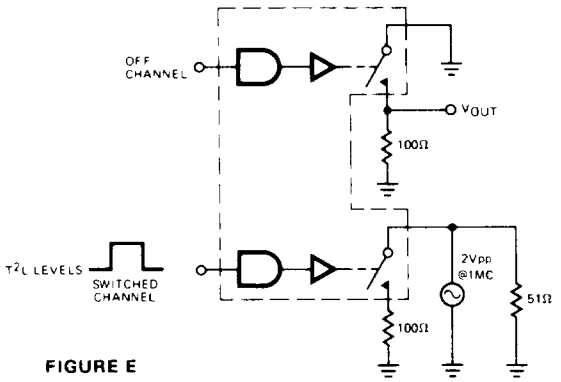
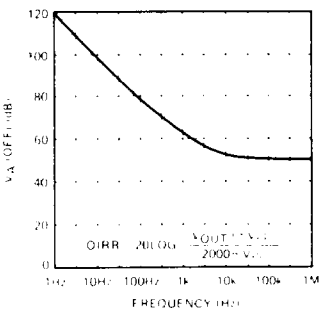


FIGURE E

OFF ISOLATION vs FREQUENCY



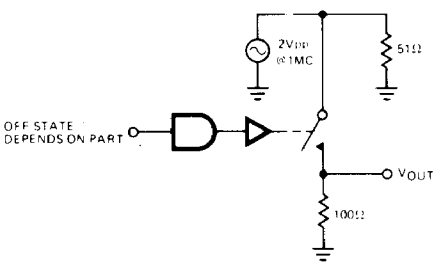
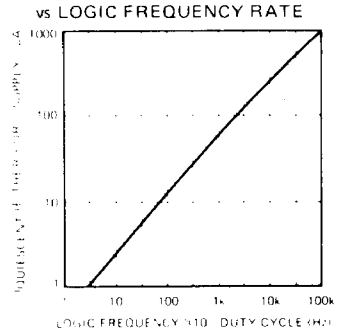


FIGURE F

POWER SUPPLY QUIESCENT CURRENT vs LOGIC FREQUENCY RATE



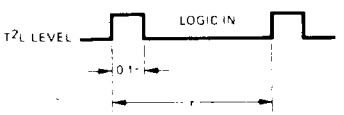


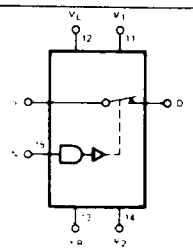
FIGURE G

SWITCHING STATE DIAGRAMS

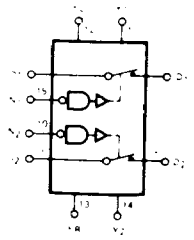
SWITCH STATES
ARE FOR LOGIC "1" INPUT

DIP PACKAGE

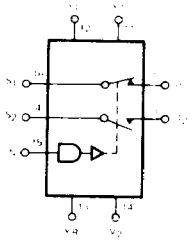
SPST
5040 (r_{DS} (ON) <75Ω)



DUAL SPST
5041 (r_{DS} (ON) <75Ω)

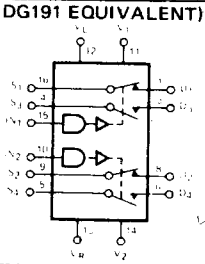


SPDT
5042 (r_{DS} (ON) <75Ω)

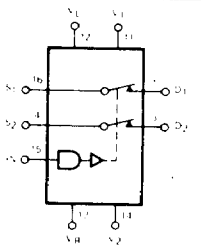


(DG191 EQUIVALENT)

DUAL SPDT
5043 (r_{DS}(ON) <75Ω)

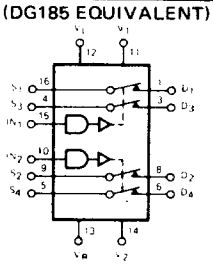


DPST
5044 (r_{DS} (ON) <75Ω)



(DG185 EQUIVALENT)

DUAL DPST
5045 (r_{DS} (ON) <75Ω)

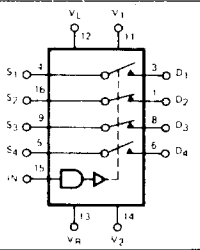


SWITCHING STATE DIAGRAMS (Cont.)

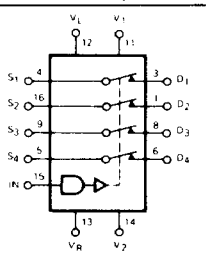
SWITCH STATES
ARE FOR LOGIC "1" INPUT

DIP PACKAGE

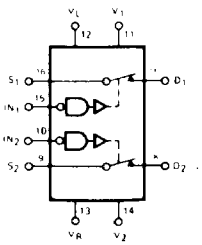
DPDT
5046 (r_{DS} (ON) <75Ω)



4PST
5047 (r_{DS} (ON) <75Ω)

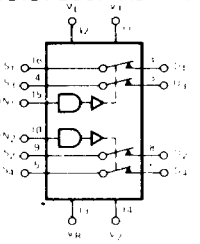


DUAL SPST
5048 (r_{DS} (ON) <35Ω)

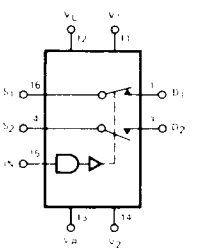


(DG184 EQUIVALENT)

DUAL DPST
5049 (r_{DS} (ON) <35Ω)

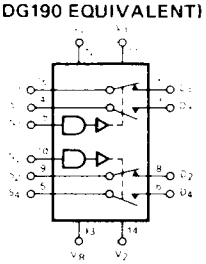


SPDT
5050 (r_{DS} (ON) <35Ω)



(DG190 EQUIVALENT)

DUAL SPDT
5051 (r_{DS} (ON) <35Ω)



APPLICATIONS

IMPROVED SAMPLE & HOLD
USING AS-5043

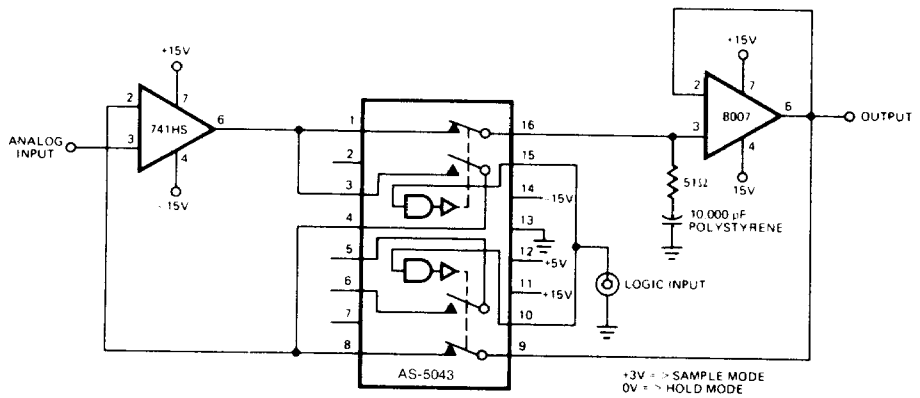


FIGURE H

USING THE CMOS SWITCH TO DRIVE
AN R/2R LADDER NETWORK (2 LEGS)

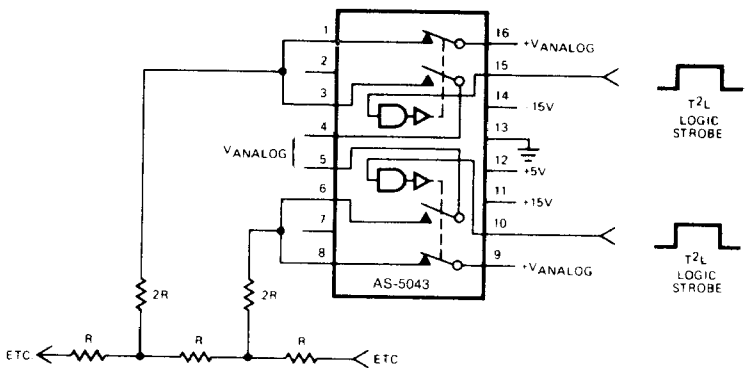


FIGURE I

EXAMPLE: If $-V_{ANALOG} = -10VDC$ and $+V_{ANALOG} = +10VDC$ then Ladder Legs are switched between ±10VDC, depending upon state of Logic Strobe.

THEORY OF OPERATION

A. FLOATING BODY CMOS STRUCTURE

In a conventional C-MOS structure, the body of the "n" channel device is tied to the negative supply, thus forming a reverse biased diode between the drain/source and the body (Fig. J). Under certain conditions this diode can become forward biased; for example, if the supplies are off (at ground) and a negative input is applied to the drain. This can have serious consequences for two reasons. Firstly, the diode has no current limiting and if excessive current flows, the circuit may be permanently damaged. Secondly, this diode forms part of a parasitic SCR in the conventional C-MOS structure. Forward biasing the diode causes the SCR to turn on, giving rise to a "latch-up" condition.

The new improved C-MOS process incorporates an additional diode in series with the body (Fig. K). The cathode of this diode is then tied to V+, thus effectively floating the body. The inclusion of this diode not only blocks the excessive current path, but also prevents the SCR from turning on.

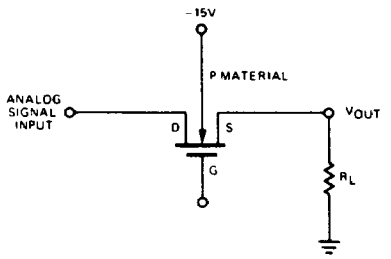


FIGURE J

B. OVERVOLTAGE PROTECTION

The floating body construction inherently provides overvoltage protection. In the conventional C-MOS process, the body of all N-channel FETs is tied to the most negative power supply and the body of all P-channel devices to the most positive supply (i. e., ±15V). Thus, for an overvoltage spike of > ±15V, a forward bias condition exists between drain and body of the MOSFET. For example, in Fig. J if the analog signal input is more negative than −15V, the drain to body of the N-channel FET is forward biased and destruction of the device can result. Now by floating the body, using diode D1, the drain to body of the MOSFET is still forward biased, but D1 is reversed biased so no current flows (up to the breakdown of D1 which is ≥ 40V). Thus, negative excursions of the analog signal can go up to a maximum of -25V. When the signal goes positive (≥ +15V, D1 is forward biased, but now the drain to body junction is reversed for the N-channel FET; this allows the signal to go to a maximum of +25V with no appreciable current flow. While the explanation above has been restricted to N-channel devices, the same applies to P-channel FETs and the construction is as shown in Fig. L. Fig. L describes an output stage showing the paralleling of an N and P channel to linearize the $r_{DS(ON)}$ with signal input. The presence of diodes D1 and D2 effectively floats the bodies and provides over voltage protection to a maximum of ±25V.

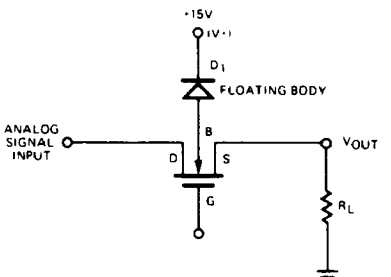


FIGURE K

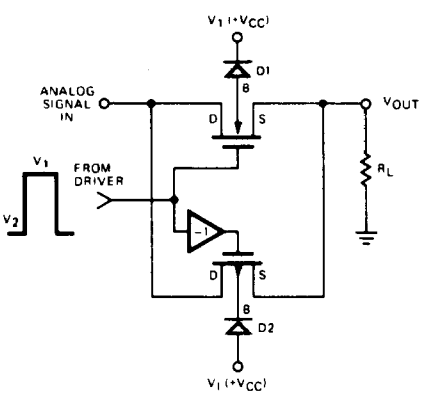
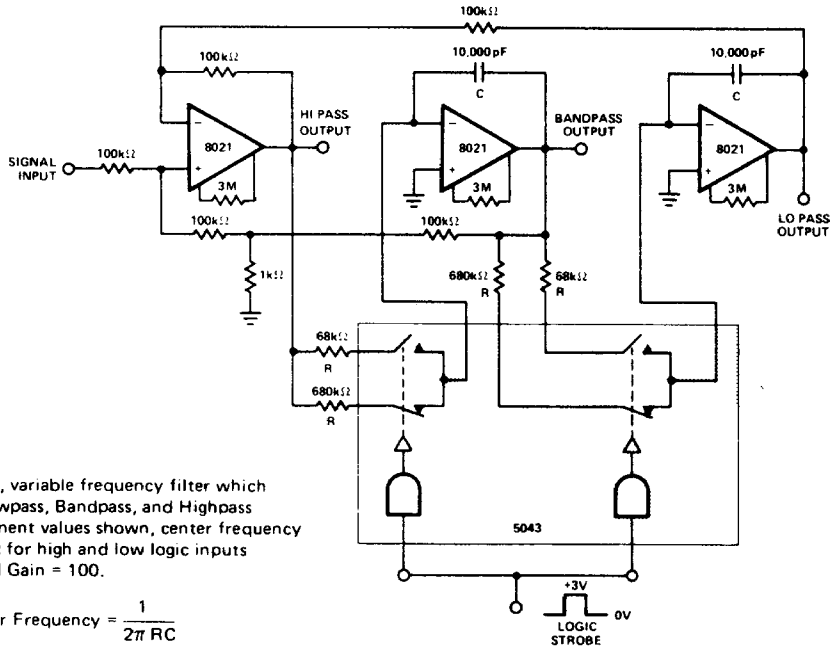


FIGURE L

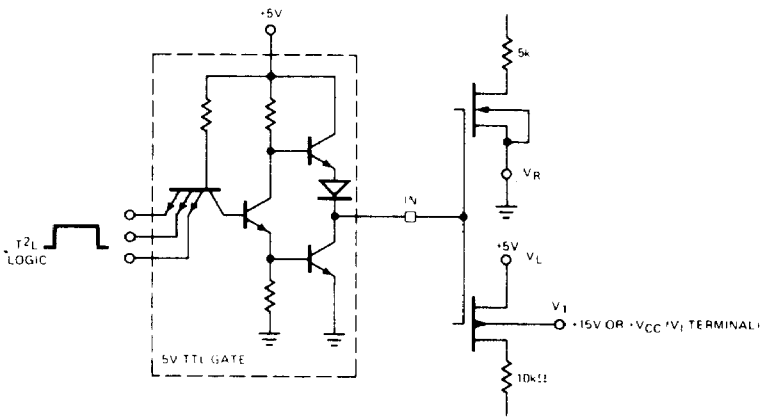
DIGITALLY TUNED
LOW POWER ACTIVE FILTER



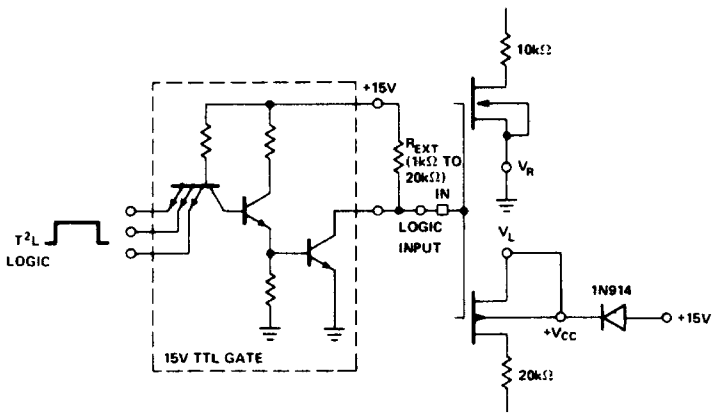
Constant gain, constant Q, variable frequency filter which provides simultaneous Lowpass, Bandpass, and Highpass outputs. With the component values shown, center frequency will be 235Hz and 23.5Hz for high and low logic inputs respectively, Q = 100, and Gain = 100.

$$f_n = \text{Center Frequency} = \frac{1}{2\pi RC}$$

LOGIC INTERFACING

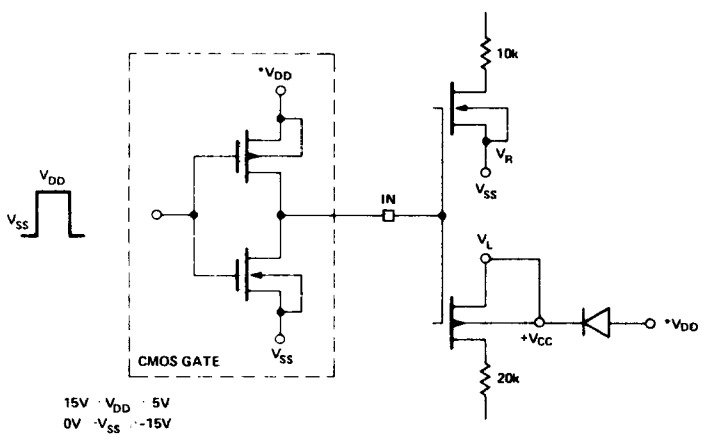


FOR INTERFACING WITH T^2L OPEN COLLECTOR LOGIC.



TYP. EXAMPLE FOR +15V CASE SHOWN

FOR USE WITH CMOS LOGIC.



15V ≤ V_{DD} ≤ 5V
0V ≤ V_{SS} ≤ -15V

ORDERING INFORMATION

MODEL	SWITCH CONFIGURATION	OPER. TEMP RANGE	PACKAGE
AS-5040C	SPST	0 to +70° C	16 pin Epoxy
AS-5040M		−55 to +125° C	16 pin Cerdip
AS-5041C	Dual SPST	0 to +70° C	16 pin Epoxy
AS-5041M		−55 to +125° C	16 pin Cerdip
AS-5042C	SPDT	0 to +70° C	16 pin Epoxy
AS-5042M		−55 to + 125 °C	16 pin Cerdip
AS-5043C	Dual SPDT	0 to +70° C	16 pin Epoxy
AS-5043M		−55 to +125° C	16 pin Cerdip
AS-5044C	DPST	0 to +70° C	16 pin Epoxy
AS-5044M		−55 to +125° C	16 pin Cerdip
AS-5045C	Dual DPST	0 to +70° C	16 pin Epoxy
AS-5045M		−55 to +125° C	16 pin Cerdip
AS-5046C	DPDT	0 to +70° C	16 pin Epoxy
AS-5046M		−55 to +125° C	16 pin Cerdip
AS-5047C	4PST	0 to +70° C	16 pin Epoxy
AS-5047M		−55 to +125° C	16 pin Cerdip
AS-5048C	Dual SPST	0 to +70° C	16 pin Epoxy
AS-5048M		−55 to +125° C	16 pin Cerdip
AS-5049C	Dual DPST	0 to +70° C	16 pin Epoxy
AS-5049M		−55 to +125° C	16 pin Cerdip
AS-5050C	SPDT	0 to +70° C	16 pin Epoxy
AS-5050M		−55 to +125° C	16 pin Cerdip
AS-5051C	Dual SPDT	0 to +70° C	16 pin Epoxy
AS-5051M		−55 to +125° C	16 pin Cerdip