TOSHIBA

TC74HC259AP/AF/AFN

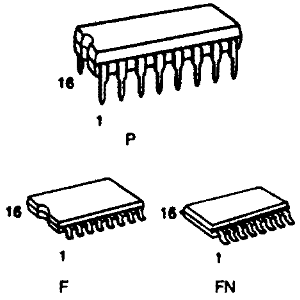
8-Bit Addressable Latch

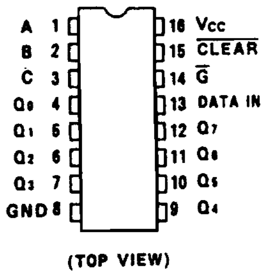
The TC74HC259A is high speed CMOS MULTIPLEXERs fabricated with silicon gate C^2MOS technology.

It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

The respective bits are controlled by address inputs A, B, and C. When $\overline{CLEAR}$ input is held high and enable input $\overline{G}$ is held low, the data is written into the bit selected by address inputs, the other bit hold their previous conditions. When both $\overline{CLEAR}$ and $\overline{G}$ held high, writing of all bits is inhibited regardless of address inputs, and their previous conditions are held. When $\overline{CLEAR}$ is held low and $\overline{G}$ is held high, all bits are reset to low regardless of the other inputs. When both of $\overline{CLEAR}$ and $\overline{G}$ held low, all bits which isn't selected by address inputs are reset to low.

All inputs are equipped with protection circuits against static discharge or transient excess voltage.

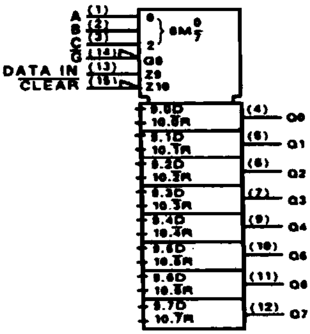




Pin Assignment

Features

- High Speed: t_{pd} = 15ns(typ.) at V_{CC} = 5V
- Low Power Dissipation: I_{CC} = 4μA(Max.) at Ta = 25°C
- High Noise Immunity: $V_{NIH} = V_{NIL}$ = 28% V_{CC} (Min)
- Output Drive Capability: 10 LSTTL Loads
- Symmetrical Output Impedance: $|I_{OH}| = I_{OL}$ = 4mA(Min.)
- Balanced Propagation Delays: $t_{pLH} = t_{pHL}$
- Wide Operating Voltage Range: $V_{CC}(opr)$ = 2V ~ 6V
- Pin and Function Compatible with 74LS259



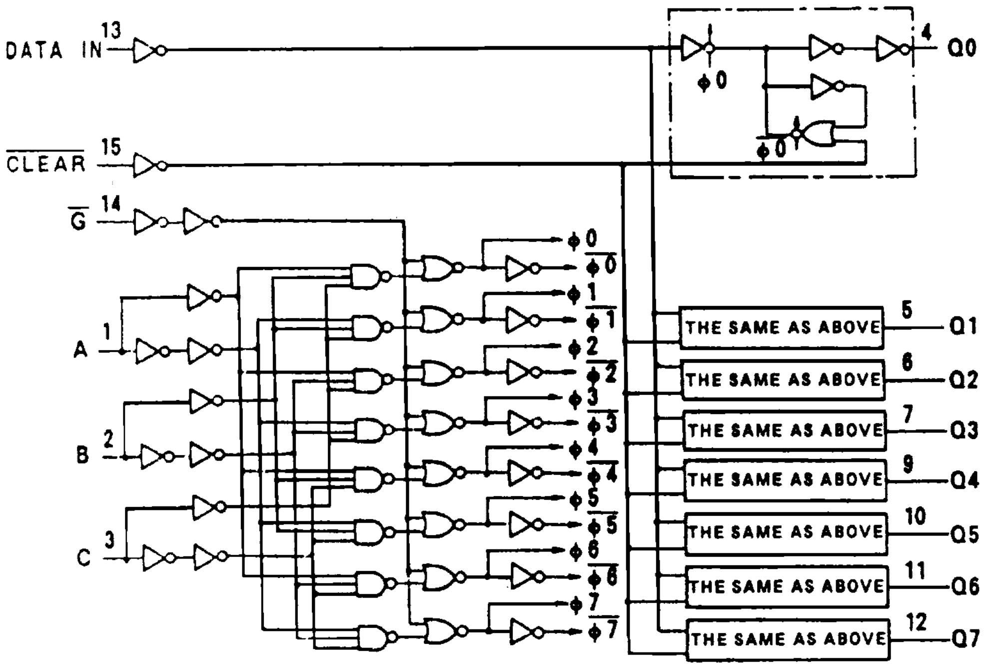
IEC Logic Symbol

Truth Table

Inputs		Output of Addressed Latch	Each Other Output	Function
$\overline{CLEAR}$	G			
H	L	D	QiO	Addressable Latch
H	H	QiO	QiO	Memory
L	L	D	L	8-Line Demultiplexer
L	H	L	L	Clear all Bits to "L"

Selected Inputs			Latch Addressed
C	B	A	
L	L	L	Q0
L	L	H	Q1
L	H	L	Q2
L	H	H	Q3
H	L	L	Q4
H	L	H	Q5
H	H	L	Q6
H	H	H	Q7

D :The level at the data input.
QiO :The level before the indicated steady-state input conditions were established (i = 0, 1,...7)



Logic Diagram

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Supply Voltage Range	V_{CC}	-0.5 ~ 7	V
DC Input Voltage	V_{IN}	-0.5 ~ V_{CC} + 0.5	V
DC Output Voltage	V_{OUT}	-0.5 ~ V_{CC} + 0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)*/180(SOIC)	mW
Storage Temperature	T_{stg}	-65 ~ 150	°C
Lead Temperature 10sec	T_L	300	°C

*500mW in the range of Ta = -40°C ~ 65°C. From Ta = 65°C to 85°C a derating factor of -10mW/°C shall be applied until 300mW.

Recommended Operating Conditions

Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC}	2 ~ 6	V
Input Voltage	V_{IN}	0 V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	-40 ~ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ~1000(V_{CC} = 2.0V) 0 ~ 500(V_{CC} = 4.5V) 0 ~ 400(V_{CC} = 6.0V)	ns

DC Electrical Characteristics

Parameter	Symbol	Test Condition		V_{CC}	Ta = 25°C Min.	Ta = 25°C Typ.	Ta = 25°C Max.	Ta = -40 ~ 85°C Min.	Ta = -40 ~ 85°C Max.	Unit
High-Level Input Voltage	V_{IH}	–		2.0 4.5 6.0	1.5 3.15 4.2	– – –	– – –	1.5 3.15 4.2	– – –	V
Low-Level Input Voltage	V_{IL}	–		2.0 4.5 6.0	– – –	– – –	0.5 1.35 1.8	– – –	0.5 1.35 1.8	V
High-Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} = -20µA	2.0 4.5 6.0	1.9 4.4 5.9	2.0 4.5 6.0	– – –	1.9 4.4 5.9	– – –	V
			I_{OH} = -4 mA I_{OH} = 5.2mA	4.5 6.0	4.18 5.68	4.31 5.80	– –	4.13 5.63	– –	
Low-Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 20µA	2.0 4.5 6.0	– – –	0.0 0.0 0.0	0.1 0.1 0.1	– – –	0.1 0.1 0.1	V
			I_{OL} = 4 mA I_{OL} = 5.2mA	4.5 6.0	– –	0.17 0.18	0.26 0.26	– –	0.33 0.33	
Input Leakage Current	I_{IN}	V_{IN} = V_{CC} or GND		6.0	–	–	±0.1	–	±1.0	µA
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		6.0	–	–	4.0	–	40.0	µA

Timing Requirements (Input $t_r = t_f = 6ns$)

Parameter	Symbol	Test Condition	V_{CC}	Ta = 25°C Typ.	Ta = 25°C Limit	Ta = -40 ~ 85°C Limit	Unit
Minimum Pulse Width ($\overline{G}$)	$t_{W(L)}$ $t_{W(H)}$	–	2.0	–	75	95	ns
			4.5	–	15	19	
			6.0	–	13	16	
Minimum Pulse Width ($\overline{CLEAR}$)	$t_{W(L)}$	–	2.0	–	75	95	
			4.5	–	15	19	
			6.0	–	13	16	
Minimum Set-up Time (DATA)	t_s	–	2.0	–	50	60	
			4.5	–	10	12	
			6.0	–	9	11	
Minimum Set-up Time (A, B, C)	t_s	–	2.0	–	25	30	
			4.5	–	5	6	
			6.0	–	5	5	
Minimum Hold Time (DATA)	t_h	–	2.0	–	25	30	
			4.5	–	5	6	
			6.0	–	5	5	
Minimum Hold Time (A, B, C)	t_h	–	2.0	–	0	0	MHz
			4.5	–	0	0	
			6.0	–	0	0	

AC Electrical Characteristics (C_L = 15pF, V_{CC} = 5V, Ta = 25°C)

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Output Transition Time	t_{TLH} t_{THL}	–	–	4	8	ns
Propagation Delay Time (DATA, Q)	t_{pLH} t_{pHL}	–	–	15	22	
Propagation Delay Time (A, B, C-Q)	t_{pLH} t_{pHL}	–	–	21	32	
Propagation Delay Time ($\overline{CLEAR}$-Q)	t_{pHL}	–	–	13	23	

AC Electrical Characteristics (C_L = 50pF, Input $t_r = t_f$ = 6ns)

Parameter	Symbol	Test Condition	V_{CC}	Ta = 25°C Min.	Ta = 25°C Typ.	Ta = 25°C Max.	Ta = -40 ~ 85°C Min.	Ta = -40 ~ 85°C Max.	Unit
Output Transition Time	t_{TLH} t_{THL}	–	2.0 4.5 6.0	– – –	30 8 7	75 15 13	– – –	95 19 16	ns
Propagation Delay Time (DATA-Q)	t_{pLH} t_{pHL}	–	2.0 4.5 6.0	– – –	56 18 15	130 26 22	– – –	165 33 28	ns
Propagation Delay Time (A, B, C)	t_{pLH} t_{pHL}	–	2.0 4.5 6.0	– – –	83 25 21	185 37 31	– – –	230 46 39	ns
Propagation Delay Time ($\overline{G}$-Q)	t_{pLH} t_{pHL}	–	2.0 4.5 6.0	– – –	67 20 17	165 33 28	– – –	205 41 35	ns
Propagation Delay Time ($\overline{CLEAR}$-Q)	t_{pHL}	–	2.0 4.5 6.0	– – –	52 16 14	135 27 23	– – –	170 34 29	ns
Input Capacitance	C_{IN}	–		–	5	10	–	10	pF
Power Dissipation Capacitance	C_{PD}(1)	–		–	35	–	–	–	pF

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:
$I_{CC(opr)} = C_{PD} \bullet V_{CC} \bullet f_{IN} + I_{CC}/4$(per Latch)

Notes