MOTOROLA

Octal D-Type Transparent Latch With Active Low Enable 3-State Inverted Outputs

ELECTRICALLY TESTED PER:
MIL-M-38510/34602

The 54F533 consists of eight latches with 3-state outputs for bus organized system applications. The flip-flops appear transparent to the data when Latch Enable (LE) is HIGH. When LE is LOW, the data that meets setup times is latched. Data appears on the bus when the Output Enable ($\overline{OE}$) is LOW. When $\overline{OE}$ is HIGH the bus output is in the high impedance state.

- Eight Latches in a Single Package
- 3-State Outputs for Bus Interfacing

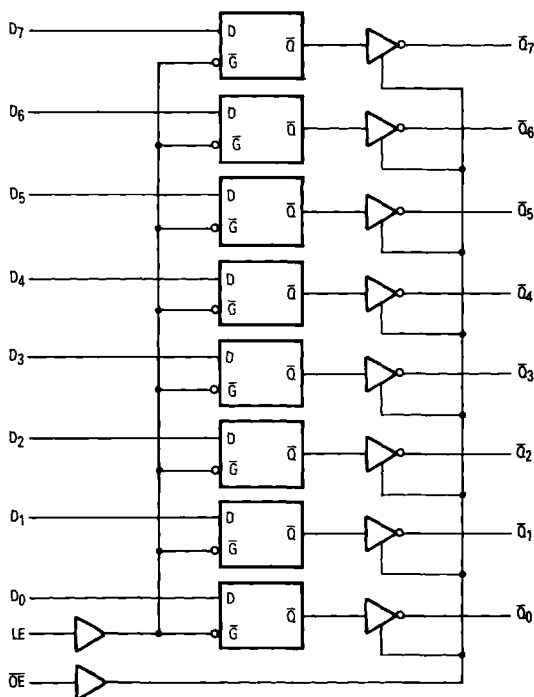**MPO**

AVAILABLE AS:

1) JAN: JM38510/34602BXA
2) SMD: *
3) 883C: 54F533/BXAJC

X = CASE OUTLINE AS FOLLOWS:
    PACKAGE: CERDIP: R
                 CERFLAT: S
                     LCC: 2
*Call Factory for latest update

LOGIC DIAGRAM

PIN ASSIGNMENTS

FUNCTION	DIL	FLATS	LCC	BURN-IN (CONDITION A)
$\overline{OE}$	1	1	1	V_{CC}
$\overline{Q}_0$	2	2	2	OPEN
D_0	3	3	3	V_{CC}
D_1	4	4	4	V_{CC}
$\overline{Q}_1$	5	5	5	OPEN
$\overline{Q}_2$	6	6	6	OPEN
D_2	7	7	7	V_{CC}
D_3	8	8	8	V_{CC}
$\overline{Q}_3$	9	9	9	OPEN
GND	10	10	10	GND
LE	11	11	11	V_{CC}
$\overline{Q}_4$	12	12	12	OPEN
D_4	13	13	13	V_{CC}
D_5	14	14	14	V_{CC}
$\overline{Q}_5$	15	15	15	OPEN
$\overline{Q}_6$	16	16	16	OPEN
D_6	17	17	17	V_{CC}
D_7	18	18	18	V_{CC}
$\overline{Q}_7$	19	19	19	OPEN
V_{CC}	20	20	20	V_{CC}

BURN-IN CONDITIONS:
V_{CC} = 5.0 V MIN/6.0 V MAX

54F533

TRUTH TABLE

Inputs		Outputs	
D_n	LE	$\overline{OE}$	$\overline{Q}_n$
H	⌐	L	H
L	⌐	L	L
X	X	H	Z

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = HIGH Impedance

CONNECTION DIAGRAM

V_{CC}	$\overline{Q}_7$	D_7	D_6	$\overline{Q}_6$	$\overline{Q}_5$	D_5	D_4	$\overline{Q}_4$	LE
20	19	18	17	16	15	14	13	12	11

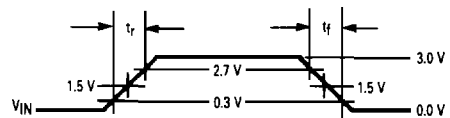| 1	2	3	4	5	6	7	8	9	10
$\overline{OE}$	$\overline{Q}_0$	D_0	D_1	$\overline{Q}_1$	$\overline{Q}_2$	D_2	D_3	$\overline{Q}_3$	GND
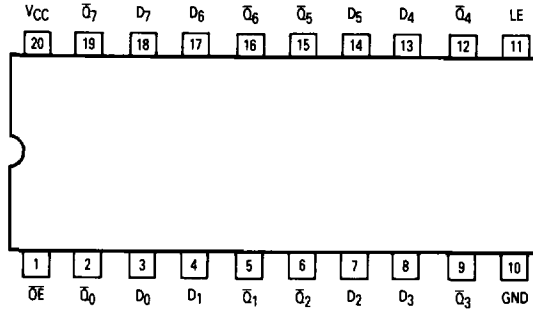
FUNCTIONAL DESCRIPTION

The 54F533 contains eight D-type latches with 3-state output buffers. When the Latch Enable (LE) input is HIGH, data on the D_n inputs enter the latches. In this condition the latches are transparent, i.e., a latch output will change state each time its D inputs at setup time preceding the HIGH-to-LOW transition of LE. The 3-state buffers are controlled by the Output Enable ($\overline{OE}$) input. When $\overline{OE}$ is LOW, the buffers are in the bi-state mode. When $\overline{OE}$ is HIGH the buffers are in the high impedance mode but this does not interfere with entering new data into the latches.
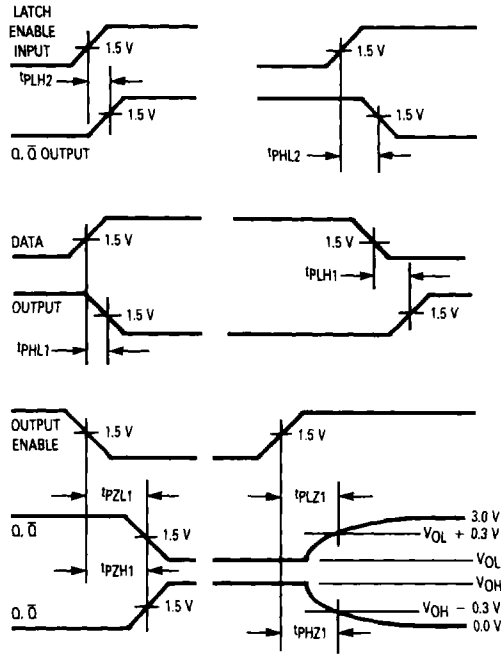
AC TEST CIRCUIT
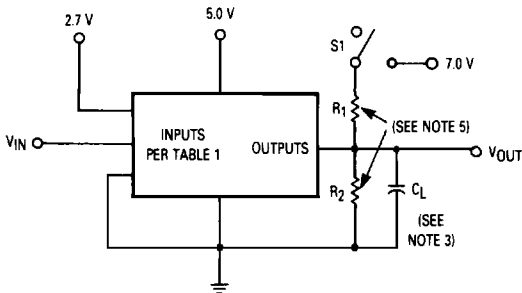
Test Type	S1
t_{PLH}	open
t_{PHL}	open
t_{PHZ}	open
t_{PZH}	open
t_{PLZ}	closed
t_{PZL}	closed

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WAVEFORMS

LATCH ENABLE INPUT — 1.5 V t_{PLH2} 1.5 V Q, $\overline{Q}$ OUTPUT t_{PHL2}

DATA — 1.5 V OUTPUT — 1.5 V t_{PHL1} t_{PLH1} 1.5 V

OUTPUT ENABLE — 1.5 V t_{PZL1} t_{PLZ1} Q, $\overline{Q}$ — 1.5 V t_{PZH1} t_{PHZ1} Q, $\overline{Q}$ — 1.5 V

3.0 V
V_{OL} + 0.3 V
V_{OL}
V_{OH}
V_{OH} − 0.3 V
0.0 V

DATA $t_{s(L)}$ $t_{h(L)}$ V_M LE V_M Q $\overline{Q}$ t_{PLH2} t_{PHL2} V_M

DATA V_M $t_{s(H)}$ $t_{h(H)}$ LE V_M $\overline{Q}$ Q t_{PLH2} t_{PHL2} V_M
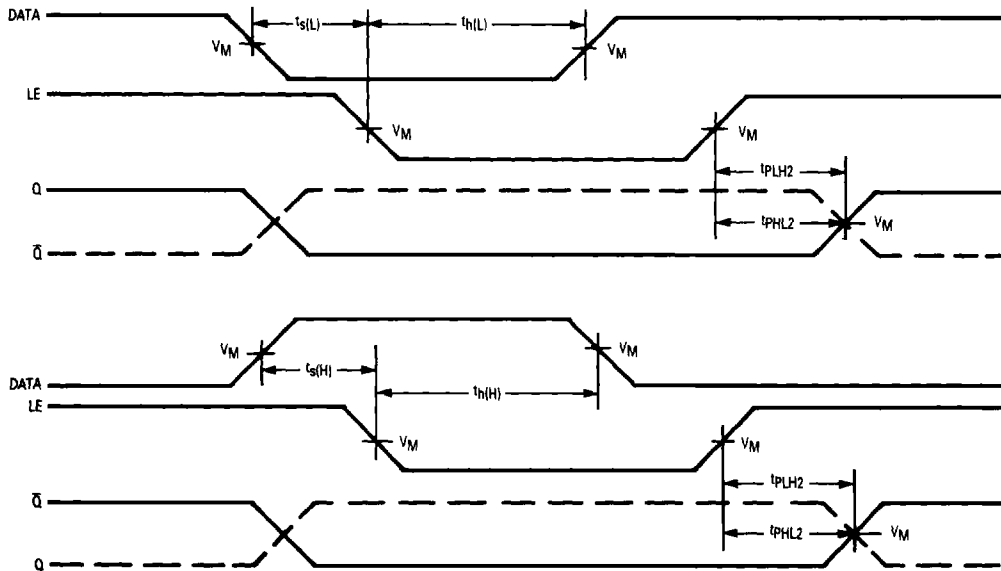
* $t_{s(H, L)}$ = 2.0 ns.
* $t_{h(H, L)}$ = 3.0 ns.
* Setup and Hold times are for information only. No testing required.

Symbol	Parameter	Limits						Units	Test Condition (Unless Otherwise Specified)
		+25°C		+125°C		−55°C			
		Subgroup 1		Subgroup 2		Subgroup 3			
	Static Parameters:	Min	Max	Min	Max	Min	Max		
V_{OH}	Logical "1" Output Voltage	2.5		2.5		2.5		V	V_{CC} = 4.5 V, I_{OH} = −1.0 mA, V_{IL} = 0.8 V, other inputs are open, $\overline{OE}$ = 0.8 V, LE = 2.0 V.
V_{OL}	Logical "0" Output Voltage		0.5		0.5		0.5	V	V_{CC} = 4.5 V, I_{OL} = 20 mA, V_{IH} = 2.0 V, other inputs are open, LE = 2.0 V, $\overline{OE}$ = 0.8 V.
V_{IC}	Input Clamping Voltage		−1.2					V	V_{CC} = 4.5 V, I_{IN} = −18 mA, other inputs are open.
I_{IH}	Logical "1" Input Current		20		20		20	µA	V_{CC} = 5.5 V, V_{IH} = 2.7 V, other inputs are open.
I_{IHH}	Logical "1" Input Current		100		100		100	µA	V_{CC} = 5.5 V, V_{IHH} = 7.0 V, other inputs are open.
I_{OD}	Diode Current	35		35		35		mA	V_{CC} = 4.5 V, V_{IN} = 5.5 V, other inputs are open, LE = 5.5 V, $\overline{OE}$ = 0 V, V_{OUT} = 2.5 V.
I_{IL}	Logical "0" Input Current	−0.03	−0.6	−0.03	−0.6	−0.03	−0.6	mA	V_{CC} = 5.5 V, V_{IN} = 0.5 V, other inputs are open.
I_{OS}	Output Short Circuit Current	−60	−150	−60	−150	−60	−150	mA	V_{CC} = 5.5 V, V_{IN} = 0 V, other inputs are open, V_{OUT} = 0 V, LE = 5.5 V, $\overline{OE}$ = 0 V.
I_{OZH}	Output Off Current High		50		50		50	µA	V_{CC} = 5.5 V, V_{IN} = 5.5 V, other inputs are open, V_{OUT} = 2.4 V, $\overline{OE}$ = 2.0 V, LE = 5.5 V.
I_{OZL}	Output Off Current Low		−50		−50		−50	µA	V_{CC} = 5.5 V, V_{IN} = 0 V, other inputs are open, V_{OUT} = 0.5 V, $\overline{OE}$ = 2.0 V, LE = 5.5 V.
I_{CCH}	Power Supply Current Off		50		50		50	mA	V_{CC} = 5.5 V, V_{IN} = 0 V (all inputs), LE = 5.5 V, $\overline{OE}$ = 0 V.
I_{CCL}	Power Supply Current Off		70		70		70	mA	V_{CC} = 5.5 V, V_{IN} = 5.5 V (all inputs), LE = 5.5 V, $\overline{OE}$ = 0 V.
I_{CCZ}	Power Supply Current Off		61		61		61	mA	V_{CC} = 5.5 V, all inputs are open, LE & $\overline{OE}$ = 5.5 V.
V_{IH}	Logical "1" Input Voltage	2.0		2.0		2.0		V	V_{CC} = 4.5 V.
V_{IL}	Logical "0" Input Voltage		0.8		0.8		0.8	V	V_{CC} = 4.5 V.
		Subgroup 7		Subgroup 8A		Subgroup 8B			
	Functional Tests								per Truth Table with V_{CC} = 4.5 V, **(Repeat at)** V_{CC} = 5.5 V, V_{INL} = 0.5 V, and V_{INH} = 2.5 V.

Symbol	Parameter	Limits						Units	Test Condition (Unless Otherwise Specified)
	Switching Parameters	+25°C		+125°C		−55°C			
		Subgroup 9		Subgroup 10		Subgroup 11			
		Min	Max	Min	Max	Min	Max		
tPHL1	Propagation Delay /Data-Output D_n to $\overline{Q}_n$	3.0	7.0	3.0	9.0	3.0	9.0	ns	$V_{CC} = 5.0$ V, $C_L = 50$ pF, $R_1 = R_2 = 499$ Ω.
tPLH1	Propagation Delay /Data-Output D_n to $\overline{Q}_n$	4.0	9.0	4.0	12	4.0	12	ns	$V_{CC} = 5.0$ V, $C_L = 50$ pF, $R_1 = R_2 = 499$ Ω.
tPHL2	Propagation Delay /Data-Output LE to $\overline{Q}_n$	3.0	7.0	3.0	9.0	3.0	9.0	ns	$V_{CC} = 5.0$ V, $C_L = 50$ pF, $R_1 = R_2 = 499$ Ω.
tPLH2	Propagation Delay /Data-Output LE to $\overline{Q}_n$	5.0	11	4.0	14	4.0	14	ns	$V_{CC} = 5.0$ V, $C_L = 50$ pF, $R_1 = R_2 = 499$ Ω.
tPLZ1	Output Disable Time, $\overline{OE}$ to $\overline{Q}_n$	2.0	5.5	2.0	7.5	2.0	7.5	ns	$V_{CC} = 5.0$ V, $C_L = 50$ pF, $R_1 = R_2 = 499$ Ω.
tPHZ1	Output Disable Time, $\overline{OE}$ to $\overline{Q}_n$	2.0	6.0	2.0	8.5	2.0	8.5	ns	$V_{CC} = 5.0$ V, $C_L = 50$ pF, $R_1 = R_2 = 499$ Ω.
tPZL1	Output Enable Time, $\overline{OE}$ to $\overline{Q}_n$	2.0	6.5	2.0	9.0	2.0	9.0	ns	$V_{CC} = 5.0$ V, $C_L = 50$ pF, $R_1 = R_2 = 499$ Ω.
tPZH1	Output Enable Time, $\overline{OE}$ to $\overline{Q}_n$	2.0	10	2.0	12.5	2.0	12.5	ns	$V_{CC} = 5.0$ V, $C_L = 50$ pF, $R_1 = R_2 = 499$ Ω.

NOTES:
1. Input pulse has the following characteristics: $t_r = t_f \leq 2.5$ ns, PRR $\leq$ 1.0 MHz, $Z_{OUT} = 50$ Ω.
2. Terminal conditions (pins not designated may be high $\geq$ 2.0 V, low $\leq$ 0.8 V, or open).
3. $C_L = 50$ pF $\simeq$ 10% including scope probe, wiring and stray capacitance, without package in test fixture.
4. Voltage measurements are to be made with respect to network ground terminal.
5. $R_1 = R_2 = 499$ Ω $\pm$ 5.0%.

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