

## Octal transceiver with dual enable; 3-state

74LVC623

## FEATURES

- Wide supply voltage range of 1.2 V to 3.6 V
- In accordance with the JEDEC standard no. 8-1A
- Flow-through pin-out architecture
- CMOS low power consumption
- inputs accept voltages upto 5.5 V
- Direct interface with TTL levels
- Output drive capability 50  $\Omega$  transmission lines @ 85 °C

## DESCRIPTION

The 74LVC623 is a high-performance, low-power, low-voltage, Si-gate CMOS device and superior to most advanced CMOS compatible TTL families. The 74LVC623 is an octal transceiver featuring non-inverting 3-state bus compatible outputs in both send and receive directions. This octal bus transceiver is designed for asynchronous two-way communication between data buses. The control function implementation allows maximum flexibility in timing. This device allows data transmission from the A bus to the B bus or from the B bus to the A bus, depending upon the logic levels at the enable inputs ( $OE_{AB}$ ,  $\overline{OE}_{BA}$ ). The enable inputs can be used to disable the device so that the buses are effectively isolated. The dual enable function configuration gives this transceiver the capability to store data by simultaneous enabling of  $OE_{AB}$  and  $\overline{OE}_{BA}$ . Each output reinforces its input in this transceiver configuration. Thus, when both control inputs are enabled and all other data sources to the two sets of the bus lines are at high impedance OFF-state, both sets of bus lines will remain at their last states. The 8-bit codes appearing on the two sets of buses will be identical.

The '623' is identical to the '620' but has true (non-inverting) outputs.

## QUICK REFERENCE DATA

GND = 0 V;  $T_{amb} = 25\text{ }^\circ\text{C}$ ;  $t_r = t_f \leq 2.5\text{ ns}$

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
$t_{PHL}/t_{PLH}$	propagation delay $A_n$ to $B_n$ ; $B_n$ to $A_n$	$C_L = 50\text{ pF}$ $V_{CC} = 3.3\text{ V}$	3.8	ns
$C_I$	input capacitance		5.0	pF
$C_{VO}$	input/output capacitance		10	pF
$C_{PD}$	power dissipation capacitance per buffer	notes 1 and 2	40	pF

## Notes to the quick reference data

1.  $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu\text{W}$ ):  
 $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$  where:  
 $f_i$  = input frequency in MHz;  $C_L$  = output load capacity in pF;  
 $f_o$  = output frequency in MHz;  $V_{CC}$  = supply voltage in V;  
 $\Sigma (C_L \times V_{CC}^2 \times f_o)$  = sum of outputs.
2. The condition is  $V_i = \text{GND to } V_{CC}$ .

## ORDERING INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74LVC623D	20	SO	plastic	SOT163-1
74LVC623DB	20	SSOP	plastic	SOT339-1
74LVC623PW	20	TSSOP	plastic	SOT360-1

## PINNING

PIN	SYMBOL	NAME AND FUNCTION
1	$OE_{AB}$	output enable input (active HIGH)
2, 3, 4, 5, 6, 7, 8, 9	$A_0$ to $A_7$	data inputs/outputs
10	GND	ground (0 V)
18, 17, 16, 15, 14, 13, 12, 11	$B_0$ to $B_7$	data inputs/outputs
19	$\overline{OE}_{BA}$	output enable input (active LOW)
20	$V_{CC}$	positive supply voltage

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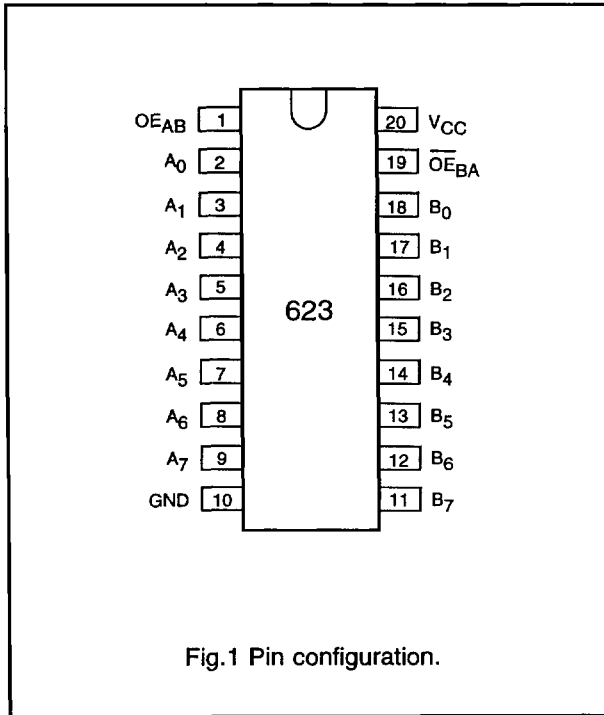


Fig.1 Pin configuration.

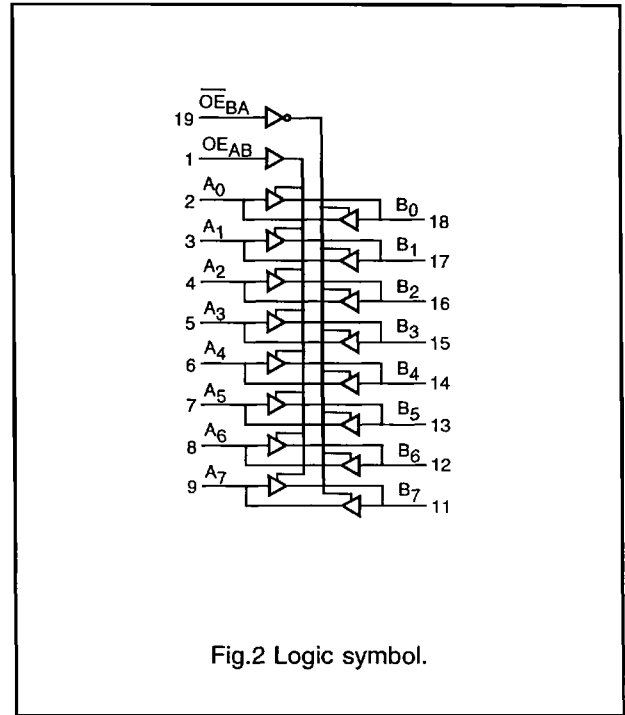


Fig.2 Logic symbol.

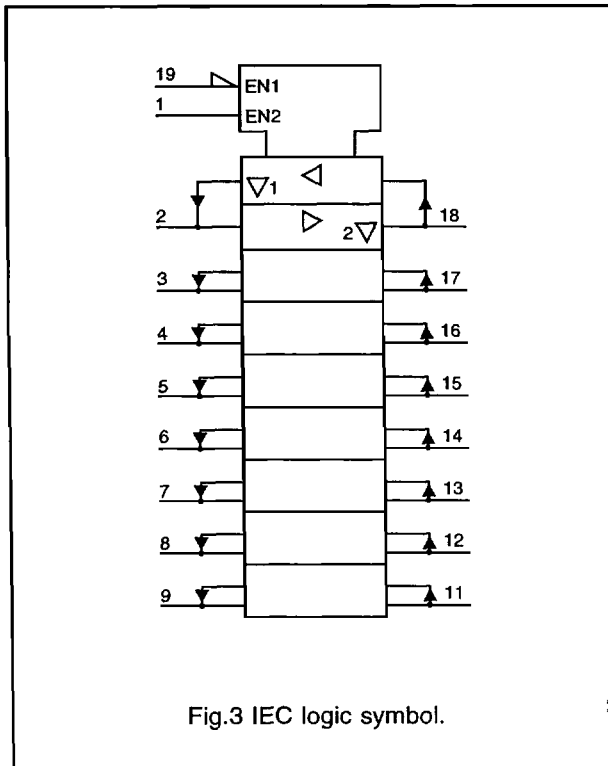


Fig.3 IEC logic symbol.

FUNCTION TABLE

INPUTS		INPUTS/OUTPUTS	
OE <sub>AB</sub>	OE <sub>BA</sub>	A <sub>n</sub>	B <sub>n</sub>
L	L	A = B	inputs
H	H	inputs	B = A
L	H	Z	Z
H	L	A = B inputs	inputs B = A

H = HIGH voltage level  
 L = LOW voltage level  
 Z = high impedance OFF-state

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**DC CHARACTERISTICS FOR 74LVC623**

For the DC characteristics see chapter "LVC family characteristics", section "Family specifications".

 $I_{CC}$  category: MSI**AC CHARACTERISTICS FOR 74LVC623**GND = 0 V;  $t_r = t_f \leq 2.5$  ns;  $C_L = 50$  pF

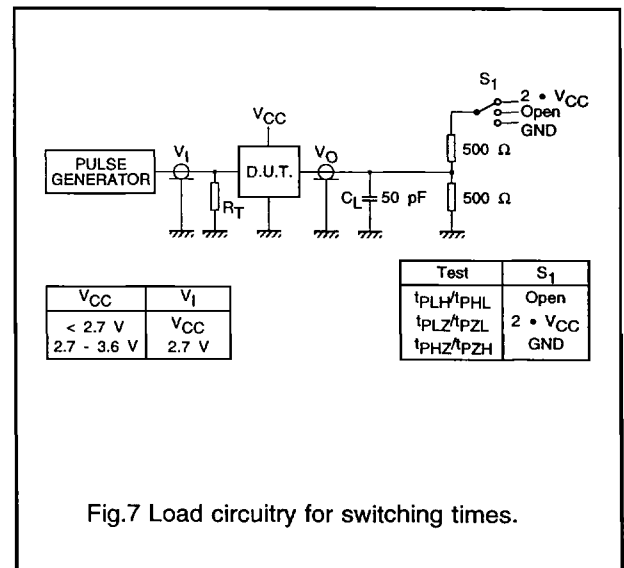
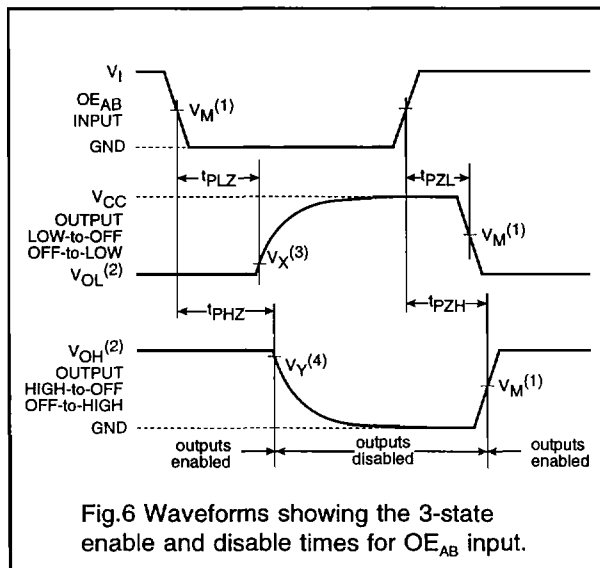
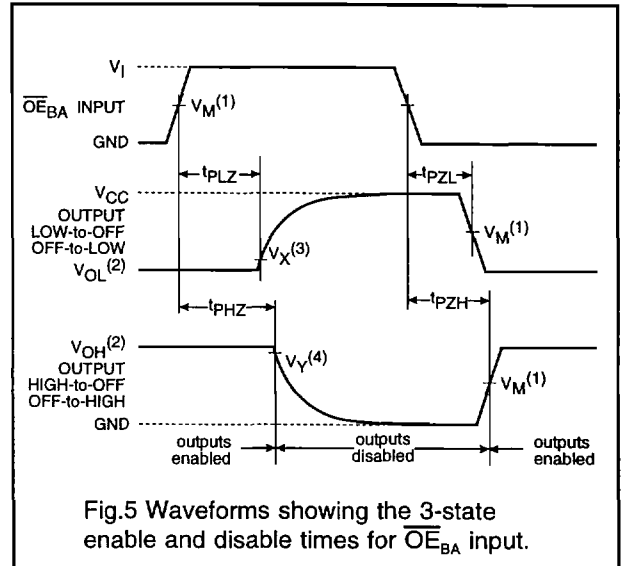
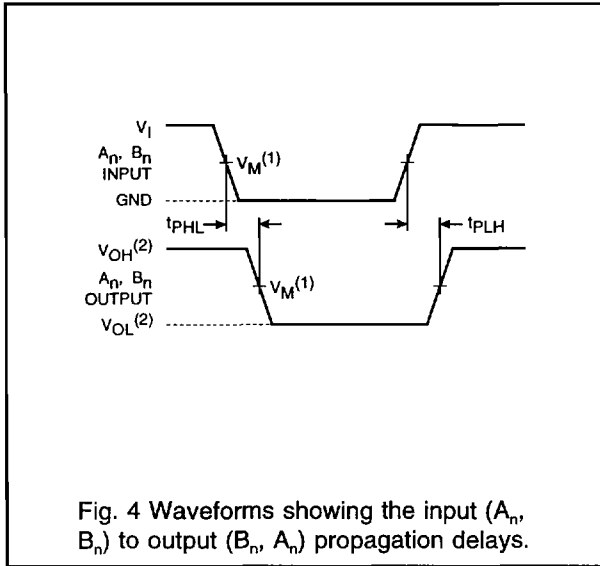
SYMBOL	PARAMETER	$T_{amb}$ (°C)			UNIT	TEST CONDITIONS	
		-40 to +85				$V_{CC}$ (V)	WAVEFORMS
		MIN.	TYP.	MAX.			
$t_{PHL}/t_{PLH}$	propagation delay	–	21	–	ns	1.2	Figs 4, 7
	$A_n$ to $B_n$ ;	1.5	4.6	8.5		2.7	
	$B_n$ to $A_n$	1.5	4.1*	7.5		3.0 to 3.6	
$t_{PZH}/t_{PZL}$	3-state output enable time	–	25	–	ns	1.2	Figs 6, 7
	$OE_{AB}$ to $B_n$	1.5	5.0	8.5		2.7	
		1.5	4.5*	7.5		3.0 to 3.6	
$t_{PHZ}/t_{PLZ}$	3-state output disable time	–	8	–	ns	1.2	Figs 6, 7
	$OE_{AB}$ to $B_n$	1.5	4.5	7.5		2.7	
		1.5	4.0*	6.5		3.0 to 3.6	
$t_{PZH}/t_{PZL}$	3-state output enable time	–	25	–	ns	1.2	Figs 5, 7
	$\overline{OE}_{BA}$ to $A_n$	1.5	5.0	8.5		2.7	
		1.5	4.5*	7.5		3.0 to 3.6	
$t_{PHZ}/t_{PLZ}$	3-state output disable time	–	8	–	ns	1.2	Figs 5, 7
	$\overline{OE}_{BA}$ to $A_n$	1.5	4.5	7.5		2.7	
		1.5	4.0*	6.5		3.0 to 3.6	

**Notes:** All typical values are measured at  $T_{amb} = 25$  °C.\* Typical values are measured at  $V_{CC} = 3.3$  V.

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AC WAVEFORMS



- Notes:
- (1)  $V_M = 1.5 \text{ V}$  at  $V_{CC} \geq 2.7 \text{ V}$   
 $V_M = 0.5 \cdot V_{CC}$  at  $V_{CC} < 2.7 \text{ V}$
  - (2)  $V_{OL}$  and  $V_{OH}$  are the typical output voltage drop that occur with the output load
  - (3)  $V_X = V_{OL} + 0.3 \text{ V}$  at  $V_{CC} \geq 2.7 \text{ V}$   
 $V_X = V_{OL} + 0.1 \cdot V_{CC}$  at  $V_{CC} < 2.7 \text{ V}$
  - (4)  $V_Y = V_{OH} - 0.3 \text{ V}$  at  $V_{CC} \geq 2.7 \text{ V}$   
 $V_Y = V_{OH} - 0.1 \cdot V_{CC}$  at  $V_{CC} < 2.7 \text{ V}$