F10000
4-BIT SHIFT REGISTER

GENERAL DESCRIPTION — The F10000 is a 4-Bit Parallel/Serial In, Parallel/Serial Out Shift Register. High Speed ECL technology permits storage, shifting, counting and serial code conversion at rates in excess of 200 MHz.

Features include assertion outputs for each stage, overriding asynchronous master reset, serial and parallel D type inputs and a gated clock. Availability of these features on one chip significantly improves the reliability, performance, and power consumption of high speed systems.

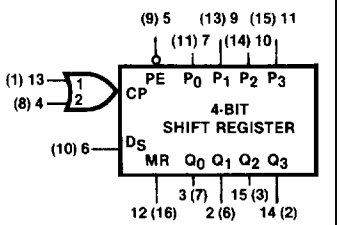
The F10000 incorporates a unique voltage compensation network which ensures that significant parameters such as logic levels, noise margins and speed remain constant over a wide range of power supply voltage.

- **HIGH SPEED . . . 200 MHz TYPICAL SHIFT FREQUENCY**
- **D TYPE INPUTS SERIAL AND PARALLEL**
- **GATED CLOCK INPUT**
- **ASYNCHRONOUS MASTER RESET**
- **TERMINATED LINE DRIVE CAPABILITY**
- **WIRED-OR CAPABILITY**
- **SEPARATE V_{CC} PINS ELIMINATE NOISE COUPLING**
- **50 kΩ INPUT PULL DOWNS . . . UNUSED INPUTS MAY BE LEFT OPEN**
- **SINGLE V_{EE} POWER SUPPLY . . . −4.7 V TO −6.2 V**
- **NOISE MARGINS INSENSITIVE TO POWER SUPPLY VARIATIONS AND GRADIENTS**

PIN NAMES

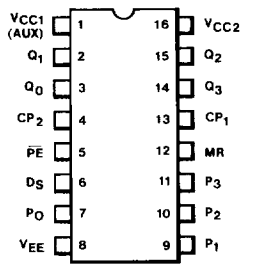
P_n	Parallel Data Inputs
PE	Parallel Enable (Active LOW)
CP_n	Clock In, Shifts on Positive Transition
MR	Asynchronous Master Reset—Active HIGH
D_S	Data Input, Serial
Q_n	Register Outputs

LOGIC SYMBOL

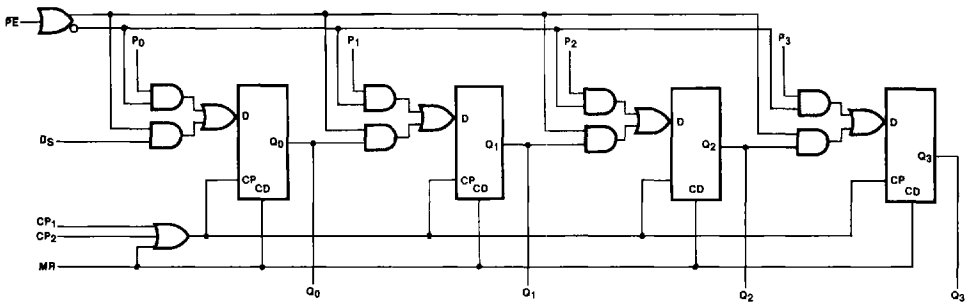


V_{CC1} = 1 (5)
V_{CC2} = 16 (4)
V_{EE} = 8 (12)
( ) = Flatpak

CONNECTION DIAGRAM
DIP (TOP VIEW)
PACKAGE OUTLINE 6B



LOGIC DIAGRAM



Note that this diagram is provided for understanding of logic operation only. It should not be used for evaluation of propagation delays as many gate functions are achieved internally without incurring a full gate delay.

FUNCTIONAL DESCRIPTION — The F10000 is a high-speed 4-Bit Shift Register. It consists of four master/slave flip-flops and four 2-input multiplexers interconnected so as to permit loading of the masters from either a preceding slave output (Q_{n-1}) or an external (P_n) input. The function desired is selected by the Parallel Enable (PE) input.

The masters are loaded during the LOW period of the clock (CP1, 2). As the clock changes from LOW to HIGH, the masters are inhibited from change followed by the enabling of the data path from master to slave. This data is then presented at the outputs (Q_n). While the clock is HIGH, the masters are inhibited from change and the master/slave data path remains open. During the HIGH to LOW transition of the clock, the master/slave data path is inhibited. This is followed by the enabling of the masters for the acceptance of data from the parallel or serial logic inputs.

As the two clock inputs are ORed together, both must be LOW for the masters to accept new data. If either is raised to a HIGH, the register is clocked.

A HIGH on one Clock input can prevent the register from shifting, providing a hold condition. To prevent false triggering, this input must change from LOW to HIGH while the clock is HIGH.

The Master Reset (MR) function is asynchronous. When held HIGH, it overrides all other commands and forces all outputs (Q_n) LOW.

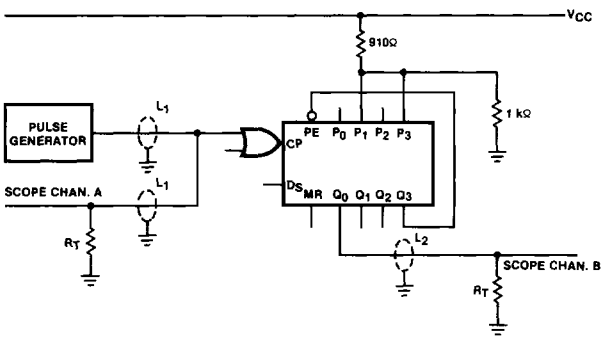
DC CHARACTERISTICS: $V_{EE} = -5.2$ V, $V_{CC} = GND$

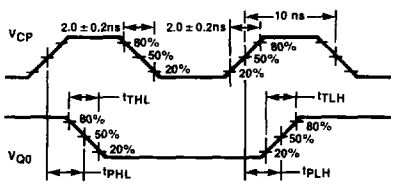
SYMBOL	CHARACTERISTIC	LIMITS			UNITS	T_A	CONDITIONS
		B	TYP	A			
I_{IH}	Input Current HIGH MR (Pin 12)			260 700	μA	25°C	$V_{IN} = V_{IHA}$
I_{EE}	Power Supply Current	−85	−66		mA	25°C	Outputs Open, Pin 4 or 13 Tied to V_{IH}

SWITCHING CHARACTERISTICS: $V_{EE} = -5.2$ V, $T_A = 25°C$

SYMBOL	CHARACTERISTIC	LIMITS			UNITS	CONDITIONS
		B	TYP	A		
f_{count}	Shift Right Frequency	150	200		MHz	See Figure 3
t_{PLH}	Propagation Delay Clock to Output	2.0	3.2	5.0	ns	See Figure 1
t_{PHL}	Propagation Delay Clock to Output	2.0	3.2	5.0	ns	
t_{PHL}	Propagation Delay Master Reset to Output		2.5		ns	See Figure 2
t_{TLH}	Output Transition Time LOW to HIGH (20% to 80%)	1.3	2.0	3.5	ns	See Figure 1
t_{THL}	Output Transition Time HIGH to LOW (80% to 20%)	1.3	2.0	3.5	ns	
t_w	Clock Pulse Width		2.5		ns	See Figure 3
t_w	MR Pulse Width		3.5		ns	
t_s	Set-Up Time Prior to Clock D_S to CP, P_n to CP	1.5	0.5		ns	
t_h	Hold Time After Clock D_S to CP, P_n to CP	1.0	−0.5		ns	
t_s	Set-Up Time Prior to Clock PE to CP	5.4	3.2		ns	
t_h	Hold Time After Clock PE to CP	0	−3.2		ns	

SWITCHING CIRCUITS AND WAVEFORMS

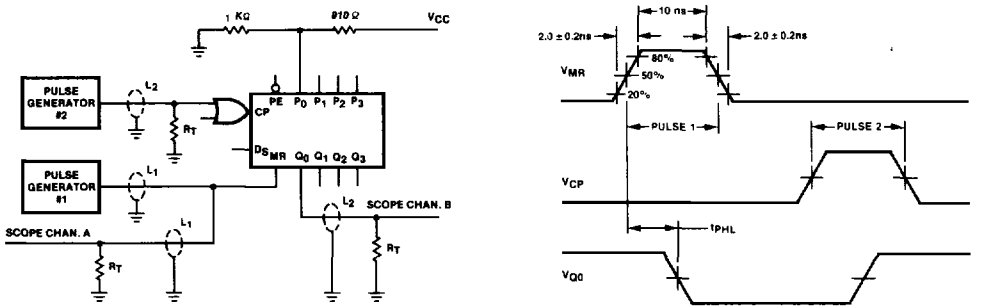




$L_1 = L_2 = 50\ \Omega$ impedence lines
$V_{CC} = +2.0$ V, Pin 1 and 16
$V_{EE} = -3.2$ V, Pin 8
$R_T = 50\ \Omega$ termination of scope
f = 10 MHz
Pulse Width = 10 ns

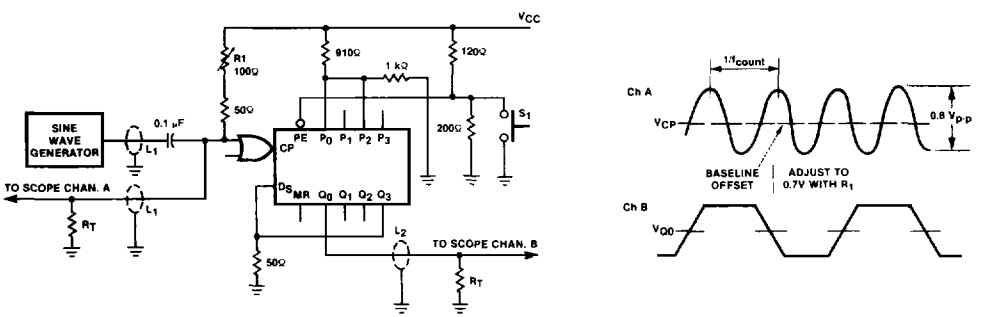
Fig. 1. Clock to Output, Output Transition Time

SWITCHING CIRCUIT AND WAVEFORMS (Cont'd)



$L_1 = L_2 = 50\ \Omega$ impedance lines.
$V_{CC1} = V_{CC2} = +2.0$ V
$V_{EE} = -3.2$ V
$R_T = 50\ \Omega$ Termination of Scope
f = 10 MHz
Pulse 2 ≃ Pulse 1

Fig. 2. Master Reset to Output



$L_1 = L_2 = 50\ \Omega$ impedance lines
$V_{CC1} = V_{CC2} = +2.0$ V
$R_T = 50\ \Omega$ termination of scope
$f = f_{MAX}$
Load the register by closing S_1

Fig. 3. Shift Frequency