01147

Am54/74157·Am9322

Quad Two-Input Multiplexer

Distinctive Characteristics:

- Selects four of eight data inputs with single select line and over-riding enable.
- 100% reliability assurance testing including high-temperature bake, temperature cycling, centrifuge and package hermeticity testing in compliance with MIL STD 883.
- Mixing privileges for obtaining price discounts. Refer to price list.
- Available in highly reliable molded epoxy, hermetic dual-in-line or Hermetic flat package.
- Electrically tested and optically inspected dice for the assemblers of hybrid products.

FUNCTIONAL DESCRIPTION

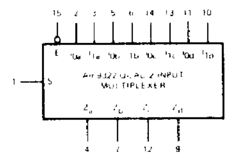
The Am9322 Quad Two-Input Multiplexer is the logic implementation of a four-pole, two-position switch with the position of the switch set by the logic level supplied to the select input. An active low enable is provided. The logic equations describing the device are given below.

$Z_a = \bar{E}(I_{0a}\bar{S} + I_{1a}S)$ $Z_c = \bar{E}(I_{0c}\bar{S} + I_{1c}S)$

$Z_b = \bar{E}(I_{0b}\bar{S} + I_{1b}S)$ $Z_d = \bar{E}(I_{0d}\bar{S} + I_{1d}S)$

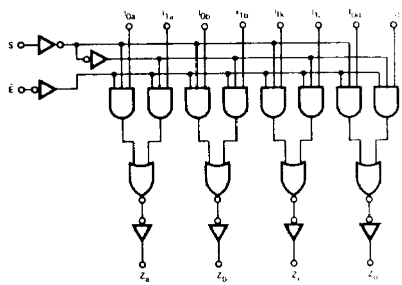
The Am9322 is useful for data bussing and general logic design. Some typical applications are shown in Figures 6 and 7.

LOGIC SYMBOL



V_{CC} = PIN 16
GND = PIN 8

LOGIC DIAGRAM



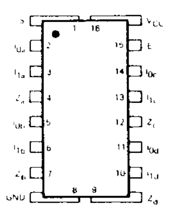
Am9322 ORDERING INFORMATION

Package Type	Temperature Range	Order Number
Molded DIP	0°C to +75°C	U6M932259X
Hermetic DIP	0°C to +75°C	U7B932259X
Hermetic DIP	−55°C to +125°C	U7B932251X
Hermetic Flat Pak	−55°C to +125°C	U4L932251X
Dice	Note	UXX9322XXD

Revised Ordering Information See Section 9

Note: The dice supplied will contain units which meet both 0°C to +75°C and −55°C to +125°C temperature ranges.

CONNECTION DIAGRAM
Top View



NOTE: PIN 1 is marked for orientation.

MAXIMUM RA ; (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°
Temperature (Ambient) Under Bias	−55°C to +125°
Supply Voltage to Ground Potential (Pin 16 to Pin 8) Continuous	−0.5 V to +7
DC Voltage Applied to Outputs for HIGH Output State	−0.5 V to $+V_{CC}$ m
DC Input Voltage	−0.5 V to +5.5
Output Current, Into Outputs	30
DC Input Current	−30 mA to +5.0

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

Am932259X T_A = 0°C to +75°C V_{CC} = 5.0 V ±5%
Am932251X T_A = −55°C to +125°C V_{CC} = 5.0 V ±10%

Parameters	Description	Test Conditions		Min.	Typ. (Note 1)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., I_{OH} = −0.8 mA V_{IN} = V_{IH} or V_{IL}		2.4	3.6		Volts
V_{OL}	Output LOW Voltage	V_{CC} = MIN., I_{OL} = 16.0 mA V_{IN} = V_{IH} or V_{IL}			0.2	0.4	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs		2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs				0.8	Volts
I_{IL} (Note 2)	Unit Load Input LOW Current	V_{CC} = MAX., V_{IN} = 0.4 V			−1.0	−1.6	mA
I_{IH} (Note 2)	Unit Load Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.4 V			4.0	40	μA
	Input HIGH Current	V_{CC} = MAX., V_{IN} = 5.5 V				1.0	mA
I_{SC}	Output Short Circuit Current	V_{CC} = MAX., V_{OUT} = 0.0 V		−30		−100	mA
I_{CC}	Power Supply Current	V_{CC} = MAX. All inputs and outputs HIGH	Am932251X		30	47	mA
			Am932259X		30	47	mA

Notes: 1) Typical Limits are at V_{CC} = 5.0 V, 25°C Ambient and maximum loading.
2) Actual input currents are obtained by multiplying unit load current by input load factor (See Loading Rules).

Am9322 Switching Characteristics (T_A = +25°C)

Parameters	Description		Test Conditions	Am932251X Min	Am932251X Typ	Am932251X Max	Am932259X Min	Am932259X Typ	Am932259X Max	Units
t_{pd+}(S)	Turn Off Delay	Select Input/Output		8	17	25	8	17	30	ns
t_{pd-}(S)	Turn On Delay	Select Input/Output	V_{CC} = 5.0 V	10	20	27	10	20	31	ns
t_{pd+}(D)	Turn Off Delay	Data Input/Output	C_L = 15 pF	4	10	17	5	10	22	ns
t_{pd-}(D)	Turn On Delay	Data Input/Output		4	11	16	5	11	18	ns
t_{pd+}($\bar{E}$)	Turn Off Delay	Enable Input/Output	(Refer to Figures 1 & 4)	6	12	20	6	12	24	ns
t_{pd-}($\bar{E}$)	Turn On Delay	Enable Input/Output		9	19	23	9	19	26	ns

54/. / Switching Characteristics (T_A = +25°C)

Parameter	Description	Test Condition	Min.	Typ.	Max.	Units
t_{pd+}	Data to Output	V_{CC} = 5V, C_L = 15 pF, R_L = 400Ω			14	ns
t_{pd-}					14	
t_{pd+}	Strobe to Output				20	ns
t_{pd-}					21	
t_{pd+}	Select to Output				23	ns
t_{pd-}					27	

EFINITION OF TERMS

BSCRIPT TERMS:

HIGH, applying to a HIGH-signal level or when used with V_{CC} indicate HIGH V_{CC} value.

Input.

LOW, applying to a LOW signal level or when used with V_{CC} indicate LOW V_{CC} value.

Output.

NCTIONAL TERMS:

-Out The logic HIGH or LOW output drive capability in terms input Unit Loads.

ut Unit Load One T²L gate input load. In the HIGH state it is ual to I_R and in the LOW state it is equal to I_F.

I_{ia}, I_{ib}, I_{ic}, I_{id} **Data Inputs** One of the two multiplexer data inputs multiplexers a, b, c or d. i = 0, 1.

Output The logic output of the two Input multiplexers. = a, b, c, d

ERATIONAL TERMS:

Forward input load current, for unit input load. Refer to Figure 5.

Output HIGH current, forced out of output in V_{OH} test. Refer to ure 5.

Output LOW current, forced into the output in V_{OL} test. Refer Figure 5.

I_{CC} The current drawn by the device with input and output terminals open.

I_{IH} Reverse input load current with V_{IH} applied to input. Refer to Figure 5.

Negative Current Current flowing out of the device.

Positive Current Current flowing into the device

V_{IH} Minimum logic HIGH input voltage. Refer to Figure 5.

V_{IL} Maximum logic LOW input voltage. Refer to Figure 5.

V_{OH} Minimum logic HIGH output voltage with output HIGH current I_{OH} flowing out of output. Refer to Figure 5.

V_{OL} Maximum logic LOW output voltage with output LOW current I_{OL} into output. Refer to Figure 5.

SWITCHING TERMS: (All switching times are measured at the 1.5 V logic level).

t_{pd+}(D) The propagation delay from a Data Input signal transition to the output LOW-HIGH transition. Refer to Figure 1.

t_{pd-}(D) The propagation delay from a Data Input signal transition to the output HIGH-LOW transition. Refer to Figure 1.

t_{pd+}($\bar{E}$) The propagation delay from the Enable Signal transition to the Z_a output LOW-HIGH transition. Refer to Figure 1.

t_{pd-}($\bar{E}$) The propagation delay from the Enable Signal transition to the Z_a output HIGH-LOW transition. Refer to Figure 1.

t_{pd+}(S) The propagation delay from the Select Input signal transition to the Z_a output LOW-HIGH transition. Refer to Figure 1.

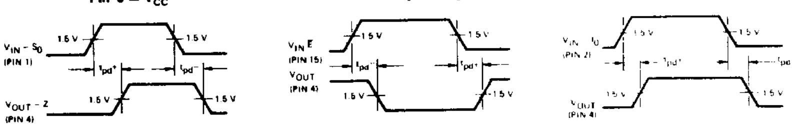
t_{pd-}(S) The propagation delay from the Select Input signal transition to the Z_a output HIGH-LOW transition. Refer to Figure 1.

SWITCHING TIME WAVEFORMS

t_{pd}; S to Z_a CONDITIONS
Pins 2, 15 = GND.
Pin 3 = V_{CC}

t_{pd}; $\bar{E}$ to Z_a CONDITIONS
All Other Inputs High

t_{pd}; I_{0a} to Z_a CONDITIONS
Pins 1, 15 = GND.



All Inputs are outputs of TTμL series gates loaded with 15 pF. All outputs are loaded with the same capacitance (referred to as C_L) and only with capacitance.

Figure 1

PERFORMANCE CURVES

Input Characteristics

Input Current Versus Input Voltage

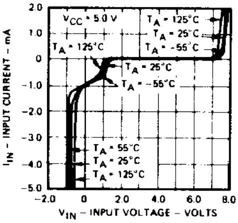
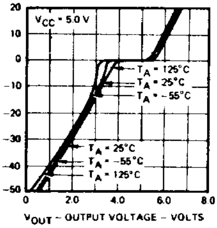


Figure 2

Output Characteristics

Output Current Versus Output Voltage (Output High)



Output Current Versus Output Voltage (Output Low)

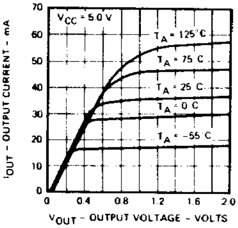
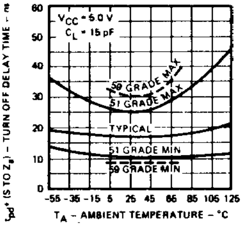


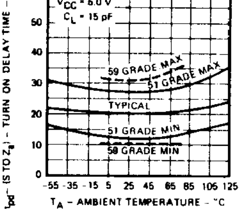
Figure 3

Switching Characteristics

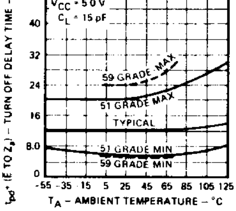
Turn Off Delay Time Versus Ambient Temperature (S to Z_a)



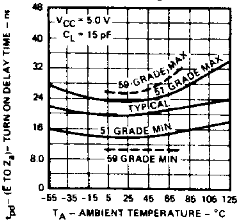
Turn On Delay Time Versus Ambient Temperature (S to Z_a)



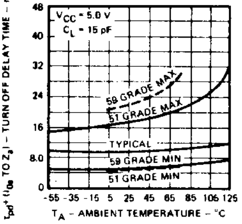
Turn Off Delay Time Versus Ambient Temperature ($\bar{E}$ to Z_a)



Turn On Delay Time Versus Ambient Temperature ($\bar{E}$ to Z_a)



Turn Off Delay Time Versus Ambient Temperature (I_{0a} to Z_a)



Turn On Delay Time Versus Ambient Temperature (I_{0a} to Z_a)

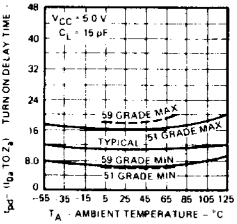


Figure 4

TRUTH TABLE

Enable	Select Input	Data Inputs		Output
$\bar{E}$	S	I_{0i}	I_{1i}	Z_i
H	X	X	X	L
L	H	X	L	L
L	H	X	H	H
L	L	L	X	L
L	L	H	X	H

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
I = a, b, c, d

TABLE I

MSI INTERFACING RULES

Interfacing Digital Family	Equivalent Input Unit Load HIGH	LOW
Advanced Micro Devices 9300/2500 Series	1	1
FSC Series 9300	1	1
TI Series 54/7400	1	1
Signetics Series 8200	2	2
National Series DM 75/85	1	1
DTL Series 930	12	1

TABLE III

Am9322 LOADING RULES (in unit loads)

Input/Output	Pin Nos.	Input Load	Output Drive HIGH	Output Drive LOW
S	1	1	—	—
I_{0a}	2	1	—	—
I_{1a}	3	1	—	—
Z_a	4	—	20	10
I_{0b}	5	1	—	—
I_{1b}	6	1	—	—
Z_b	7	—	20	10
GND	8	—	—	—
Z_d	9	—	20	10
I_{1d}	10	1	—	—
I_{0d}	11	1	—	—
Z_c	12	—	20	10
I_{1c}	13	1	—	—
I_{0c}	14	1	—	—
$\bar{E}$	15	1	—	—
V_{CC}	16	—	—	—

TABLE II

INPUT/OUTPUT INTERFACE CONDITIONS

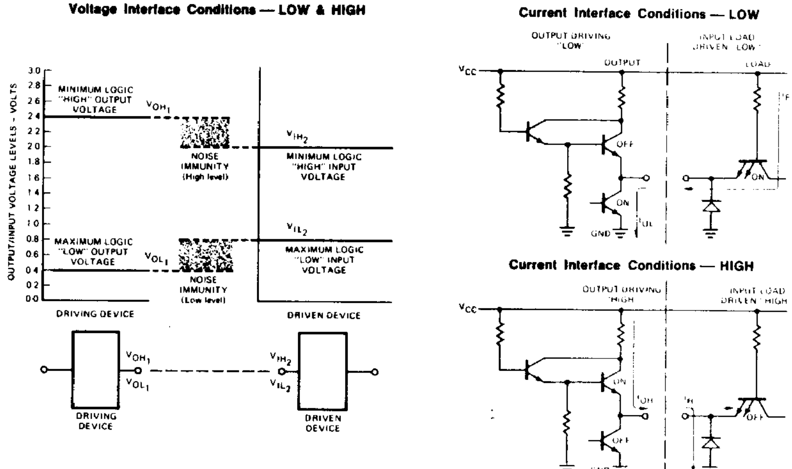
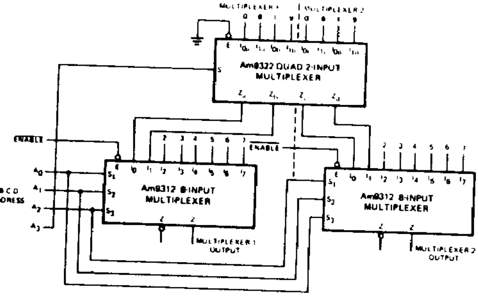


Figure 5

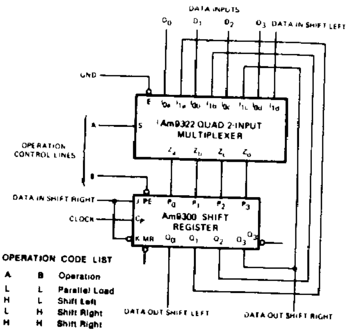
Am9322 APPLICATIONS



Dual 10-Input Multiplexer

Two 10-input Multiplexers are shown above with the select lines common to the two multiplexers. Inputs are selected by an 8421 BCD Address.

Figure 6



OPERATION CODE LIST

A	B	Operation
L	L	Parallel Load
H	L	Shift Left
L	H	Shift Right
H	H	Shift Right

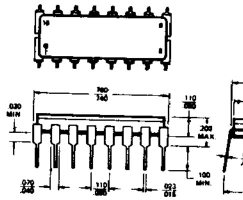
Shift Left, Shift Right, Parallel Load Register

This register will shift left, shift right, and load 4 bits of parallel data according to the operation code applied to A and B.

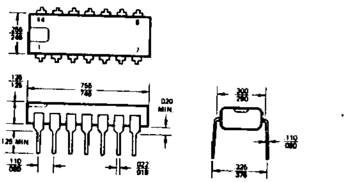
Figure 7

PHYSICAL DIMENSIONS
Dual-In-Line

Hermetic

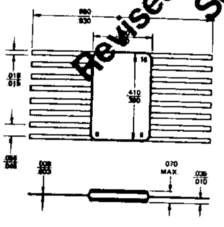


Molded



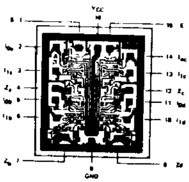
Revised Package Information
See Section 9

Flat Package



Metallization and Pad Layout

60 x 69 Mils



ADVANCED MICRO DEVICES INC.
901 Thompson Place
Sunnyvale
California 94086
(408) 732-2400
TWX: 910-339-9280
TELEX: 34-6306

Advanced Micro Devices can not assume responsibility for use of any circuitry described other than circuitry entirely embodied in an Advanced Micro Devices product. (2)

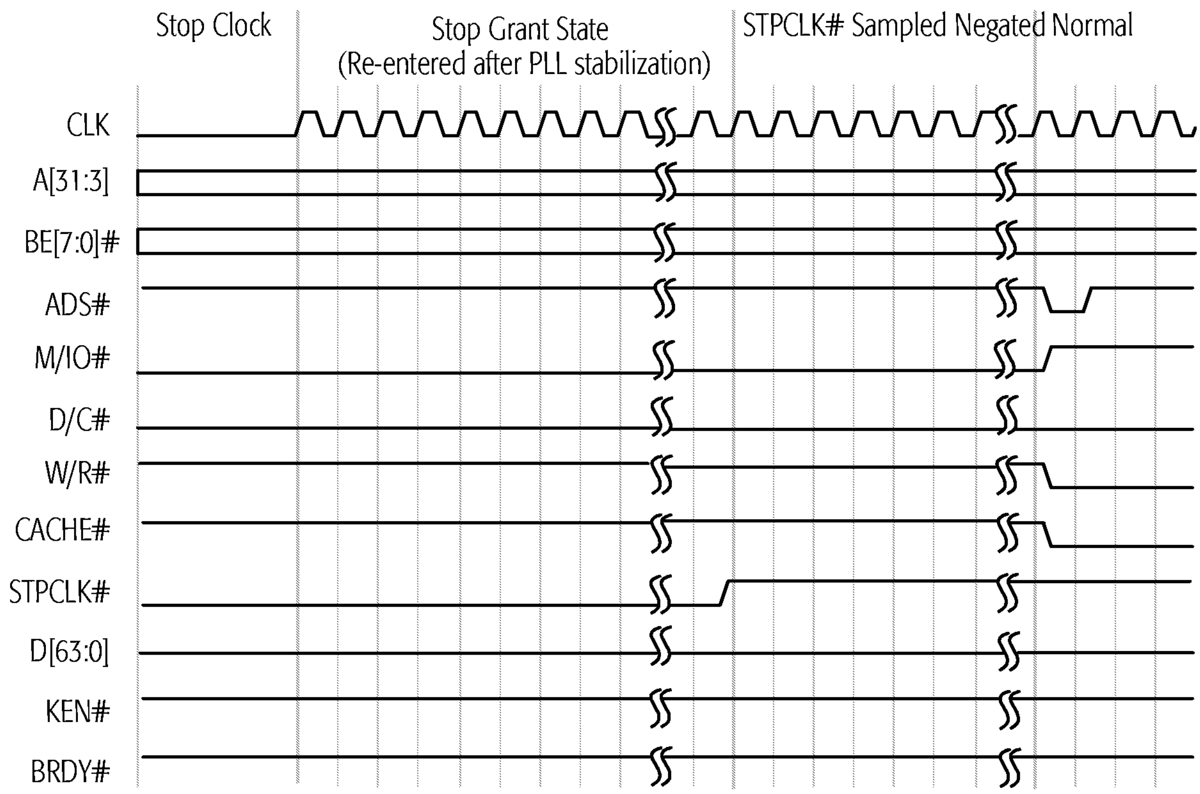


Figure 75. Stop Grant and Stop Clock Modes, Part 2

INIT-Initiated Transition from Protected Mode to Real Mode

INIT is typically asserted in response to a BIOS interrupt that writes to an I/O port. This interrupt is often in response to a Ctrl-Alt-Del keyboard input. The BIOS writes to a port (similar to port 64h in the keyboard controller) that asserts INIT. INIT is also used to support 80286 software that must return to Real mode after accessing extended memory in Protected mode.

The assertion of INIT causes the processor to empty its pipelines, initialize most of its internal state, and branch to address FFFF_FFF0h—the same instruction execution starting point used after RESET. Unlike RESET, the processor preserves the contents of its caches, the floating-point state, the MMX state, Model-Specific Registers (MSRs), the CD and NW bits of the CR0 register, the time stamp counter, and other specific internal resources.

Figure 76 shows an example in which the operating system writes to an I/O port, causing the system logic to assert INIT. The sampling of INIT asserted starts an extended microcode sequence that terminates with a code fetch from FFFF_FFF0h, the reset location. INIT is sampled on every clock edge but is not recognized until the next instruction boundary. During an I/O write cycle, it must be sampled asserted a minimum of three clock edges before BRDY# is sampled asserted if it is to be recognized on the boundary between the I/O write instruction and the following instruction. If INIT is asserted synchronously, it can be asserted for a minimum of one clock. If it is asserted asynchronously, it must have been negated for a minimum of two clocks, followed by an assertion of a minimum of two clocks.

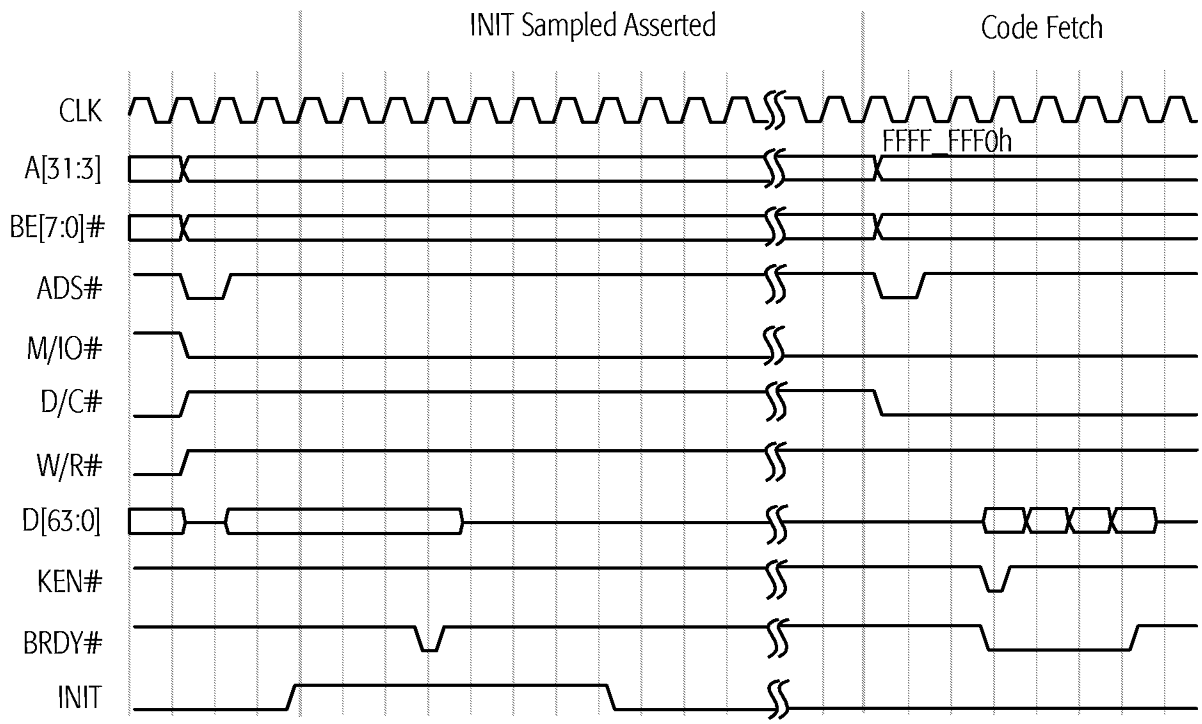


Figure 76. INIT-Initiated Transition from Protected Mode to Real Mode

6 Power-on Configuration and Initialization

On power-on the system logic must reset the AMD-K6-2 processor by asserting the RESET signal. When the processor samples RESET asserted, it immediately flushes and initializes all internal resources and its internal state, including its pipelines and caches, the floating-point state, the MMX and 3DNow! states, and all registers. Then the processor jumps to address FFFF_FFF0h to start instruction execution.

6.1 Signals Sampled During the Falling Transition of RESET

FLUSH# FLUSH# is sampled on the falling transition of RESET to determine if the processor begins normal instruction execution or enters Tri-State Test mode. If FLUSH# is High during the falling transition of RESET, the processor unconditionally runs its Built-In Self Test (BIST), performs the normal reset functions, then jumps to address FFFF_FFF0h to start instruction execution. (See “Built-In Self-Test (BIST)” on page 217 for more details.) If FLUSH# is Low during the falling transition of RESET, the processor enters Tri-State Test mode. (See “Tri-State Test Mode” on page 218 and “FLUSH# (Cache Flush)” on page 103 for more details.)

BF[2:0] The internal operating frequency of the processor is determined by the state of the bus frequency signals BF[2:0] when they are sampled during the falling transition of RESET. The frequency of the CLK input signal is multiplied internally by a ratio defined by BF[2:0]. (See “BF[2:0] (Bus Frequency)” on page 92 for the processor-clock to bus-clock ratios.)

BRDYC# BRDYC# is sampled on the falling transition of RESET to configure the drive strength of A[20:3], ADS#, HITM#, and W/R#. If BRDYC# is Low during the fall of RESET, these outputs are configured using higher drive strengths than the standard strength. If BRDYC# is High during the fall of RESET, the standard strength is selected. (See “BRDYC# (Burst Ready Copy)” on page 95 for more details.)

6.2 RESET Requirements

During the initial power-on reset of the processor, RESET must remain asserted for a minimum of 1.0 ms after CLK and V_{CC} reach specification. (See “CLK Switching Characteristics” on page 255 for clock specifications. See “Electrical Data” on page 247 for V_{CC} specifications.)

During a warm reset while CLK and V_{CC} are within specification, RESET must remain asserted for a minimum of 15 clocks prior to its negation.

6.3 State of Processor After RESET

Output Signals

Table 31 shows the state of all processor outputs and bidirectional signals immediately after RESET is sampled asserted.

Table 31. Output Signal State After RESET

Signal	State	Signal	State
A[31:3], AP	Floating	LOCK#	High
ADS#, ADSC#	High	M/IO#	Low
APCHK#	High	PCD	Low
BE[7:0]#	Floating	PCHK#	High
BREQ	Low	PWT	Low
CACHE#	High	SCYC	Low
D/C#	Low	SMIACT#	High
D[63:0], DP[7:0]	Floating	TDO	Floating
FERR#	High	VCC2DET	Low
HIT#	High	VCC2H/L#	Low
HITM#	High	W/R#	Low
HLDA	Low	–	–

Registers

Table 32 on page 175 shows the state of all architecture registers and Model-Specific Registers (MSRs) after the processor has completed its initialization due to the recognition of the assertion of RESET.